デザイン・ガイド: TIDA-01623
$30W/in^3$、93.4% 効率、100W AC/DC アダプタのリファレンス・デザイン

概要

このテスト済みリファレンス・デザインは、ノート PC アダプタやスマートフォン用充電器アプリケーション向けの、広い入力電圧範囲 (100～240VAC) に対応した高効率、高電力密度の AC/DC アダプタ・ソリューションです。このデザインは、UCC28056 ベースのフロント・エンド遷移モード (TM) 力率補正 (PFC) 回路と、後段にある UCC28780 ベースの絶縁 DC/DC 変換用アクティブ・クランプ・フライバックで構成されています。

リソース

TIDA-01623	デザイン・フォルダ
UCC28056	プロダクト・フォルダ
UCC28780	プロダクト・フォルダ
UCC24612	プロダクト・フォルダ
ISO7710F	プロダクト・フォルダ
ATL431LI	プロダクト・フォルダ
LMC7111	プロダクト・フォルダ
LP2981-N	プロダクト・フォルダ
TPD1E05U06-Q1	プロダクト・フォルダ
CSD17575Q3	プロダクト・フォルダ

TI E2E™ Community

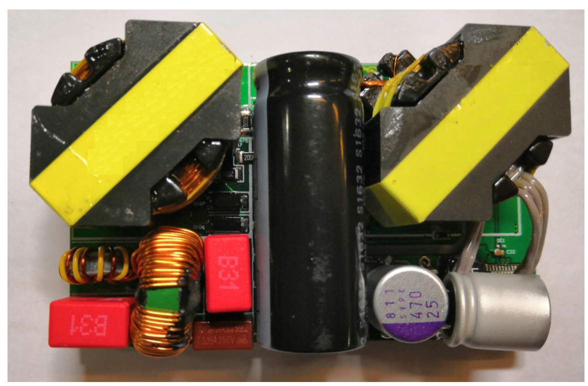
E2E™エキスパートに質問

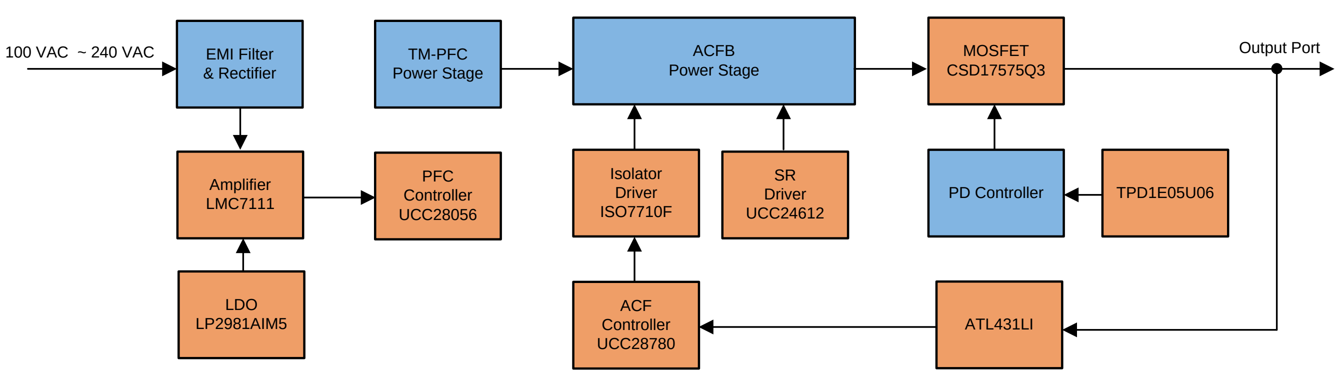
特長

- 広い動作入力電圧範囲: 100～240V_{AC}、全電圧範囲で最大電力を供給
- 自然冷却で高効率(ピーク値 93.4%)
- 5V/5A、9V/5A、15V/5A、20V/5A の出力構成
- 低スタンバイ消費電力(130mW)
- 小サイズ(70 × 42 × 16.5mm)
- 高い電力密度($30W/in^3$)

アプリケーション

- ノート PC 向け電源アダプタの設計
- モバイル向け充電器の設計
- その他の AC/DC アダプタ/電源
- 産業用AC/DC





1 System Description

Notebook PCs and smartphones need adapters to charge their batteries. USB Power Delivery (PD) negotiation allows devices to create a contract to deliver the optimum power level for each application under the current battery conditions. This protocol expands USB to deliver up to 100 W (20 V, 5 A) of power. High efficiency and high power density are required for the adapter to save power and make the device easier to carry. A notebook adapter is an AC/DC converter. 図 1 shows a typical diagram of this converter. When the output power is higher than 75 W, a power factor correction (PFC) stage is required.

The global regulatory environment surrounding the legislation of external power supply efficiency and no-load power draw has rapidly evolved in the last decade. The newer generation power supplies need to meet multiple norms such as United States Department of Energy (DoE) Level VI standard.

This adapter reference design operates over a wide input voltage range from 100-V to 240-V AC and must be able to power different equipment with different voltage demands automatically. The circuit consists of a front-end transition mode (TM) power factor correction (PFC) circuit, followed by an active-clamp, flyback-based isolated DC/DC power stage. The design uses the UCC28056 controller for the PFC stage and the UCC28780 controller for the ACF stage to achieve a compact and robust control structure. Synchronous rectification based on the UCC24612 helps achieve higher efficiencies. Gallium nitride (GaN) FETs are used in this design to achieve high switching frequency. When faults such as over-current, over-power, and over-voltage happen, the adapter reacts quickly to protect the terminal device.

This reference design is a high efficiency, high power density, 100-W output power AC/DC adapter that achieves a peak efficiency of 93.4% and a 30-W/in^3 power density. The input voltage ranges from 100 V to 240 V_{AC}, and the output could be configured as 5-V/5-A, 9-V/5-A, 15-V/5-A, and 20-V/5-A outputs. When an over-current, short-circuit, or over-power event occurs, this adapter reference design can cut off the output and recovery automatically. With over-voltage, the adapter is latched to avoid further damage to the terminal devices. Also, this adapter meets low no-load power consumption, which is less than 130 mW.

This converter operates at a high switching frequency near 500 kHz, which helps decrease the size of the transformer and capacitors. This design is fully tested and validated for various parameters such as regulation, efficiency, output ripple, startup, and switching stresses. Overall, the design meets the key challenges of adapter power supplies to provide safe and reliable power with all protections built in, while delivering high performance with low power consumption

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	CONDITIONS	SPECIFICATIONS			UNIT
		MIN	TYP	MAX	
INPUT CHARACTERISTICS					
Input voltage (VINAC)	-	100	230	240	V_{AC}
Frequency (fLINE)	-	47	50	63	Hz
Brown-in voltage	-		82		Hz
Brown-out voltage	-		77		Hz

表 1. Key System Specifications (continued)

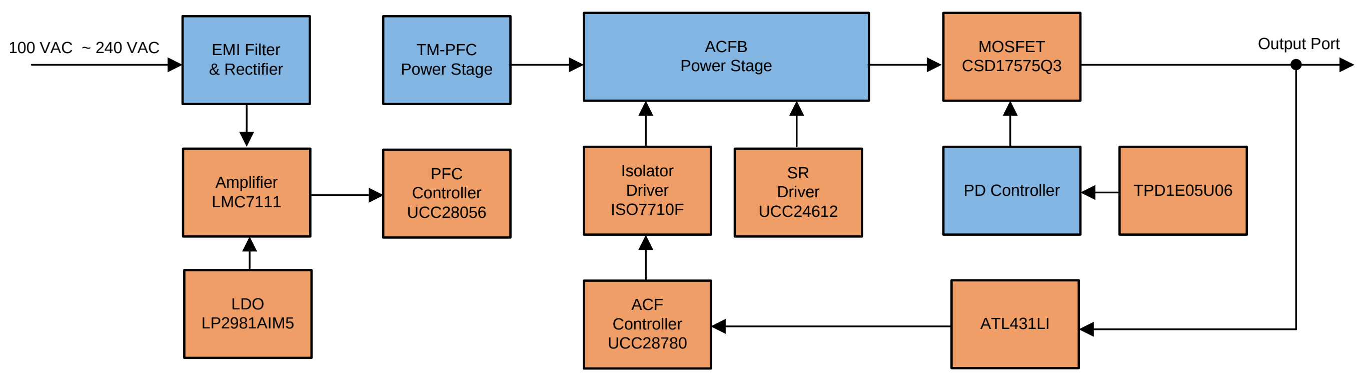
PARAMETER	CONDITIONS	SPECIFICATIONS			UNIT
		MIN	TYP	MAX	
OUTPUT CHARACTERISTICS					
Output voltage	5-V sink attached	4.95	5	5.05	V
	9-V sink attached	8.91	9	9.09	
	15-V sink attached	14.85	15	15.15	V
	20-V sink attached	19.8	20	20.2	
Output voltage	5-V sink attached		5		A
	9-V sink attached		5		A
	15-V sink attached		5		A
	20-V sink attached		5		A
Load regulation	5-V sink attached		5%		V_{out}
	9-V sink attached		5%		V_{out}
	15-V sink attached		5%		V_{out}
	20-V sink attached		5%		V_{out}
Ripple and noise	5-V sink attached		150		mV
	9-V sink attached		200		mV
	15-V sink attached		200		mV
	20-V sink attached		200		mV
Maximum output power	For 20 V_{out}			100	W
SYSTEM CHARACTERISTICS					
Peak efficiency	Low Line		92.6		%
	High Line		93.4		%
Operating ambient temperature				55	°C
Board form factor	Length×Breadth×Height	70	42	16.5	mm

2 System Overview

2.1 Block Diagram

図 1 shows the high-level block diagram of the circuit. The circuit consists of a front-end transition mode (TM) power factor correction (PFC) circuit, followed by an active-clamp flyback-based isolated DC/DC power stage. The design uses the UCC28056 controller for the PFC stage and the UCC28780 controller for the ACF stage to achieve a compact and robust control structure. The synchronize rectifier controller UCC24612-1 controls the synchronize rectifier MOSFET for better efficiency performance. For high-efficiency needs, GaN-FET is used as the primary switch. The main switching devices are NV6115 and NV6117 GaN devices from Navitas Semiconductor, Inc. The output voltage could be configured as 5-V/5-A, 9-V/5-A, 15-V/5-A, and 20-V/5-A outputs. The design achieves a peak efficiency of 93.4% at a very high switching frequency. The power density of the design has been increased to 30 W/in^3, which is much higher than traditional solutions.

図 1. TIDA-01623 Block Diagram



2.2 Highlighted Products

2.2.1 UCC28056

To implement the high performance, small form factor PFC design at 100-W power, the UCC28056 is the preferred controller as it offers a series of benefits to address the next generation's need for low total harmonic distortion (THD) norms for desktop PC power supplies.

The UCC28056 is a high-performance, 6-pin, fully-featured PFC controller that is small in size and offers excellent light load efficiency and standby power. The UCC28056 simplifies the design of power supply systems requiring good power factor that must also be capable of meeting today's tough standards for efficiency and standby power. At full load, the UCC28056 operates the PFC power stage at maximum switching frequency in transition mode. At reduced load, the part transitions seamlessly into discontinuous conduction mode, automatically reducing switching frequency for maximum efficiency. At light load, DCM operation is combined with burst mode operation to further improve light load efficiency and standby power. The UCC28056 integrates all the features necessary to implement a high performance and robust PFC stage into a 6-pin package and requires a minimal number of external components to interface with the power stage. The UCC28056 maximizes the BOM savings by eliminating need of auxiliary winding.

Key specifications include:

- Innovative DCM control law to prevent valley jumping
- Superior no-load and light-load efficiency

- Robust protection: fast response 2nd OVP on a dedicated pin
- Soft-start and soft recovery after OVP
- Input voltage brown out detection
- Eliminates need of auxiliary winding
- Innovative DCM control law to prevent valley jumping
- Strong drive capability: -1.0 A and 0.8 A

2.2.2 UCC28780

The UCC28780 is a high-frequency active-clamp flyback controller that enables high-density AC/DC power supplies that comply with stringent global efficiency standards. Zero voltage switching (ZVS) is achieved over a wide operating range with an advanced auto-tuning technique, adaptive dead time optimization, and variable switching frequency control law. Along with multimode control that changes the operation based on input and output conditions, the UCC28780 controller enables high efficiency without the risk of audible noise. The controller has a variable switching frequency of up to 1 MHz and accurate programmable operating performance points (OPP), which provides consistent thermal design power across a wide line range. This consistent power means passive components can be further reduced and enable high power density.

Key features for this device include:

- Configurable with external Si or GaN FETs
- Adaptive burst control for light-load efficiency with low output ripple and no audible noise
- Secondary-side regulation allows for dynamically scalable output voltage
- Internal soft start
- Brownout detection without direct line sensing
- Fault protections: internal overtemperature, output overvoltage, overcurrent, short circuit, and pin fault
- NTC resistor interface with external enable

2.2.3 UCC24612

The UCC24612 is a high-performance controller and driver for standard and logic-level N-channel MOSFET power devices used for low-voltage, secondary-side synchronous rectification. The combination of controller and MOSFET emulates a near-ideal diode rectifier. This solution not only directly reduces power dissipation of the rectifier, but also indirectly reduces primary-side losses as well due to compounding of efficiency gains. Using drain-to-source voltage sensing, the UCC24612 is ideal for ACF power supplies. This device is available in a 5-pin SOT-23-5 package.

Key features for this device include:

- Up to 1-MHz operating frequency
- VDS MOSFET sensing
- 4-A sink, 1-A source gate-drive capability
- Micro-power sleep current for 90+ designs
- Automatic light-load management
- Synchronous wake-up from sleep and light-load modes
- Adaptive minimum off time for better noise immunity

- 16-ns typical turnoff propagation delay
- 9.5-V gate drive clamp levels for minimum driving loss

2.2.4 LP2981-N

The LP2981-N families of fixed-output, low-dropout regulators offer exceptional, cost-effective performance for both portable and non-portable applications. Available in fixed voltages of 2.8 V, 3 V, 3.3 V, and 5 V, the family has an output tolerance of 0.75% for the A-grade devices and is capable of delivering 100-mA continuous load current. Standard regulator features, such as overcurrent and overtemperature protection, are included.

Key features for this device include:

- Output tolerance of 0.75% (A grade) 1.25% (standard grade)
- Ultra-low dropout typically: 200 mV at full load of 100 mA, 7 mV at 1 mA
- Low IQ: 600 µA typical at full load of 100 mA
- Shutdown current: 0.01 µA typical
- Low ZOUT over a wide frequency range
- High peak current capability

2.2.5 ATL431L

The ATL431 is a three-terminal adjustable shunt regulator with specified thermal stability over applicable automotive, commercial, and industrial temperature ranges. The output voltage can be set to any value between VREF (approximately 2.5 V) and 36 V with two external resistors. The regulator has a typical output impedance of 0.3 Ω. The operation current is as low as 100 µA (minimum), keeping the power loss at a quite low value.

2.2.6 ISO7710

The ISO7710 device is a high-performance, single-channel digital isolator with 5000-VRMS (DW package) and 3000-VRMS (D package) isolation ratings per UL 1577. This device is also certified by VDE, TUV, CSA, and CQC. The ISO7710 device provides high EMI and low emissions at a low power consumption while isolating CMOS or LVCMOS digital I/Os. The isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO2) insulation barrier. In the event of input power or signal loss, default output is high for a device without suffix F and low for a device with suffix F.

2.2.7 TPD1E0B04DPYR

The TPD1E0B04 is a bidirectional TVS ESD protection diode array for Thunderbolt™ 3 circuit protection. The TPD1E0B04 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

This device features a 0.13-pF IO capacitance per channel (DPL package) making it ideal for protecting high-speed interfaces up to 20 Gbps such as USB 3.1 Gen 2, Thunderbolt 3, and Antenna. The low dynamic resistance and low clamping voltage ensure system level protection against transient events.

The TPD1E0B04 is offered in the industry standard 0201 (DPL) and 0402 (DPY) packages.

2.2.8 CSD17575Q3A

The CSD17575Q3A is a 30-V NexFET™ Power MOSFET with a very low RDSon of 1.9 mΩ and a SON 3.3- mm×3.3-mm package. In this reference design, this device is used as a PD function switch for its low cost and RDSon.

2.2.9 LMC7111

The LMC7111 is a micropower CMOS operational amplifier available in the space-saving SOT-23 package. This makes the LMC7111 ideal for space and weight-critical designs. The wide common-mode input range makes it easy to design battery monitoring circuits which sense signals above the V+ supply. The main benefits of the tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, and portable computers. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

Key features for this device include:

- Tiny 5-pin SOT-23 package saves space
- Very wide common mode input range
- Specified at 2.7 V, 5 V, and 10 V
- Typical supply current 25 µA at 5 V
- 50 kHz gain-bandwidth at 5 V
- • Output to within 20 mV of supply rail at 100-kΩ load

2.3 System Design Theory

This reference design provides universal AC mains powered by 100-W output at 20 V and 5 A. The UCC28056 controls a PFC boost front end, while the UCC28780 active-clamp flyback converts the PFC output to an isolated 20 V and 5 A. The peak system efficiency is 93.4% with a 230-V_{AC} input at full load. In addition, several protections are embedded into this design which includes input under-voltage protection and output short circuit protection

Low EMI, high efficiency, high power factor and reliable power supply are the main focus of this design for targeted applications.

2.3.1 PFC Regulator Stage Design

Power factor correction (PFC) circuit shapes the input current of the power supply to maximize the real power available from the mains. In addition, it is important to have the PFC circuit comply with low total harmonic distortion (THD) regulatory requirements such as IEC61000-3-2. Currently, two modes of operation have been widely utilized for PFC implementations. For higher power circuits (> 300 W), the topology of choice is the boost converter operating in continuous conduction mode (CCM) and with average current mode control. For lower power applications (< 250 W), typically the transition mode (TM) or critical conduction mode (CrCM) boost topology is used.

For low power levels such as 100 W, TI recommends using the TM operation as it offers inherent zero-current switching of the boost diodes with no reverse-recovery losses, which permits the use of less expensive diodes without sacrificing efficiency. In addition, variable frequency operation results in distributed EMI spectrum and low emissions.

The design process and component selection for this design are illustrated in the following sections.

2.3.1.1 Circuit Component Design - Design Goal Parameters

表 2 elucidates the design goal parameters for a PFC converter design. These parameters will be used in further calculations for selection of components.

表 2. Design Goal Parameters for PFC Converter

PARAMETER	CONDITIONS	SPECIFICATIONS			UNITS
		MINIMUM	TYP	MAXIMUM	
INPUT CHARACTERISTICS					
Input voltage (VINAC)		100	230	240	V_{AC}
Frequency (fLINE)		47	50	63	Hz
Brown-in voltage			82		Hz
Brown-out voltage			77		Hz
OUTPUT CHARACTERISTICS					
Output voltage			390		V
Maximum output power				100	W
Efficiency			97.5		%
Minimum switching frequency		45			kHZ
Line regulation			1		%
Load regulation			1		%

2.3.1.2 Input Current Calculations and Fuse Selection

The input fuse and bridge rectifier are selected based upon the input current calculations. The boost voltage is designed to regulate at 390-V_{DC} for an input AC voltage range of 85- to 265-V_{AC} operation. The boost PFC converter is designed for output power of 110 W, considering the downstream DC-DC converter operating at more than 96% efficiency.

Determine PIN, the maximum input power averaged over the AC line period using 式 1.

$$P_{IN} = \frac{P_{DCBUS}}{\eta_{PFC}} = \frac{110}{0.975} = 112.8\ \text{W} \tag{1}$$

Determine the maximum average output current using 式 2.

$$I_{DCBUS(max)} = \frac{P_{DCBUS}}{V_{DCBUS(min)}} = \frac{110\ \text{W}}{390\ \text{VDC}} = 0.282\ \text{A} \tag{2}$$

Determine the maximum RMS input current using 式 3.

$$I_{IN\_RMS(max)} = \frac{P_{DCBUS}}{\eta_{PFC} \times V_{IN(min)} \times PF} = \frac{110\ \text{W}}{0.975 \times 85\ \text{VAC} \times 0.99} = 1.34\ \text{A} \tag{3}$$

Determine the maximum input current (IIN(max)), and the maximum average input current, (IIN_AVG(max)) based on the calculated RMS value, assuming the waveform is sinusoidal using 式 4 and 式 5 respectively.

$$I_{IN(max)} = \sqrt{2} \times I_{IN_{RMS(max)}} = \sqrt{2} \times 1.34 = 1.895\ \text{A} \tag{4}$$

$$I_{IN\_AVG(max)} = \frac{2}{\pi} \times I_{RMS(max)} = \frac{2}{\pi} \times 1.895 = 1.1\ \text{A} \tag{5}$$

2.3.1.3 Boost Inductor Design

For detailed derivation of equations, please refer to the *Detailed Design Procedure* section of the UCC28056 6-Pin Single-Phase Transition-Mode PFC Controller data sheet. Only the final equations are used to calculate the following values. The boost inductance value required to ensure that maximum load can be delivered from minimum line voltage may be expressed using 式 6.

$$I_{PFC0} = \frac{V_{inRMSMin}^{2}}{110\% \times P_{LdMax}} \times \frac{T_{ONMAX0}}{2} = 382\ \mu H \quad (6)$$

Lpfc = 375 uH

Maximum current in the power components will flow while delivering maximum load when supplied from minimum line voltage. In this condition, the UCC28056 always operates in transition mode (CRM).

Maximum boost inductor RMS current occurs at minimum line voltage and maximum input power.

$$I_{LPFCRMSMax} = \frac{2}{\sqrt{3}} \times \frac{110\% \times P_{LdMax}}{V_{LinRMSMin}} = 1.644\ A \quad (7)$$

Based on the inductor requirements in 式 7, a custom magnetic is designed: 375-uH and 4.5-A saturation current.

2.3.1.4 Boost Switch Selection

For detailed derivation of equations, please refer to the *Detailed Design Procedure* section of the UCC28056 6-Pin Single-Phase Transition-Mode PFC Controller data sheet . Only the final equations are used to calculate the following values.

Maximum RMS current in the switch occurs at maximum load and minimum line voltage.

$$I_{MosRMSMax} = \frac{110\% \times P_{LdMax}}{V_{LinRMSMin}} \times \sqrt{\frac{4}{3} - \frac{32 \times \sqrt{2} \times V_{InRMSMin}}{9 \times \pi \times V_{OUT}}} = 1.412\ A \quad (8)$$

MOSFET selection for the Boost switch can now be done under the following conditions:

- The voltage rating must be greater than the maximum output voltage. Under transient or line surge testing, the output voltage may rise well above its normal regulation level. For this design example, a MOSFET voltage rating of 600 V is chosen to support a regulated output voltage of 390 V.
- Based on an acceptable level of conduction loss in the MOSFET, the RDSON value required can be calculated from the maximum RMS current. For this example, design an IPD65R190C7 MOSFET, from Infineon was selected with RDSON at 25°C = 0.19 Ohms.
- For best efficiency, a MOSFET that incorporates a fast body diode should be used. Operating with discontinuous inductor current (DCM) from a low input voltage will incur additional switching power loss if a MOSFET with slow body diode is used.

2.3.1.5 Boost Diode Selection

For detailed derivation of equations, please refer to the *Detailed Design Procedure* section of the UCC28056 6-Pin Single-Phase Transition-Mode PFC Controller data sheet. Only the final equations are used to calculate the following values.

The maximum RMS current in the Boost diode occurs at maximum load and minimum Line.

$$I_{DioRMSMax} = \frac{4}{3} \times \frac{110\%\ P_{LdMax}}{V_{LinRMSMin}} \times \sqrt{\frac{2 \times \sqrt{2} \times V_{LinRMS}}{\pi \times V_{Out}}} = 0.841\ A \quad (9)$$

Conduction power loss in the Boost diode is primarily a function of the average output current.

$$I_{DioAVGMax} = \frac{P_{LdMax}}{V_{Out}} = 0.282\ \text{A} \quad (10)$$

Boost diode selection can now be made under the following conditions:

- The Boost diode requires the same voltage rating as the Boost MOSFET switch.
- The Boost diode must have average and RMS current ratings that are higher than the numbers calculated above.
- Diodes are available with a range of different speed and recovery charge. Fast diodes, with low reverse recovery charge, typically have higher forward voltage drop. Fast diodes will therefore have higher conduction loss but lower switching loss. Slow diodes, with high reverse recovery charge, typically have lower forward voltage drop. Slow diodes will therefore have lower conduction loss but higher switching loss. Maximum efficiency is achieved when the diode speed rating matches the application.

For this design, the MURS360 diode from Onsemi was selected. This diode has a voltage rating of 600 V and an average current rating of 4 A. This design has a forward voltage drop of around 0.85 V giving a conduction loss in the Boost diode of less than 0.24 W.

2.3.1.6 Output Capacitor Selection

The hold-up time is the main requirement in determining the output capacitance. ESR and the maximum RMS ripple current rating are also important, especially at higher power levels.

$$C_{OUT(min)} \geq \frac{2 \times P_{DCBUS} \times t_{holdup}}{\left(V_{DCBUS}^2 - V_{holdup}^2\right)} \quad (11)$$

The system needs to have 10 ms back-up for 80% of load (80 W).

The hold-up voltage is considered as 127 V for continuous operation of downstream DC/DC converter.

$$V_{holdup} = 127\ \text{V}$$

$$C_{OUT(min)} \geq \frac{2 \times 80\ \text{W} \times 10\ \text{ms}}{\left(390^2 - 127^2\right)} = 29.4\ \mu\text{F} \quad (12)$$

The actual value used in design is a 68-µF, 20%, 450-V capacitor.

2.3.1.7 Output Voltage Set Point

Select the divider ratio of RFB_{top} and RFB_{bottom} to set the VREF voltage to 2.5 V at the desired output voltage. The current through the divider is reduced to the minimum to keep the no-load power loss as small as possible. Consider the pull-up resistor RFB_{top} to be 10.052 MΩ.

Using the internal 2.5-V reference, VREF, the bottom divider resistor, RFB_{bottom}, is selected to meet the output voltage design goals.

$$R_{FBbottom} = \frac{V_{REF} \times R_{FBtop}}{V_{OUT} - V_{REF}} \quad (13)$$

$$R_{FB2} = \frac{2.5 \times 10.052\ \text{M}}{390 - 2.5} = 64.9\ \text{k} \quad (14)$$

A standard value 64.9-kΩ resistor for RFB2 results in a nominal output voltage set point of 390 V.

A small capacitor on VOSNS pin must be added to filter out noise. Limit the value of the filter capacitor such that the RC time constant is limited to approximately 100 µs so as not to significantly reduce the control response time to output voltage deviations.

$$C_{VOSNS} = \frac{150\ \mu}{R_{FBbottom}} = 2313\ \text{pH} \tag{15}$$

The closest standard value of 2200 pF was used on VOSNS pin.

2.3.2 ACF Converter Stage Design

ACF is a two-switch topology that achieves soft switching and recovers leakage inductance energy. Compared with traditional ACF in continuous conduction mode (CCM), ACF in critical conduction mode (CrCM) uses the magnetizing inductance instead of leakage inductance to store ZVS energy. As magnetizing inductance is much larger than leakage inductance, only a small amount of negative magnetizing current is required to achieve full ZVS soft switching. By controlling the amount of negative magnetizing current, ZVS can easily be achieved from zero to full load. With proper design, the output rectifier achieves zero current switching (ZCS) during turnoff. All of these features make ACF successful at high power density and efficiency adapter applications.

表 3. Design Goal Parameters for ACF Converter

PARAMETER	CONDITIONS	SPECIFICATION			UNITS
		MINIMUM	TYP	MAXIMUM	
INPUT CHARACTERISTICS					
Input voltage	VINDC	127	-	400	V
Line frequency		47	50	63	Hz
OUTPUT CHARACTERISTICS					
Output voltage		5		20	V
Maximum output power				100	W
Efficiency	for 20 V_{out}		95		%
Line regulation		-	1	-	%
Load regulation		-	5	-	%

2.3.2.1 Transformer Turns Ratio Calculation

The transformer that turns ratio is determined by the voltage rating of GaN and synchronous rectification MOSFET. The voltage stress of GaN NV6117 is 650 V and the SR MOSFET is a 150-V Si device. Therefore, the maximum and minimum turns ratio can be calculated separately using 式 16 and 式 17, respectively.

$$N_{PS\_max} = \frac{(1 - K_{dera}) \times V_{DS\_GaN} - V_{BULK\_max}}{V_{OUT\_max}} = 6 \tag{16}$$

Where,

• Kdera is the GaN voltage derating

• VDS_GaN is the maximum GaN drain-to-source voltage rating

• VBULK_max is the maximum bulk voltage

• VOUT_max is the maximum output voltage

$$N_{PS\_min} = \frac{V_{BULK\_max}}{(1-K_{dera}) \times V_{DS\_SR} - V_{OUT\_max} - V_{spike}} = 4.7 \quad (17)$$

Where,

• VDS_SR is the SR MOSFET drain-to-source voltage rating

• Vspike is the spike voltage on SR MOSFET

A larger turns ratio means a larger main switch duty cycle and smaller secondary RMS current. In this reference design, the turns ratio is designed as 5 to maintain the minimum secondary RMS current, which does better to the efficiency and thermal.

2.3.2.2 Primary Magnetic Inductance Calculation

After NPS is chosen, the primary magnetic inductance (Lm) can be determined based on the minimum switching frequency (fSW_min) at the minimum bulk voltage (VBULK_min), maximum duty cycle (Dmax), and maximum output power (POUT_max). When selecting the minimum switching, consider the impact on full-load efficiency and EMI filter design.

Calculate the maximum duty cycle and primary inductance using 式 18 and 式 19.

$$D_{max} = \frac{N_{PS} \times V_{OUT\_max}}{V_{BULK\_min} - N_{PS} \times V_{OUT\_max}} = 0.44 \quad (18)$$

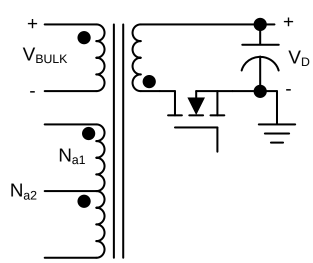
$$L_m = \frac{D_{max}^2 \times V_{BULK\_min}^2 \times \eta}{2 \times f_{SW\_min} \times P_{OUT\_max}} = 78\ \mu H \quad (19)$$

Finally, a custom magnetic is designed: 72-uH and 10-A saturation current

2.3.2.3 Auxiliary-to-Secondary Turn Ratio Design

The UCC28780 and both GaN devices are all powered by auxiliary winding at run mode. Two windings are designed to make sure that VDD will not be lower than the turnoff voltage and to minimize the power consumption. 図 2 shows the auxiliary power diagram.

図 2. Auxiliary Power Diagram



The Na1 winding is designed to power the devices at 5-V and 9-V outputs. Considering the voltage derating at a light load, there should be enough margin on VDD_min. Then at a 9-V output, the VDD is equal to the TVS diode voltage of 16 V. Na1 must stay a small value to decrease the power consumption on the transistor.

The Na2 winding is designed to power the devices at 15-V and 20-V outputs. Calculate the auxiliary-to-secondary turn ratio using 式 20 and 式 21.

$$\frac{N_{a1\_min}}{N_S} = \frac{1.5 \times V_{DD\_min}}{5} = 3.3 \quad (20)$$

$$\frac{N_{a2\_min}}{N_S} = \frac{1.5 \times V_{DD\_min}}{15} = 1.1 \tag{21}$$

2.3.2.4 Clamp Capacitor Calculation

Consider the design trade-off between conduction loss reduction and turnoff switching loss of the highside switching device (QH). A higher clamp capacitor (Cclamp) results in less RMS current flowing through the transformer windings and switching devices; therefore, the conduction loss can be reduced. However, a higher Cclamp design results in QH turning off before the clamp current returns to zero. The condition of non-ZCS increases the turnoff switching loss of QH. Therefore, Cclamp needs to be fine tuned based on the loss attribution. For best results, design the resonance between leakage inductance (Lk) and Cclamp to be completed by the time between resonant current is zero and QH is turned off. In this setup, the demagnetization time must be equal to around three quarters of the resonant period. Use 式 22, 式 23, and 式 24 to design Cclamp for obtaining ZCS at a minimum bulk voltage, minimum output voltage, and full load. A low-ESR clamp capacitor is required to minimize the conduction loss.

$$C_{clamp\_max} = \frac{1}{L_k} \times \left(\frac{L_k \times i_{m+}}{1.5\pi \times N_{PS} \times V_{OUT\_min}} \right)^2 \tag{22}$$

$$i_{m+} = \sqrt{\frac{2 \times P_{OUT\_max}}{\eta \times L_m \times f_{sw\_min}} + i_{m-}^{\ 2}} \tag{23}$$

$$i_{m-} = \sqrt{\frac{C_{SW}}{L_m}} \times V_{BULK\_min} \tag{24}$$

2.3.2.5 Bleed Resistor Calculation

A large bleed resistor (RBleed) is used to discharge clamp capacitor voltage to a residual voltage ($V_{residual}$) during the 1.44-s fault delay recovery time (tFDR). After the converter recovers from the fault mode, the lower $V_{residual}$ reduces the maximum current flowing through QH and SR within their respective safe operating areas, even if the output voltage is shorted. The target $V_{residual}$ can be calculated based on the maximum pulse current of QH or the SR current reflected to the primary side, depending on which is lower.

$$R_{Bleed} = \frac{t_{FDR}}{C_{clamp} \times \ln\left(\frac{N_{PS} \times V_{OUT\_max}}{V_{residual}} \right)} \tag{25}$$

2.3.2.6 Output Capacitor Calculation

Output capacitance (COUT) is determined by evaluating several factors and choosing the largest of the results.

1. The minimum output capacitor value must be enough to meet transient specification of output voltage due to a given load step until the voltage-control loop can respond to restore regulation. Where:
   - ΔIload is maximum load-step magnitude for transient response
   - ΔVtrans_max is the maximum transient voltage deviation for transient response
   - Δttrans is the transient response time
2. The maximum ESR of output capacitor is often limited by the maximum output peak-to-peak voltage ripple (Vpk-pk), where the worst-case output ripple is considered at maximum load (IOUT_max). If the high-frequency switching ripple at the output is mainly dominated by the ESR ripple, a sinusoidal approximation of the secondary current waveform of the ACF is made to calculate the ESR requirement based on the target output ripple specification.

$$V_{residual} = \min\left(i_{max\_QH,}\ i_{max\_SR}\right) \times \sqrt{\frac{L_k}{C_{clamp}}} \tag{26}$$

$$C_{OUT\_min} = \frac{\Delta I_{load} \times \Delta t_{trans}}{\Delta V_{trans\_max}} \tag{27}$$

$$R_{Co\_max} = \frac{2 \times \left(1 - D_{max} - f_{sw\_min} \times \pi \times \sqrt{L_k \times C_{SW}}\right) \times V_{pk-pk}}{\pi \times I_{OUT\_max}} \tag{28}$$

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

- Isolated AC source
- Single-phase power analyzer
- Digital oscilloscope
- Multi-meters
- Electronic load

3.2 Testing and Results

3.2.1 Test Setup

1. Connect input terminals of the reference board to the AC power source.
2. Connect output terminals to the PMP20413 input terminals.
3. Connect the PMP20413 output terminals to electronic load, maintaining correct polarity.
4. Set a minimum load of about 0 A and minimum voltage of 25 V.
5. Gradually increase the input voltage from 0 V to turn on voltage of 84-V AC.
6. Observe that the output voltage across the load terminals has risen to about 5 V.
7. Increase the load to maximum load smoothly and observe the switching waveforms.
8. Select different output voltages through the PMP20413 device.
9. Increase the load to maximum load smoothly and observe the switching waveforms.
10. Compare these results with those presented in the design guide.

3.2.2 Test Results

3.2.2.1 Efficiency Performance

表 4 through 表 11 list the efficiency data of the different voltages.

表 4. 5 V at 115-V AC/60 Hz

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY (%)
5.03	0.5	3.23	77.86
5.03	1	6.2	81.13
5.02	1.25	7.9	79.43
5.02	1.5	9.3	80.97
5.02	2	11.8	85.08
5.03	2.5	14.1	89.18
5.02	3	16.6	90.72
5.03	3.5	19.4	90.75
5.03	3.75	20.8	90.69
5.02	4	22.2	90.45
5.02	4.5	25.3	89.29
5	5	28.2	88.65

表 5. 5 V at 230-V AC/50 Hz

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY (%)
5.03	0.5	3.43	73.32
5.03	1	6.34	79.34
5.02	1.25	8.15	76.99
5.02	1.5	9.6	78.44
5.02	2	12.1	82.98
5.03	2.5	14.41	87.27
5.02	3	16.98	88.69
5.03	3.5	19.73	89.23
5.03	3.75	21.37	88.27
5.02	4	22.72	88.38
5.02	4.5	25.74	87.76

表 5. 5 V at 230-V AC/50 Hz (continued)

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY (%)
5	5	28.51	87.69

表 6. 9 V at 115-V AC/60 Hz

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY (%)
9.02	0.5	5.5	82.00
9.02	1	10.2	88.43
9.02	1.25	12.6	89.48
9.02	1.5	15	90.20
9.02	2	19.8	91.11
9.02	2.5	24.3	92.80
9.02	3	29.1	92.99
9.02	3.5	34	92.85
9.02	3.75	36.4	92.93
9.02	4	38.9	92.75
8.97	4.5	43.8	92.16
8.92	5	48.6	91.77

表 7. 9 V at 230-V AC/50 Hz

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY (%)
9.02	0.5	5.7	79.12
9.02	1	10.7	84.30
9.02	1.25	13	86.73
9.02	1.5	15.8	85.63
9.02	2	19.9	90.65
9.02	2.5	24.5	92.04
9.02	3	29.2	92.67
9.02	3.5	34	92.85
9.02	3.75	36.4	92.93
9.02	4	38.7	93.23
9.02	4.5	43.4	93.53
8.86	5	48.4	91.53

表 8. 15 V at 115-V AC/60 Hz

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY (%)
14.94	0.5	9.83	75.99
14.94	1	18.17	82.22
14.94	1.25	22.14	84.35
14.93	1.5	26.1	85.80
14.93	2	34.27	87.13
14.93	2.5	41.8	89.29
14.93	3	49.43	90.61
14.93	3.5	57.23	91.31
14.93	3.75	61.2	91.48
14.93	4	65.14	91.68
14.87	4.5	72.77	91.95

表 8. 15 V at 115-V AC/60 Hz (continued)

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY (%)
14.74	5	80	92.13

表 9. 15 V at 230-V AC/50 Hz

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY (%)
14.94	0.5	9.57	78.06
14.94	1	17.72	84.31
14.94	1.25	21.64	86.30
14.93	1.5	25.55	87.65
14.93	2	33.7	88.61
14.93	2.5	41.2	90.59
14.93	3	48.8	91.78
14.93	3.5	56.6	92.32
14.93	3.75	60.6	92.39
14.93	4	64.5	92.59
14.87	4.5	72	92.94
14.75	5	79.4	92.88

表 10. 20 V at 115-V AC/60 Hz

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY (%)
19.87	0.5	12.4	80.12
19.82	1	23.5	84.34
19.82	1.25	28.9	85.73
19.82	1.5	34.35	86.55
19.81	2	45	88.04
19.81	2.5	55.2	89.72
19.88	3	65.47	91.10
19.83	3.5	75.7	91.68
19.81	3.75	80.9	91.83
19.82	4	86.14	92.04
19.82	4.5	96.29	92.63
19.83	5	107.2	92.49

表 11. 20 V at 230-V AC/50 Hz

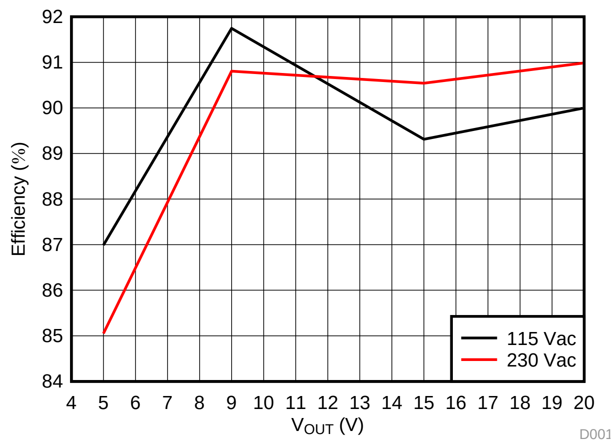
OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY (%)
19.82	0.5	12.13	81.70
19.82	1	22.93	86.44
19.82	1.25	28.4	87.24
19.82	1.5	33.8	87.96
19.81	2	44.4	89.23
19.82	2.5	54.6	90.75
19.81	3	64.9	91.57
19.81	3.5	75.23	92.16
19.82	3.75	80.3	92.56
19.83	4	85.5	92.77
19.81	4.5	95.65	93.20

表 11. 20 V at 230-V AC/50 Hz (continued)

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY (%)
19.82	5	106.1	93.4

図 3 shows the efficiency curves.

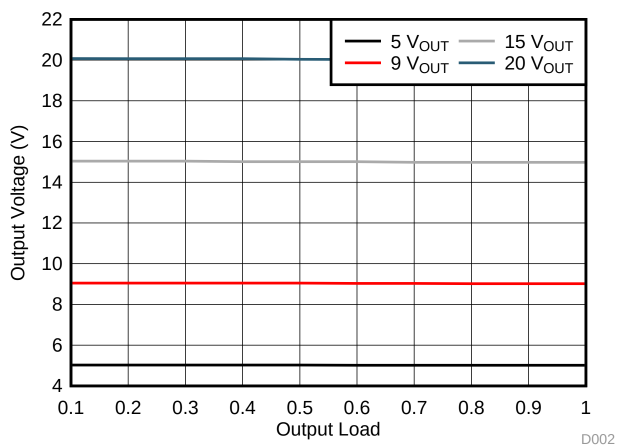
図 3. Average Efficiency Curve



3.2.2.2 *Load Regulation*

図 4 shows the load regulation at 115-V AC/60 Hz.

図 4. Load Regulation



3.2.2.3 Output Voltage Transitions

3.2.2.3.1 Start-up

注: CH1: Output Voltage; CH4: Input Voltage

図 5. Start-up Waveform at 115-V AC and 5-V/5-A Output

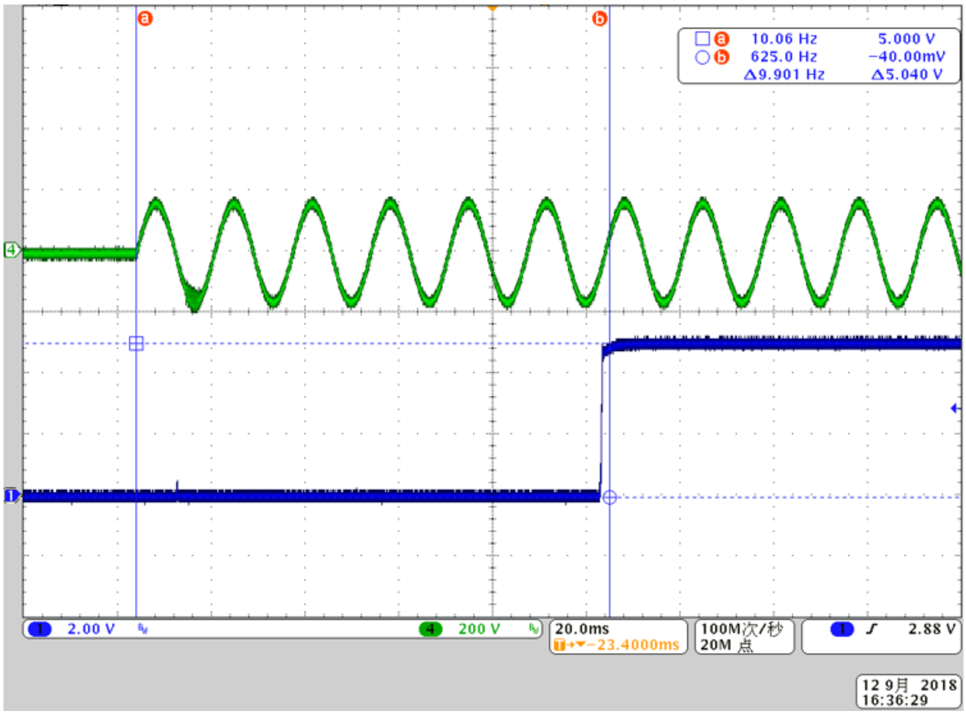
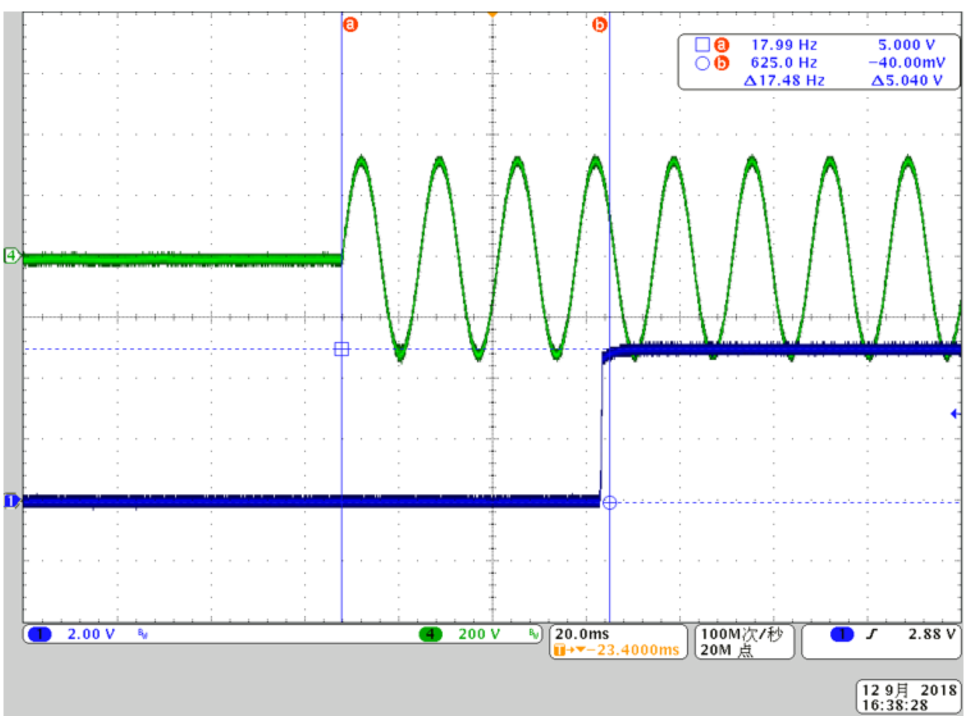


図 6. Start-up Waveform at 230-V AC and 5-V/5-A Output



3.2.2.3.2 Internal Waveform

3.2.2.3.2.1 PFC Stage Switching Waveforms

This section shows the PFC stage switching waveforms at input voltage 115 VAC and 230 VAC at different load conditions

注: CH3: PFC inductor current; CH4: PFC switch node voltage

図 7. SW-PFC-115VAC at Half-load

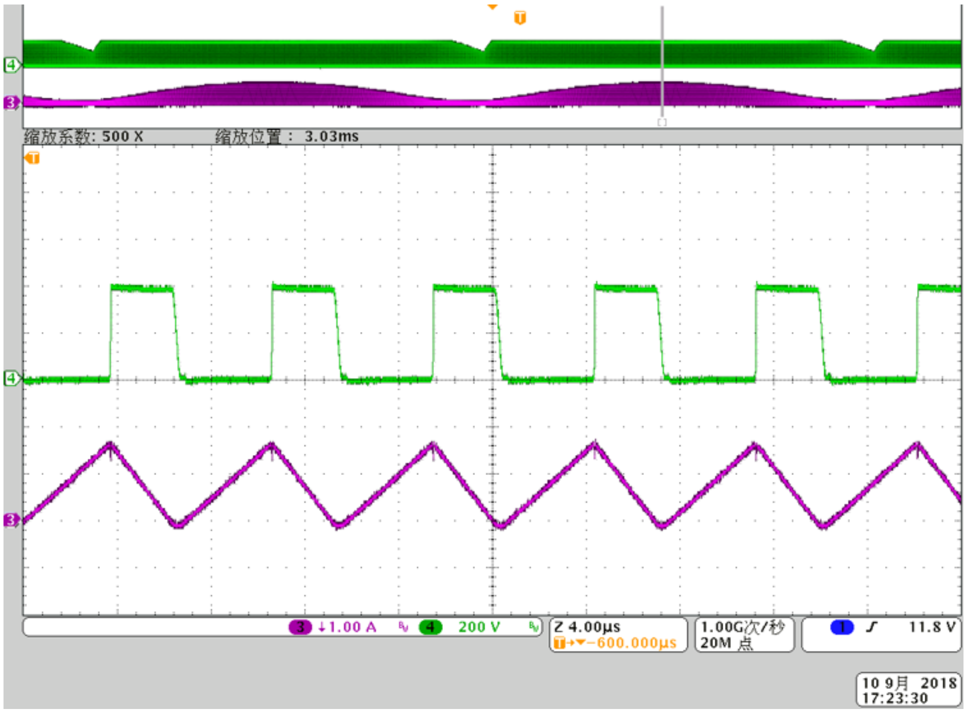


図 8. PFC-115 VAC at Full-load

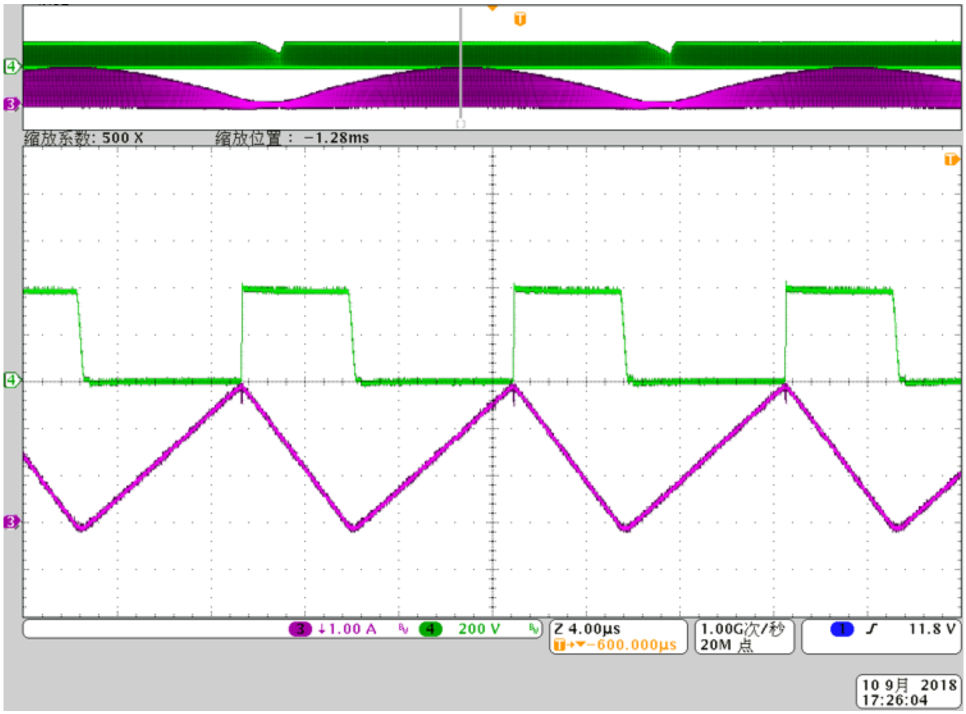


図 9. SW-PFC-230 VAC at Half-load

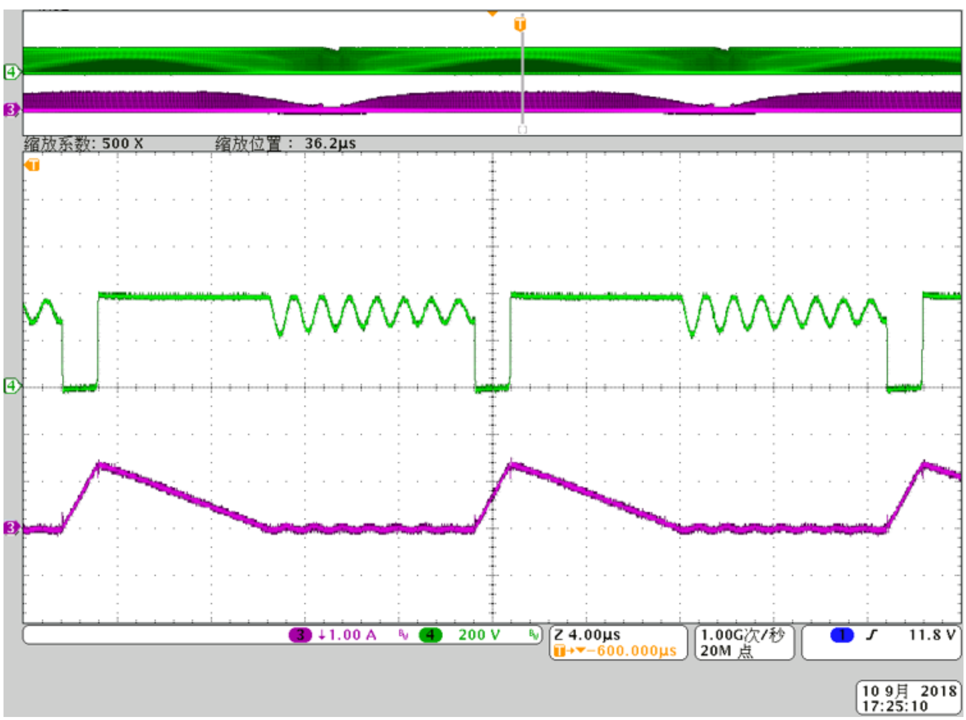
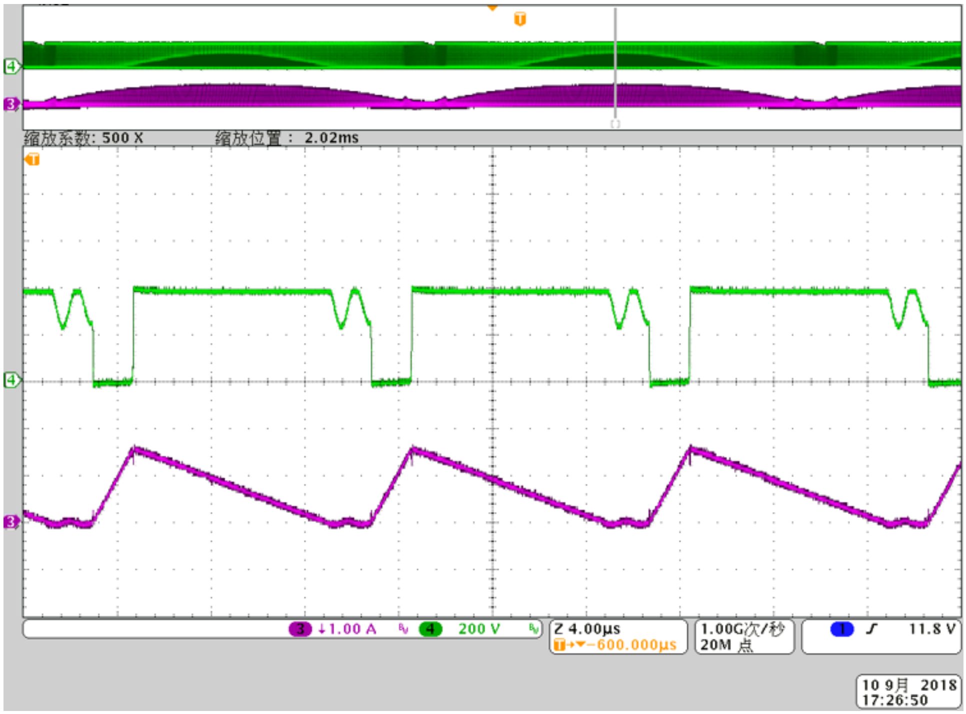


図 10. SW-PFC-230 VAC at Full-load



3.2.2.3.2.2 ACF Stage Switching Waveforms

This section shows the ACF stage switching waveforms at an input voltage of 115 VAC an 20 V_{out} at different load conditions.

注: CH3: ACF transformer primary current; CH4: ACF switching node voltage

図 11. SW-ACF-115 VAC, 20 V_{out}, 1.25 A

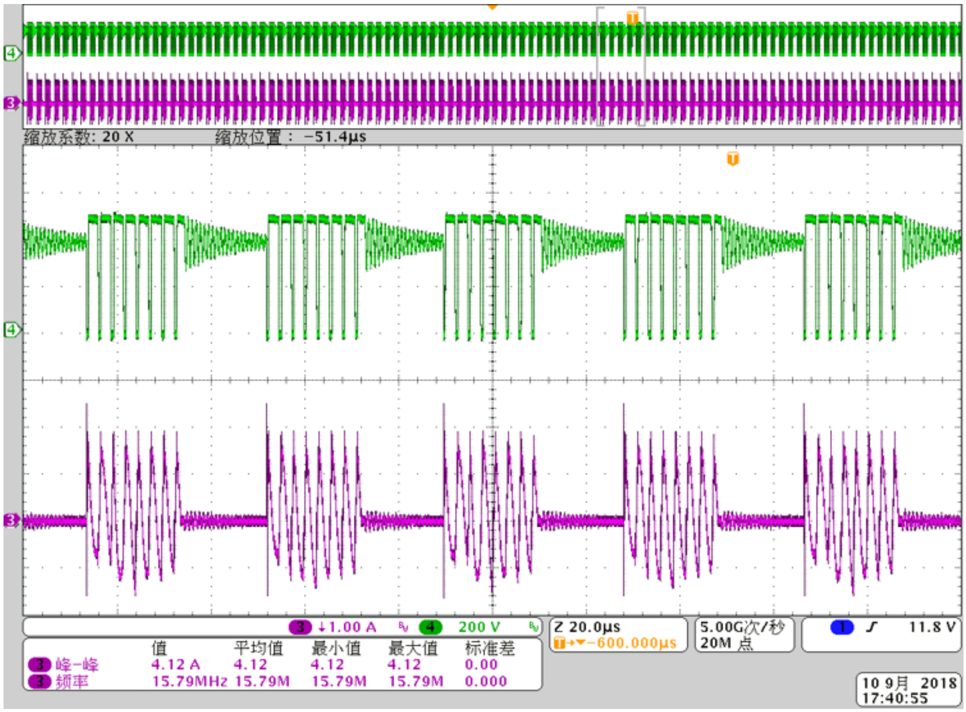


図 12. SW-ACF-115 VAC, 20 V_{out}, 2.5 A

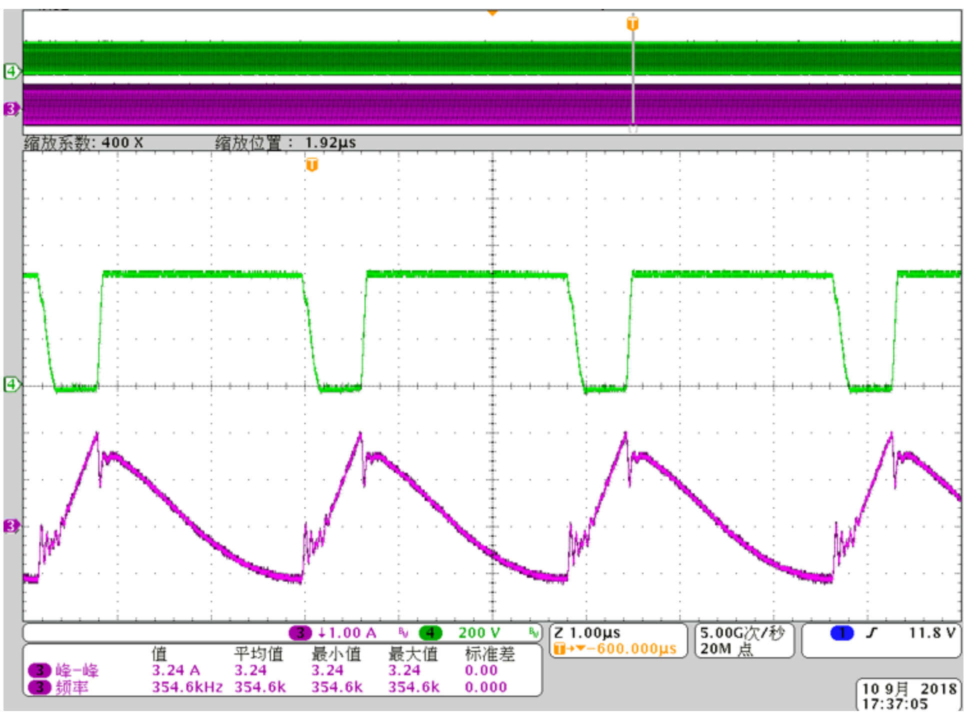


図 13. SW-ACF-115 VAC, 20 V_{out}, 3.75 A

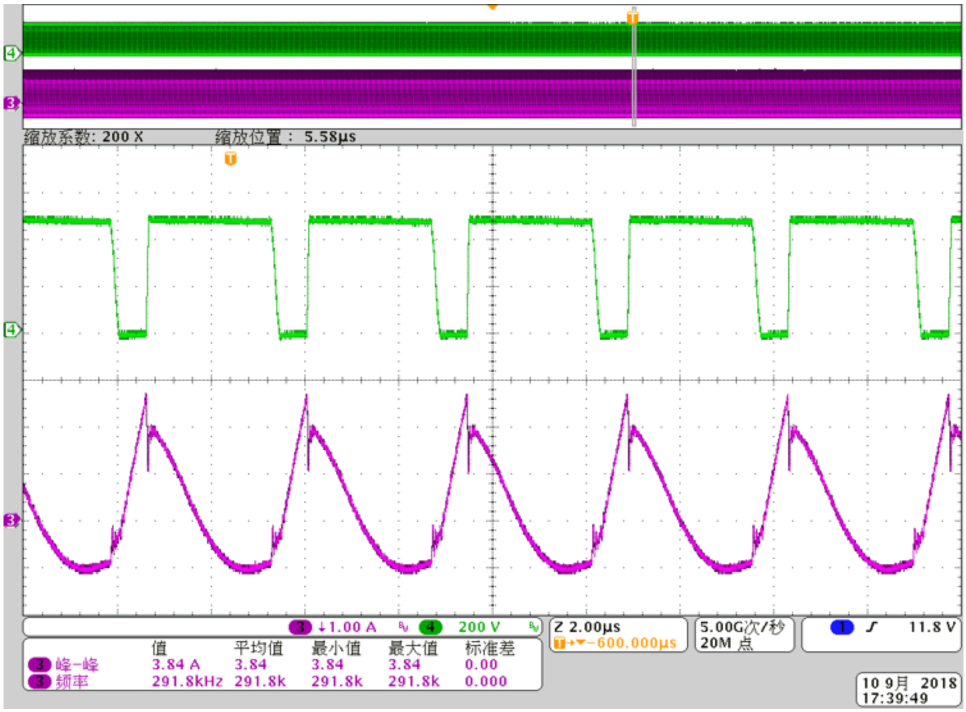
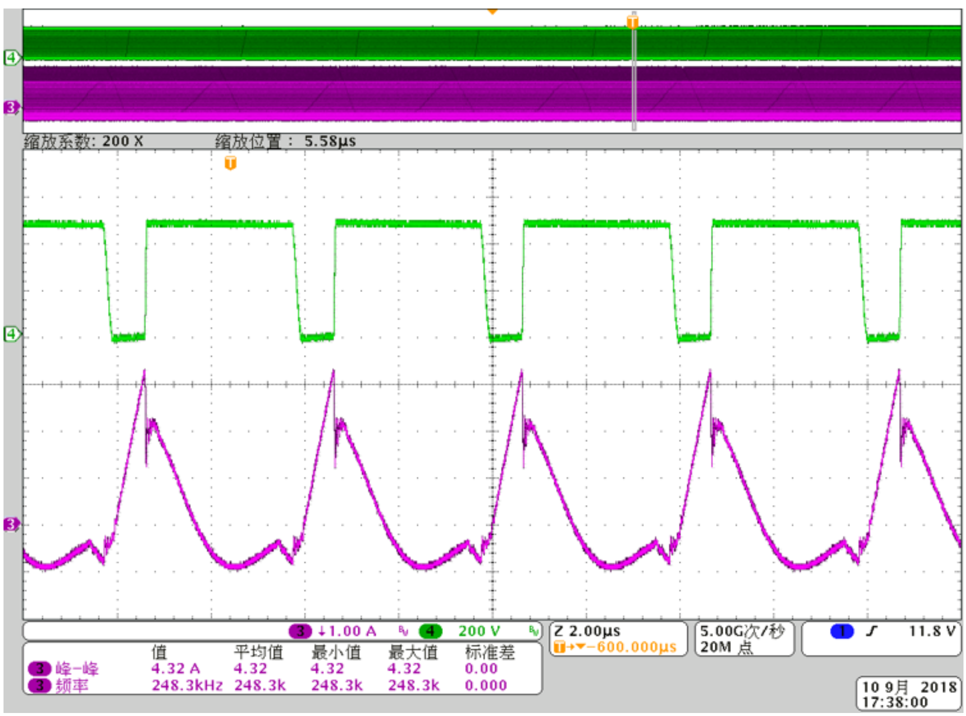


図 14. SW-ACF-115 VAC, 20 V_{out}, 5 A



3.2.2.4 Output Voltage Ripple

図 15. 115-V AC/60-Hz Input, 5-V/2.5-A Output

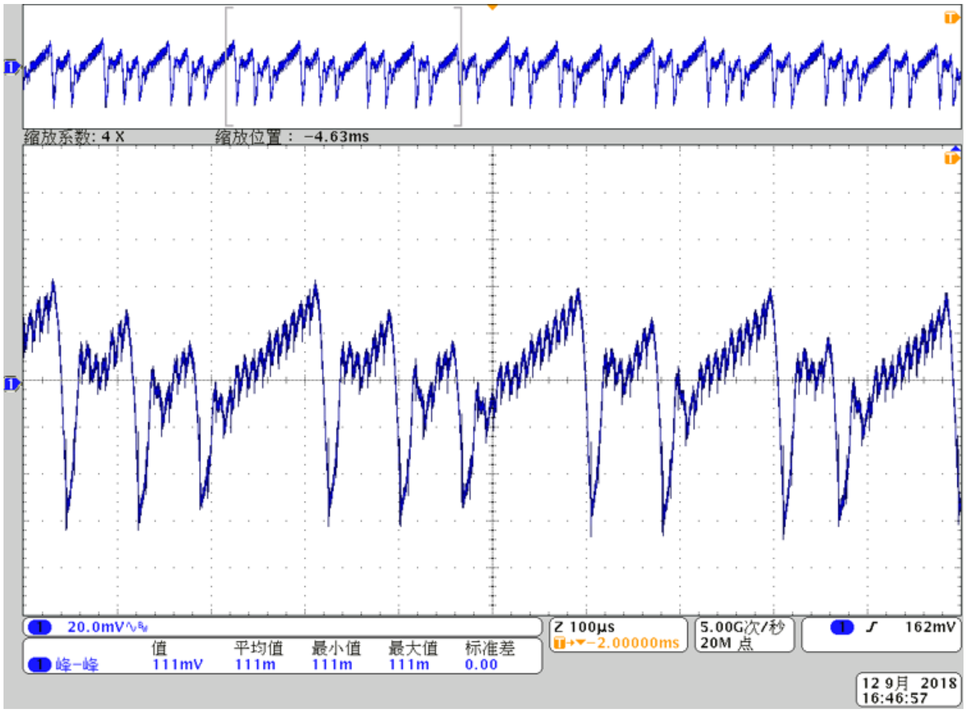


図 16. 115-V AC/60-Hz Input, 5-V/5-A Output

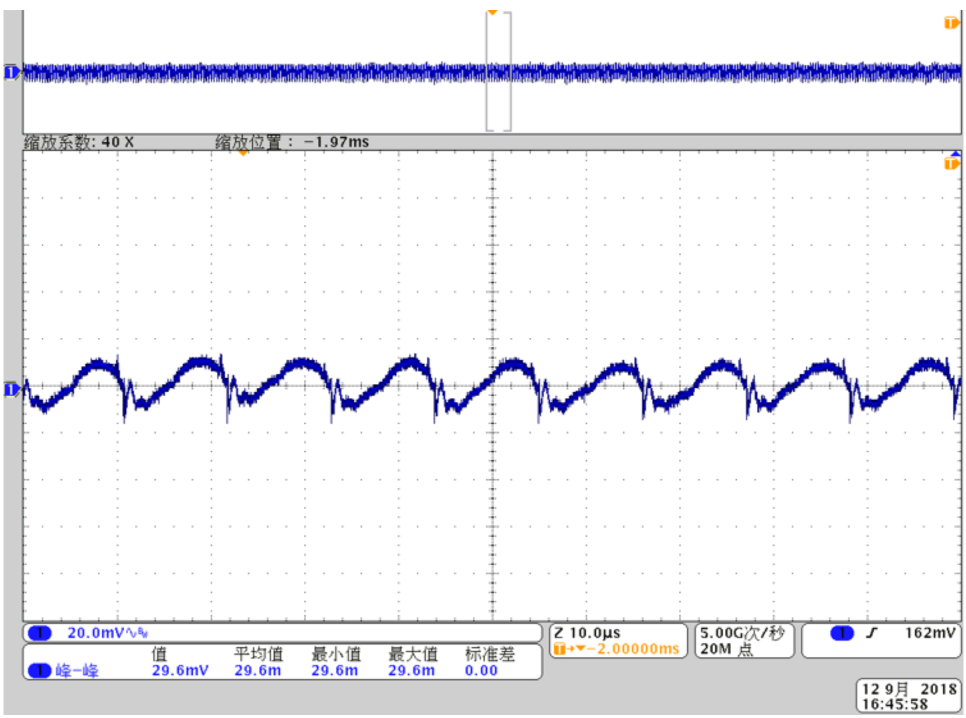


図 17. 115-V AC/60-Hz Input, 20-V/2.5-A Output

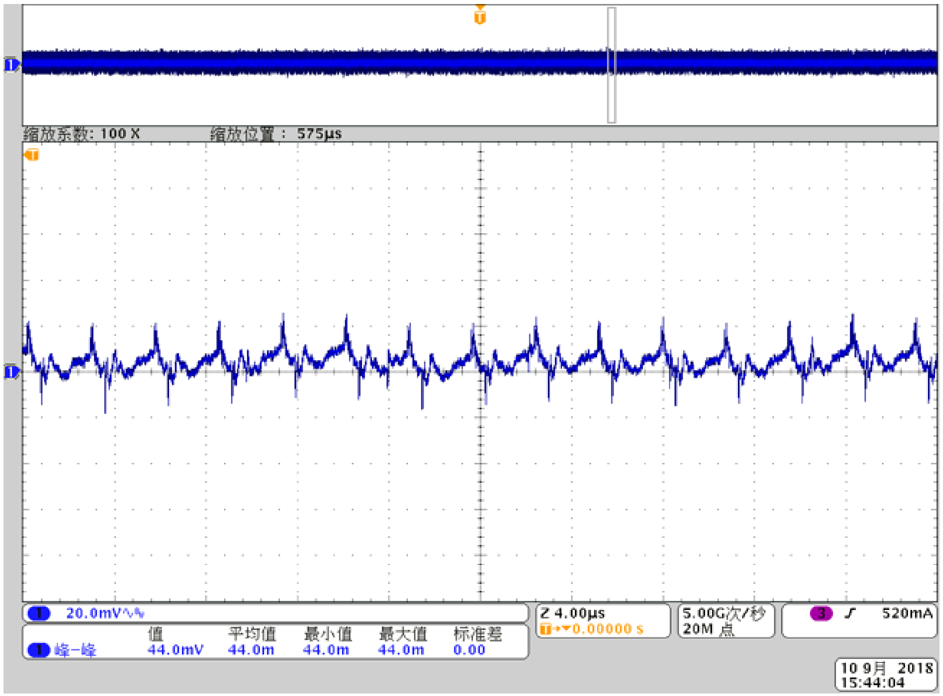
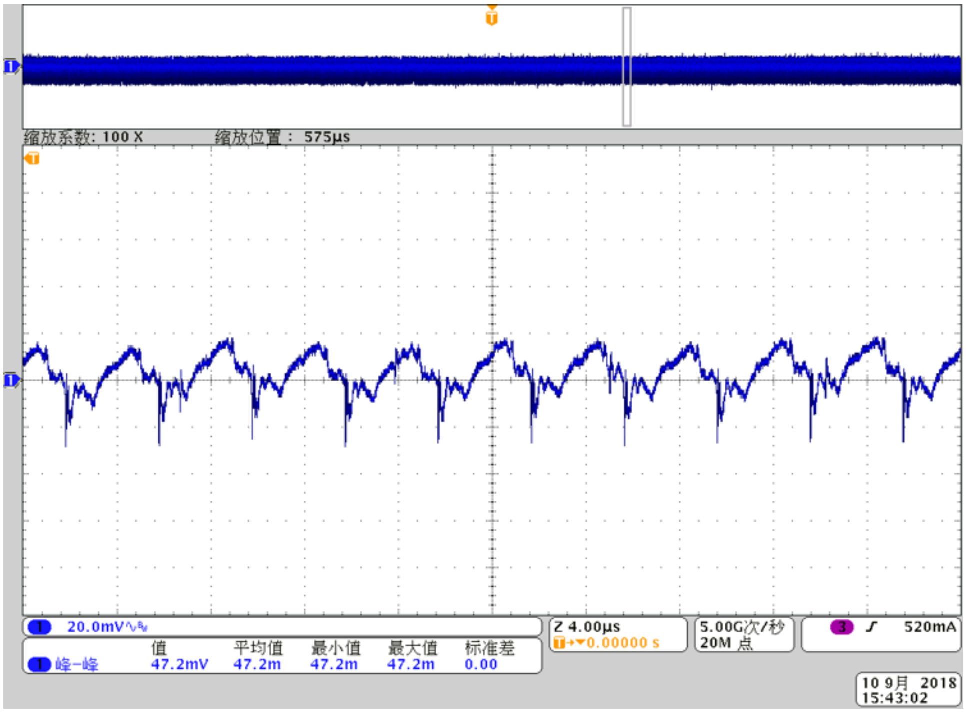


図 18. 115-V AC/60-Hz Input, 20-V/5-A Output



4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01623.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01623.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01623.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01623.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01623.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01623.

5 Related Documentation

1. Texas Instruments, *UCC28056 6-Pin Single-Phase Transition-Mode PFC Controller data sheet*
2. Texas Instruments, *UCC28780 High Frequency Active Clamp Flyback Controller data sheet*
3. Texas Instruments, *UCC24612 High Frequency Synchronous Rectifier Controller data sheet*
4. Texas Instruments, *30-W/in^3 , 94% Efficiency, 65-W USB Type-C ™ PD AC/DC Adapter Reference Design*

5.1 商標

E2E, NexFET are trademarks of Texas Instruments.
Thunderbolt is a trademark of Intel Corporation.
すべての商標および登録商標はそれぞれの所有者に帰属します。

5.2 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年**11**月発行のものから更新 **Page**

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265