

デザイン・ガイド: TIDA-01041

多相、高精度、0.5~100A のバッテリー構成に対応するバッテリー・テストのリファレンス・デザイン



概要

このリファレンス・デザインは、幅広い電流バッテリー・テスト用途に対応する多相ソリューションを実現します。LM5170 の 2 相昇降圧コントローラ・デジタイズ構成により、100A の充放電レートを達成可能です。また、高精度の定電流 (CC) / 定電圧 (CV) 較正ループにより、最高 0.01% の電圧制御精度を達成できます。主要な設計理論をすべて説明し、部品の選択プロセスや最適化についての指針も示しています。

リソース

- TIDA-01041
- LM5170-Q1
- INA828
- DAC80004
- ADS131A04


- デザイン・フォルダ
- プロダクト・フォルダ
- プロダクト・フォルダ
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- プロダクト・フォルダ

特長

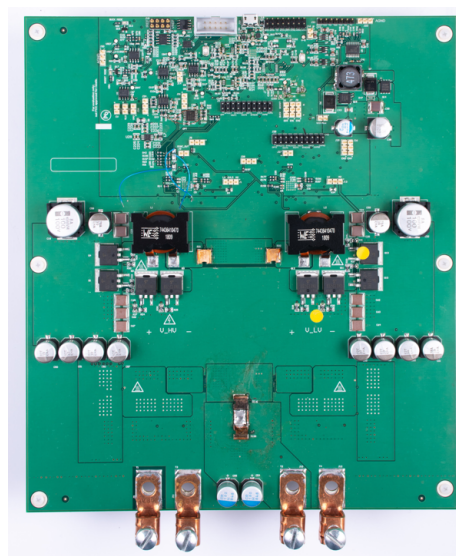
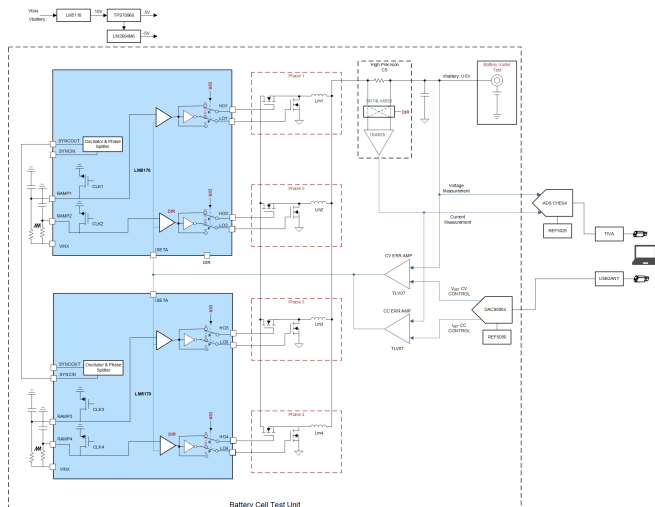
- 高精度の較正制御により 0.02% フルスケールの電流制御精度と 0.01% フルスケールの電圧制御精度を達成
- 0.5A~100A の充放電に対応
- 8V~16V の入力電圧 (バス) と、0V~4.2V (最大 5V) の出力負荷 (バッテリー)
- 充放電のために LM5170 多相双方向昇降圧型統合コントローラ/ドライバを 2 個使用

アプリケーション

- [バッテリー・テスト機器](#)



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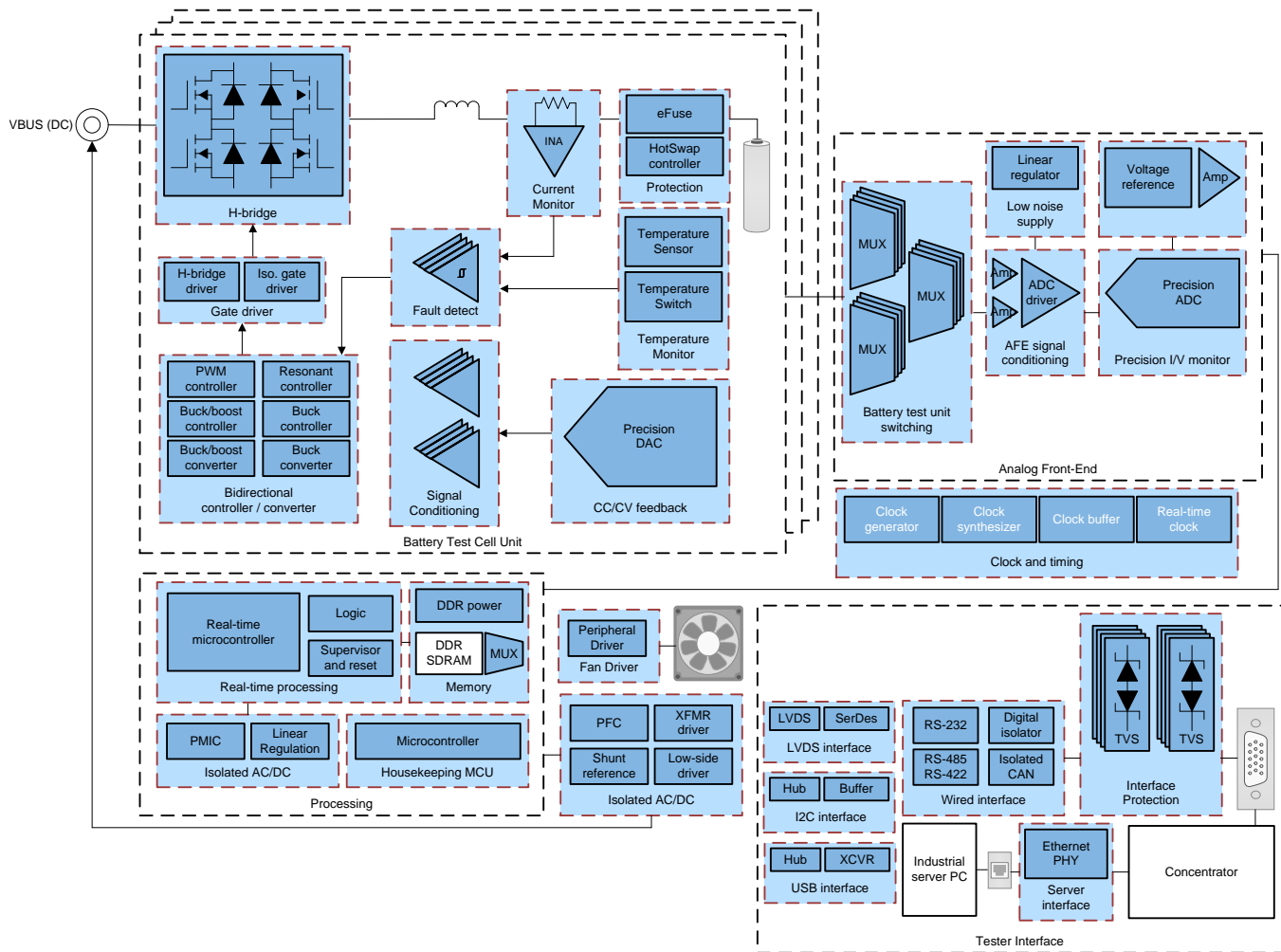


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1 System Description

Battery testers include high performing battery manufacturing equipment and laboratory test instruments, circuit control and data acquisition tools, battery simulation and manufacturing automation tools, appropriate to all battery applications and chemistries.

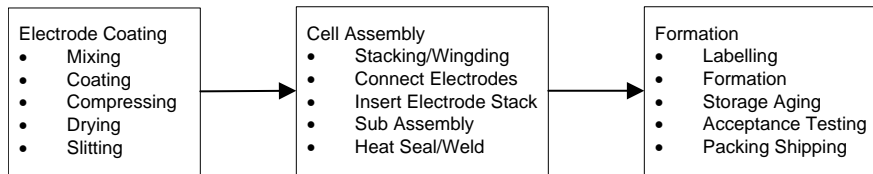
図 1. Battery Tester Block Diagram



1.1 Li-Ion Formation

Figure 2 shows the manufacturing process for the Li-Ion battery, a popular, rechargeable battery chemistry. A battery test is involved in the final part of the manufacturing process: Formation.

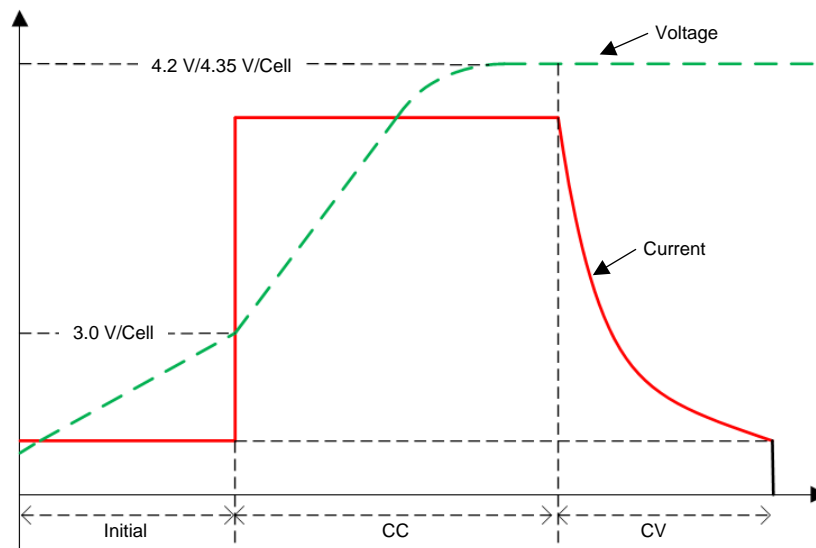
Figure 2. Simplified Li-Ion Battery Manufacturing Process



1.2 Li-Ion Battery Formation Profile

Figure 3 shows the typical Li-Ion battery formation profile, detailing the phases of the initial charging and formation of a battery which directly affects its quality and capacity for the entirety of the life span of the battery. In the first phase, labeled "Initial," a small initial charge of around 10% of the full-charge current is applied. This is done to prevent the cell from overheating and is done until the battery is able to accept the full current of the constant-current phase. During the constant-current, or "CC" phase, the battery is typically charged at 1 A or less until the battery voltage reaches 4.1 V or 4.2 V (depending on electrochemistry) where it then transitions to the constant voltage, or "CV" phase. For detailed test results on the transformation between CC and CV, see 3.1.4.3.

Figure 3. Regular Li-Ion Battery Formation Profile



For more information on Li-Ion battery formation, see the [TIDA-01040 Battery Tester Reference Design for High Current Applications](#) design guide.

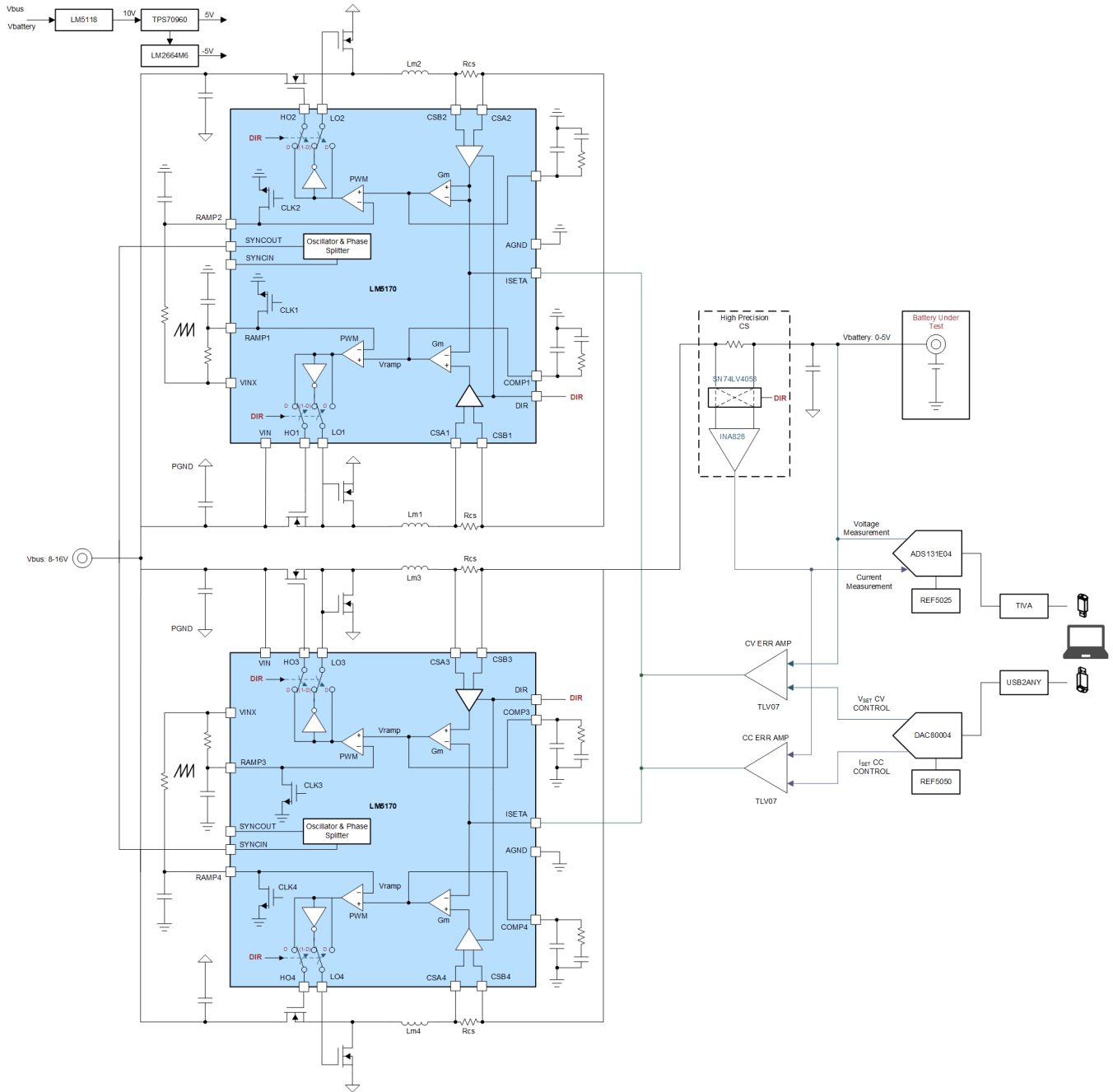
2 System Overview

This design encompasses the *Battery Test Cell Unit* and analog front end subsystems as [Figure 1](#) shows. In the following subsections, the system and its design theory are detailed.

2.1 Block Diagram

In this reference design, the LM5170 device is a multiphase, buck-boost bidirectional controller that is able to charge or discharge the load at up to 50 A each depending on the "DIR" setting. The DAC80004 device is a 16-bit DAC that sets the reference current and reference voltage for either CC or CV mode using the USB2ANY interface. The high-precision INA188 current sense amplifier measures the current charging or discharging the load. That measurement is compared with the reference control signal using the TLV07 op amp. The load voltage is compared with the reference control signal using the LM6142 op amp. The system is using two OPA827 devices to buffer the current measurement and voltage measurement signals before the data acquisition phase and the THS4561 differential amplifier converts the single-ended measurement signals to differential signals. The ADS131A04 device is a 24-bit delta-sigma ADC used to monitor the current and voltage of the load. An onboard TIVA processor is used to communicate between the ADS131A04 device and the PC for this reference design. When the system is set to CC or CV mode, the multiphase controller will output the signified voltage or current to the load. The system monitors and controls the output at the load to ensure precision while the user can monitor the results through the acquired data.

図 4. TIDA-01041 Block Diagram



2.2 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
$V_{\text{battery_min}}$	0 V	Battery-port minimum operating voltage
$V_{\text{battery_nominal}}$	4.2 V	Battery-port normal operating voltage
$V_{\text{battery_max}}$	5 V	Battery-port maximum operating voltage
$V_{\text{bus_min}}$	8 V	Bus-port minimum operating voltage
$V_{\text{bus_nominal}}$	12 V	Bus-port normal operating voltage
$V_{\text{bus_max}}$	16 V	Bus-port normal operating voltage
F_{SW}	100 kHz	Switching frequency
$I_{\text{ph_max}}$	25 A	Maximum DC current per phase, bidirectional
$I_{\text{Total_max}}$	100 A	Total maximum DC current at battery-port
Current control accuracy	0.02%	Full-scale current control accuracy for charge and discharge
Voltage control accuracy	0.01%	Full-scale current control accuracy for charge and discharge

For detailed test results on current control accuracy, refer to [3.1.4.1](#)

For detailed test results on voltage control accuracy, refer to [3.1.4.2](#)

2.3 Design Considerations

This reference design must test at charge and discharge rates of up to 100-A continuous for larger capacity batteries. The following makes this possible:

- Multiphase design, eliminating the need for larger, more expensive power stage inductors needed to draw the same amount of current with a single phase.
- To maximize battery performance however, the constant current and voltage control systems must be designed to an accuracy range within $\pm 0.05\%$. The next section takes a deeper dive into the need for multiphase in this design.

Inductor currents for each conductor are charging and discharging the output capacitor of the design concurrently depending on whether or not a given phase is active. This produces one overall current whose AC portion is absorbed by the output capacitor, resulting in a lower overall voltage ripple. As the number of phases increase, the current and voltage output ripple decreases.

2.3.1 MultiPhase Design

Multiphase converters use multiple inductors operating in parallel to operate beyond the saturation current rating of a single inductor and require less RMS current from the input capacitor; thereby, reducing the solution size and cost. See the [Multiphase buck design from start to finish \(part 1\) application report](#) for more details.

TI recommends selecting an inductor such that its peak-to-peak ripple current is less than 80% of the channel inductor full load DC current. Therefore, the inductor should satisfy:

$$L_m \geq \frac{V_{L,reg} \times (1 - D_{BK,min})}{80\% \times I_{max} \times F_{sw}} = \frac{4V \times (1 - 0.2)}{0.8 \times 25A \times 100kHz} = 1.6\mu H \tag{1}$$

This design uses 4.7- μ H inductors to further decrease current ripple. Multiphase converters parallel multiple inductors to draw currents that would be problematic for a single-phase converter due to current saturation limitations. Multiphase reduces input RMS current and output ripple current, allowing the design to employ smaller value inductors and reduce the size of the design. The ability to have inductors rated for lower current also decreases the system cost.

図 5. Normalized Input Capacitance RMS Current

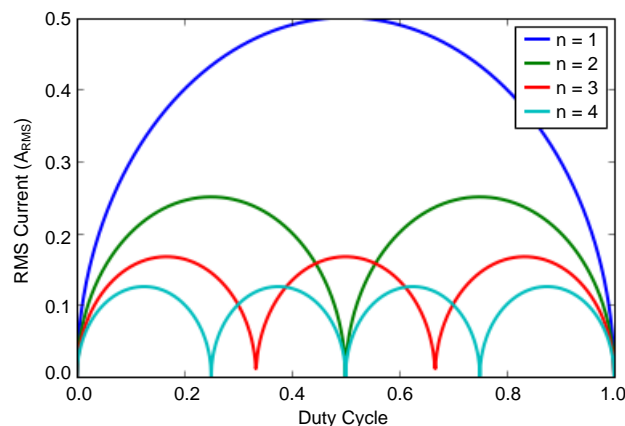
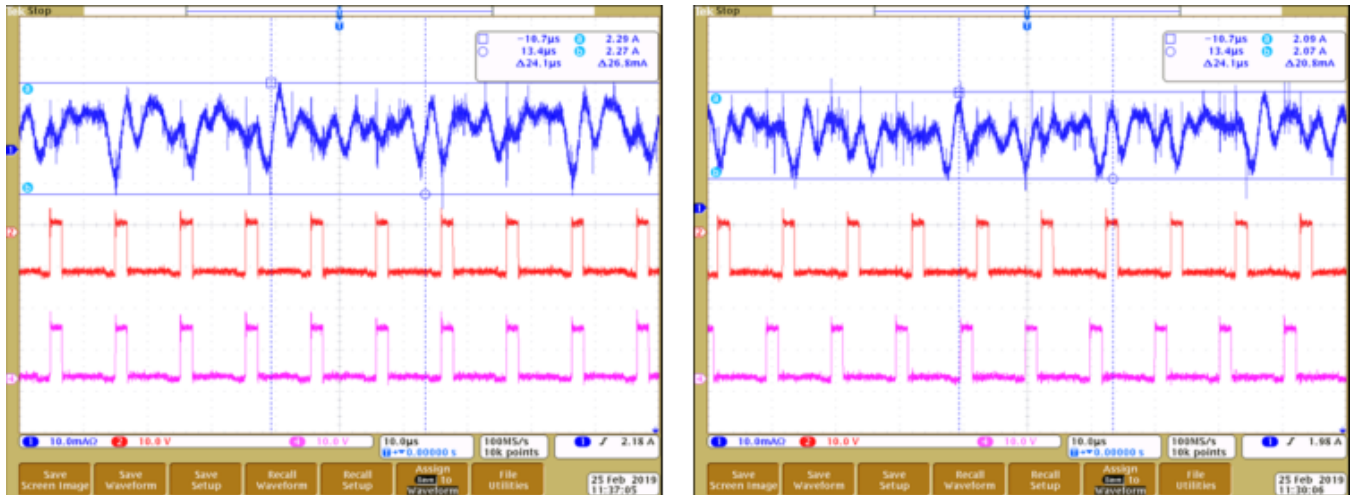


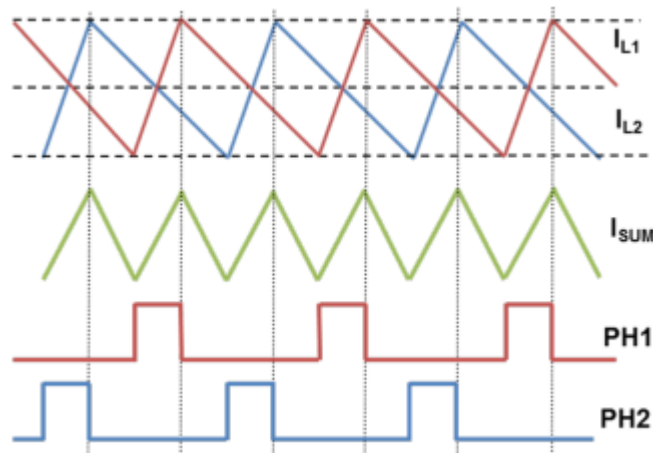
図 6. Single Phase vs Multiphase Input Ripple Current



Inductor currents at each of the four power stages of the design sum to charge and discharge its output capacitor concurrently, depending on whether or not a given phase is active. This produces one overall current, I_{sum} , whose AC portion is absorbed by the output capacitor, resulting in a lower overall voltage ripple.

図 7 shows the effect of a dual-phase system on voltage ripple. As the number of phases increase, the current and output ripple decrease.

図 7. Dual-Phase Converter Ripple Cancellation



Four phases of current allow the TIDA-01041 design to charge and discharge at up to 100 A. This is achieved by daisy chaining two LM5170 devices, each with two phases, into a multiphase configuration.

図 10 shows a block diagram of this configuration.

図 8. Four Phases Interchangeable Waveform

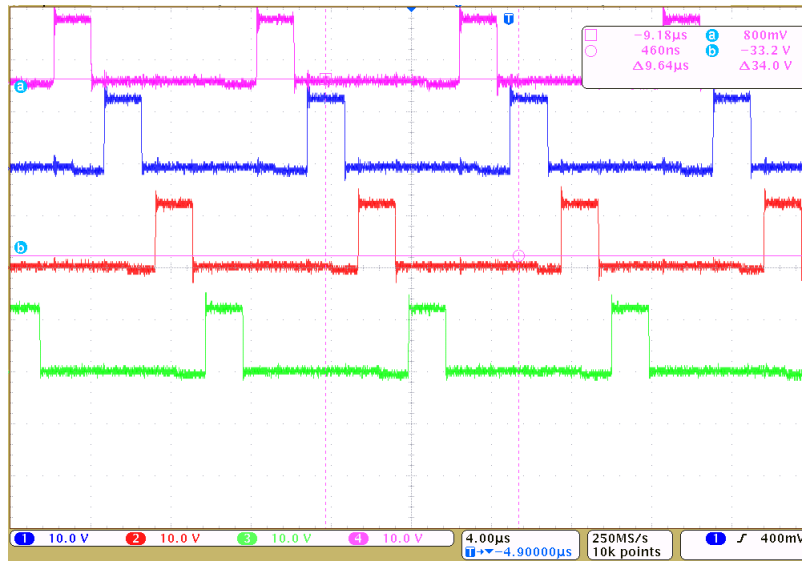
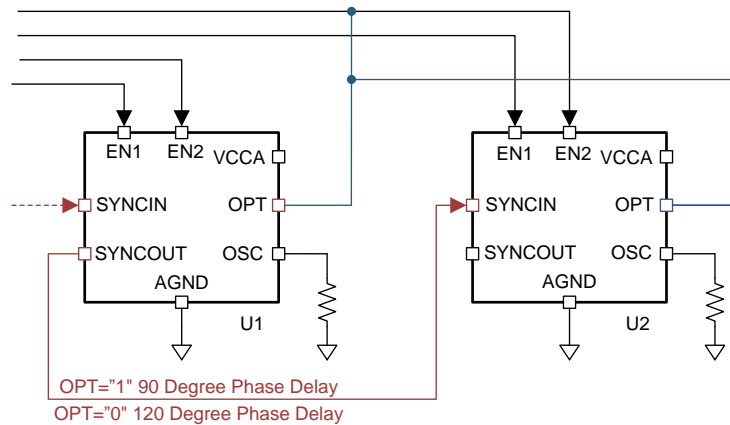
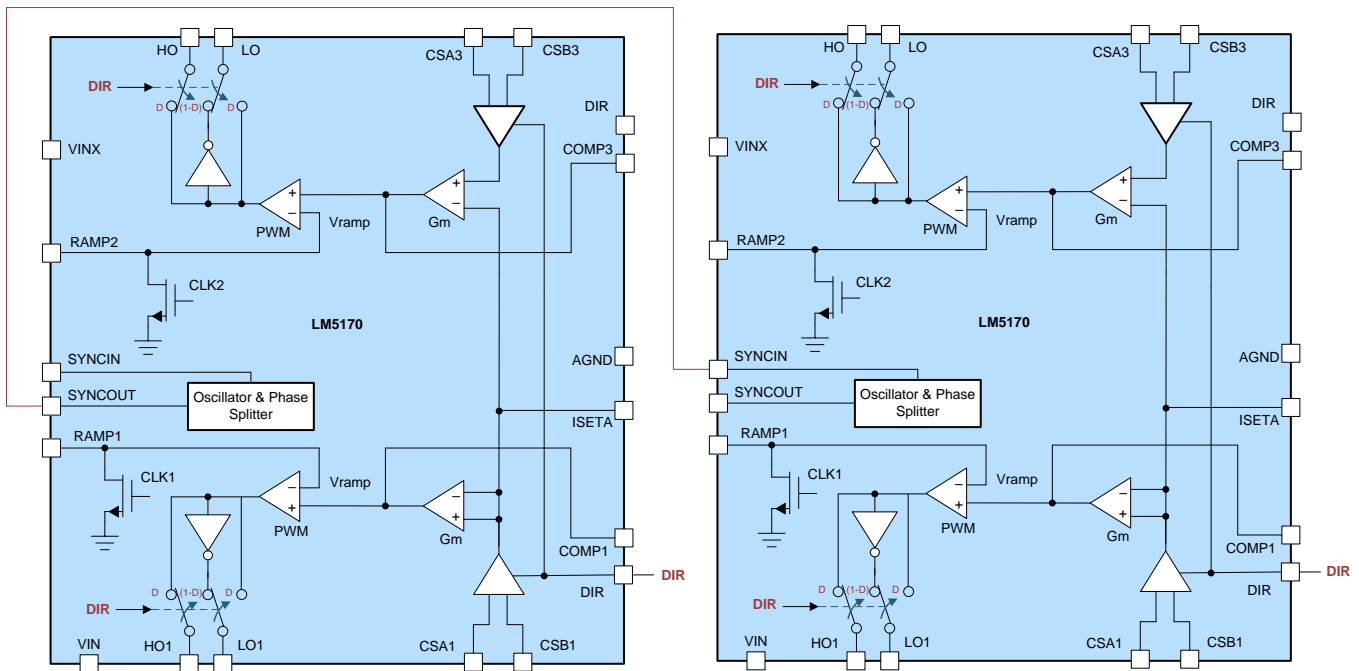


図 9. Four Phases Interchangeable Configuration



The LM5170 devices are connected from the SYNCOUT of one device to the SYNCIN of another, and can be synchronized using either an internal or external clock reference. The OPT pin of the LM5170 allows the user to adjust the phase delay of the SYNCOUT pin. A high value on the pin provides a 90 degree phase shift needed for this four-phase design. See 表 5 for proper jumper setup for multiphase configuration.

図 10. LM5170 Daisy Chain Configuration



This reference design can also be operated in a two-phase, 50-A configuration using a single LM5170 device. This is done by disconnecting jumper 3, the SYNC connection between both LM5170 devices.

This reference design requires simultaneous control of both current and voltage within an accuracy of $\pm 0.05\%$ to properly perform the battery test. The next two sections detail the design of the current and voltage control systems.

2.3.2 Constant Current Control Design

This section details the process for designing the control system that handles constant current flow for battery charging and discharging. See 3.1.4.1 for more information on accuracy test results for this system. For information on part selection and the simulation tool used for this design, see the [TIDA-01040 battery tester reference design for high current applications reference design](#).

The INA828 device, a precision instrumentation amplifier, provides a low-noise differential signal that dictates current regulation. The TIDA-01040 design uses the INA188 device as its instrumentation amplifier. There are two gain settings for the instrumentation amplifier: low current (0–50 A) and high current (50–100 A) as 図 11 shows.

図 11. INA828 Gain Settings

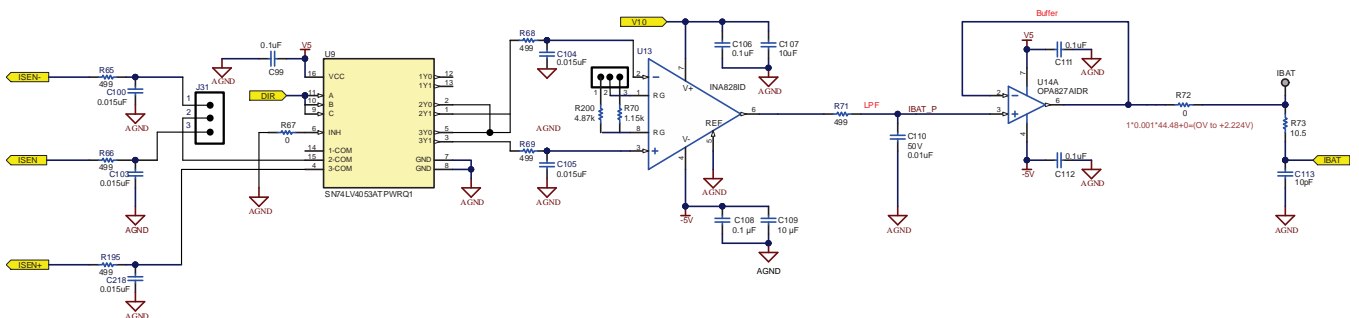


図 12. Vcm vs Vout Calculator for INA828 at Gain = 44.48 and 88.96

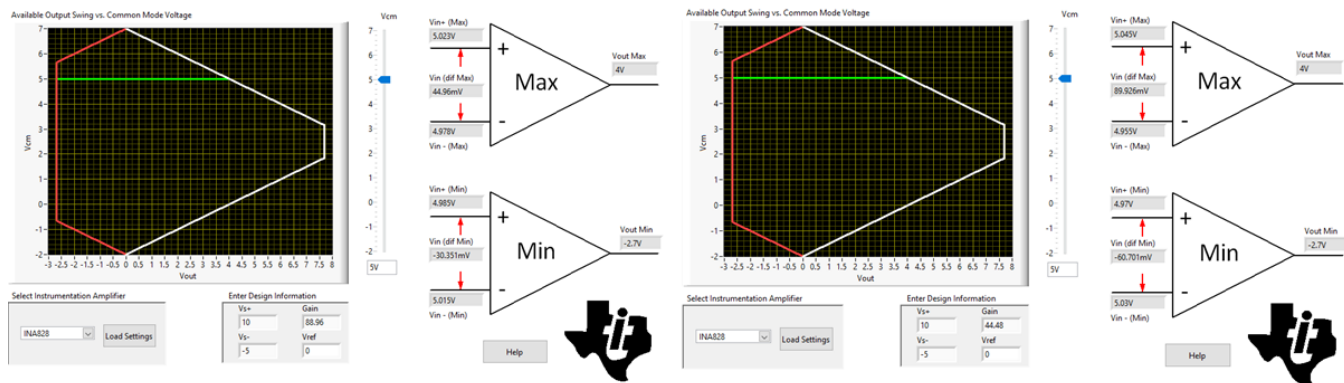


図 12 highlights the calculation results of the INA828 input and output ranges for this reference design. In this case, the maximum common-mode voltage is the same as the maximum voltage on the battery side, so its maximum value is 5 V. For low current gain at 44.48, the input range for an INA828 device with power rails at 10 V and -5 V is -60.701 mV to 89.926 mV. For high current gain at 88.96, the calculation results show the input range from -30.351 mV to 44.96 mV. These ranges both fit within the current signal range ($\pm 100 \text{ A} \times 0.5 \text{ m}\Omega = \pm 50 \text{ mV}$).

Due to the high precision of the INA828 device, the CC control amplifier it provides feedback to needs to meet certain accuracy requirements or it will bottleneck the design. In the 100-A high-current application, worst-case, the input offset voltage causes an error of $112.5 \mu\text{V} / (100 \text{ A} \times 0.001 \times 21.57) \times 100\% = 0.005216\%$ on the control loop. The error is less than the 0.01% demanded accuracy, making the TLV07 device a suitable amplifier.

Further information on the TLV07 device and its control stability is found in the [TIDA-01040 battery tester reference design for high current applications reference design](#).

図 13 shows the CC control simulation schematic. To keep the system working in CC control mode, ISETA provides a DC voltage for D4 to conduct continuously. ISET1 and ISET2 capture the differential voltage across the current sense resistor, E1 is an ideal differential amplifier to output a single-ended signal, R16 and C19 create a low-pass filter, and X6 is the error amplifier used to calibrate the current signal to the reference signal.

図 13. Constant Current Control Simulation Schematic

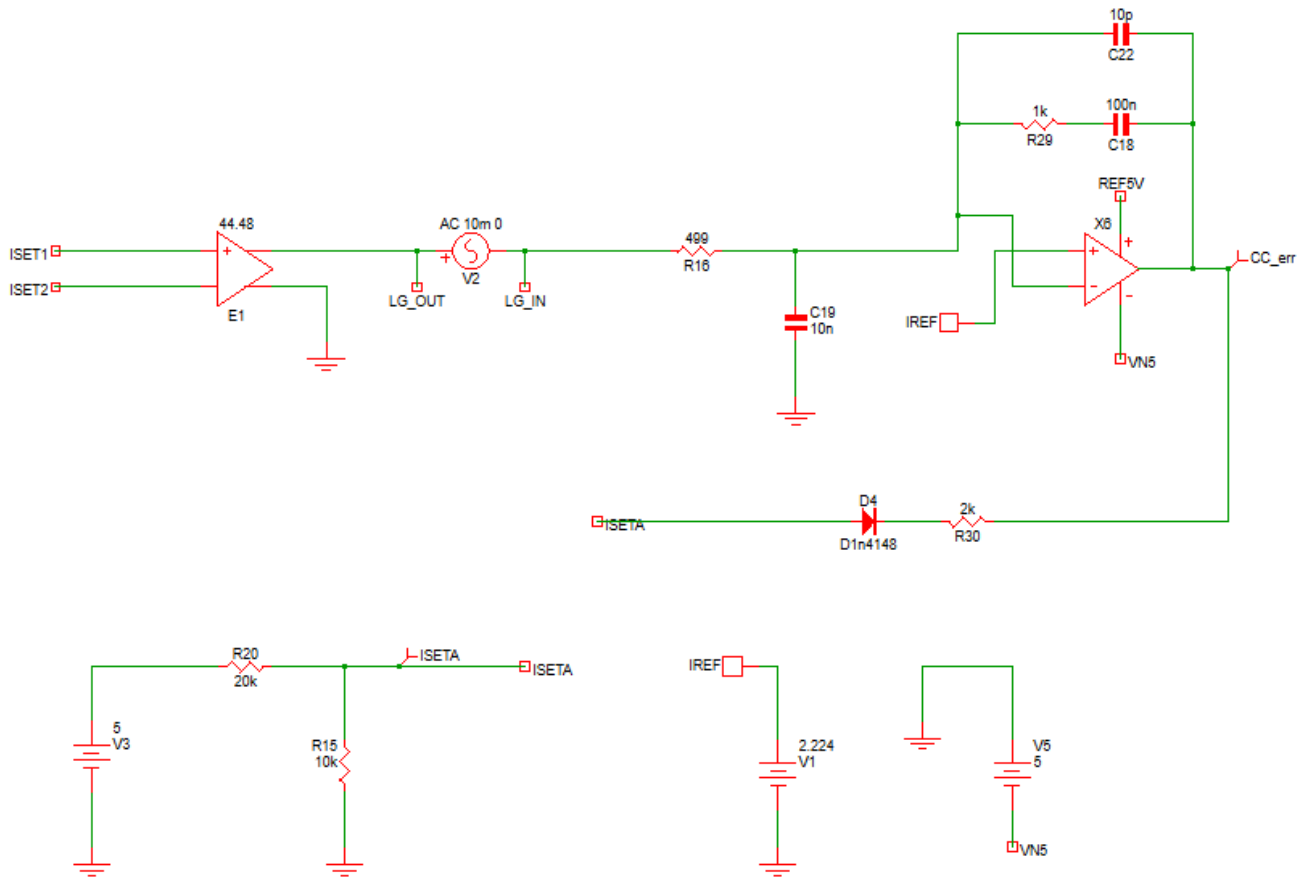
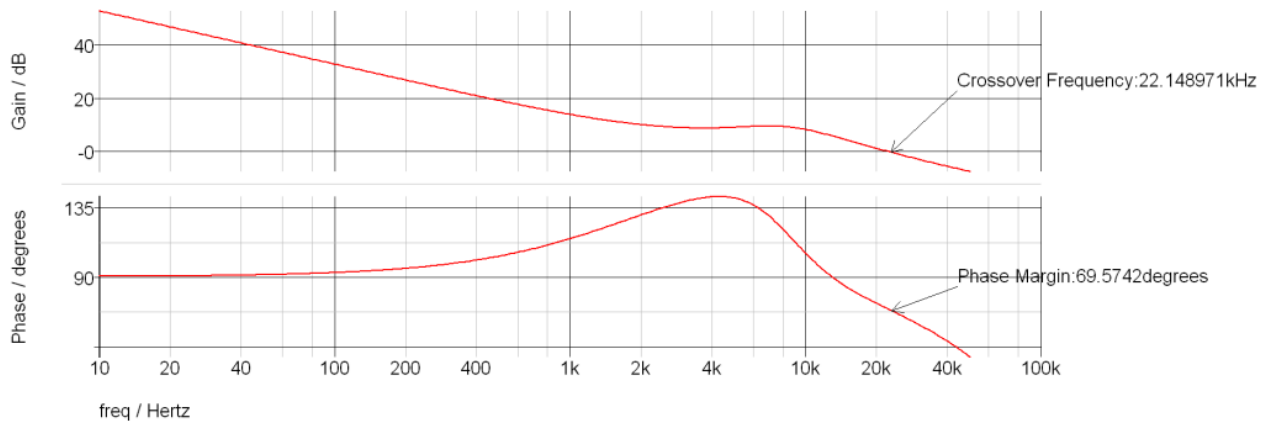


図 14 shows the small signal performance of this CC control subsystem. The gain crossover frequency is 22.15 kHz, and the phase margin is 69.57° which means this control circuit is stable and can provide enough bandwidth.

図 14. CC Small Signal Simulation Results



To generate a reference signal for current (DAC Channel D) control, commands are written to the 32-bit wide SPI shift register.

図 15. DAC SPI Shift Register

D31	D30	D29	D28	D27-D24	D23-D20	D19-D04	D03-D00
Don't Cares			R/W	Command Bits	Channel Address Bits	16/14/12-Bit DAC Data left aligned/Power Down Bits/Device Ready bit	Mode Bits

The bits that are altered for this design are the 'Channel Address bits' and the 'Data bits'. For example, inputting '03 31 C7 70' generates a reference voltage that causes the CC amplifier to regulate the charge and discharge rate of the battery to 25 A. D23–D20 is set to '03 3', selecting DAC output channel D and D19–D04 is set to '1 C7 7', which generates a decimal value that is converted into an analog signal based off the bit rate of the DAC and its voltage reference, calculated with 式 2 and 式 3.

$$D_{IN} = \frac{INAGAIN}{REFIN} \times R_{CS} \times \text{Ideal Current} \times 65536 \quad (2)$$

$$V_{OUT} = \frac{D_{IN}}{2^N} \times REFIN \quad (3)$$

More information on DAC80004 commands are found in the [DACx0004, quad 16-,14-,12-bit, 1 LSB INL, buffered, voltage-output digital-to-analog converters data sheet](#).

2.3.3 Constant Voltage Control Design

For information on part selection and the simulation tool used for this design, see the [TIDA-01040 battery tester reference design for high current applications reference design](#). There is no difference in constant voltage control design between the TIDA-01041 and the TIDA-01040 designs. This is because the output voltage at the battery is still regulated to the same range (0 V to 4.2 V).

See 3.1.4.2 for more information on accuracy test results for this system.

To generate a reference signal for voltage (DAC Channel A) control, commands are written to the 32-bit wide SPI shift register.

The bits that are altered for this design are the 'Channel Address bits' and the 'Data bits'. For example, inputting '03 0B 87 F0' generates a reference voltage that causes the CV amplifier to regulate the voltage of the battery to 4.2 V. D23–D20 is set to '03 0', selecting DAC output channel A and D19–D04 is set to 'B 87 F' which generates a decimal value that is converted into an analog signal based off the bit rate of the DAC and its voltage reference.

$$V_{OUT} = \frac{D_{IN}}{2^N} \times REFIN \quad (4)$$

$$D_{IN} = \frac{INAGAIN}{REFIN} \times \text{Ideal Voltage} \times 65536 \quad (5)$$

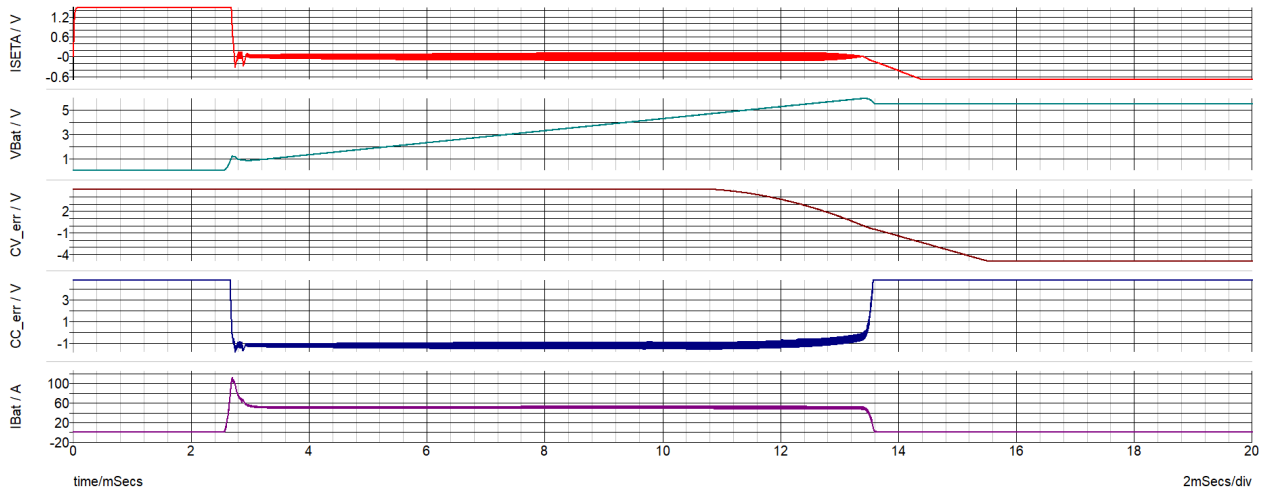
More information on DAC80004 commands is found in the [DACx0004, quad 16-,14-,12-bit, 1 LSB INL, buffered, voltage-output digital-to-analog converters data sheet](#).

2.3.4 System Transient Response

Figure 13 is the simulation schematic of the CC control, CV control, and multiphase design steps connected to create the complete TIDA-01041 system, giving an indication of the expected transient results for both control subsystems and the system as a whole. The CC and CV control designs are connected to one another by R20, R15, D4, and R30. This connection simulates the startup of the control systems: the CV amplifier produces a high voltage to bias the diode, turning on the CC amp and starting the control loop for the system. The output of these amplifiers is connected to the ISETA pin on both LM5170 devices that sets current regulation for each power stage being used to charge and discharge the battery, which is then simulated with the R12 load and C14.

Figure 16 shows the results of the system transient simulation and measurements. The voltage in the loop at startup is low, causing the CV loop to output a high voltage to compensate. This voltage causes the diode, D4, to conduct and the CC control loop starts taking control of the system. When the CC control loop takes over, the current going to the battery, IBAT, keeps constant at 100 A and the battery voltage increases over time. Once the battery reaches 4.5 V, the CV control loop takes back control of the system and decreases the output voltage. The battery current then decreases and voltage is kept steady.

Figure 16. Transient Response



2.4 Highlighted Products

This section provides more detail on some of the core products that make up this design, explaining why they were selected and their potential alternatives.

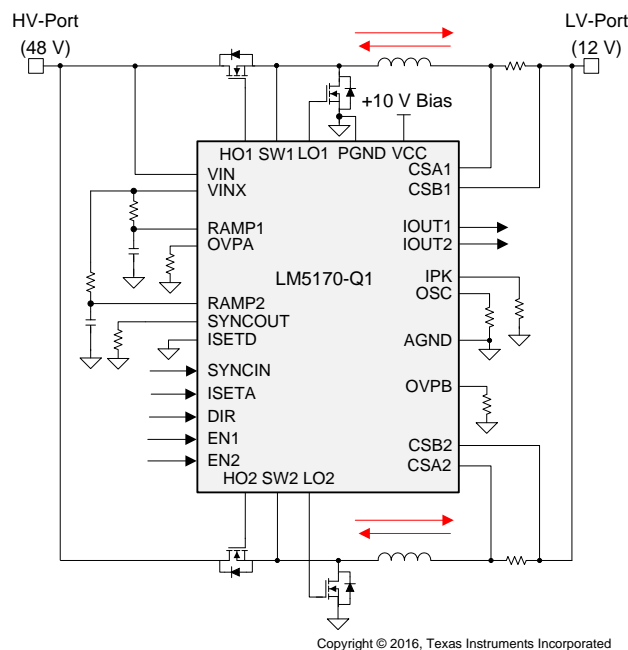
2.4.1 LM5170-Q1 Multiphase Bidirectional Current Controller

The LM5170-Q1 is a dual-channel, bidirectional, multiphase controller that can support high current battery test applications up to 200 A using eight phases. It can regulate the average current flowing between the high and low voltage ports in the direction designated by the DIR input signal.

Other important features include:

- 5-A peak half-bridge gate drivers which enables the ability to drive high currents
- Programmable oscillator frequency which allows the user to choose the FET switching frequency
- MOSFET failure detect at start-up and circuit breaker control which provides security to the system

図 17. LM5170-Q1 Simplified Application Circuit



For more on multiphase design, its benefits and the daisy chain configuration used for this design, see [2.3.1](#).

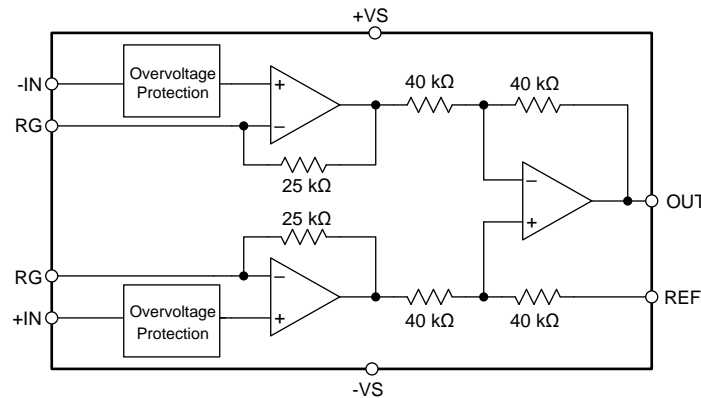
2.4.2 INA828 Precision Instrumentation Amplifier

The INA828 is a precision instrumentation amplifier with integrated resistor networks for sensing and data acquisition systems. This device measures and amplifies a differential voltage that represents output current which acts as feedback to regulate current. The INA828 device uses super-beta input transistors which allows for lower input bias current and current noise while also improving input offset voltage and offset drift.

Other important features include:

- Gain drift: 50 ppm/°C ($G > 1$) which limits the variation of calibration at high temperatures
- Bandwidth: 2 MHz ($G = 1$), 260 kHz ($G = 100$) which allows for fast transients
- Inputs protected up to ± 40 V which provides protection to the device
- Power-supply rejection: 100 dB, minimum ($G = 1$) which limits the noise observed on the signal chain

図 18. INA828 Simplified Block Diagram



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Alternatives:

The INA828 device offers lower noise than its predecessor, the INA188 device, but has a narrower bandwidth than the INA821. The INA828 device is pin-to-pin compatible with the SOIC package of the INA188 device. The INA819 has the best performance for error with only slightly more noise than the INA828.

表 2. INA828 Alternatives

	INA828	INA821	INA188	INA819
Quiescent current	0.6 mA	0.6 mA	1.4 mA	350 μ A
Noise density @ 1 kHz	7 nV/ $\sqrt{\text{Hz}}$	7 nV/ $\sqrt{\text{Hz}}$	12 nV/ $\sqrt{\text{Hz}}$	8 nV/ $\sqrt{\text{Hz}}$
Gain error (\pm)	0.15%	0.15%	0.50%	0.005%
Bandwidth at $G = 1$	2 MHz	4.7 MHz	0.6 MHz	2 MHz

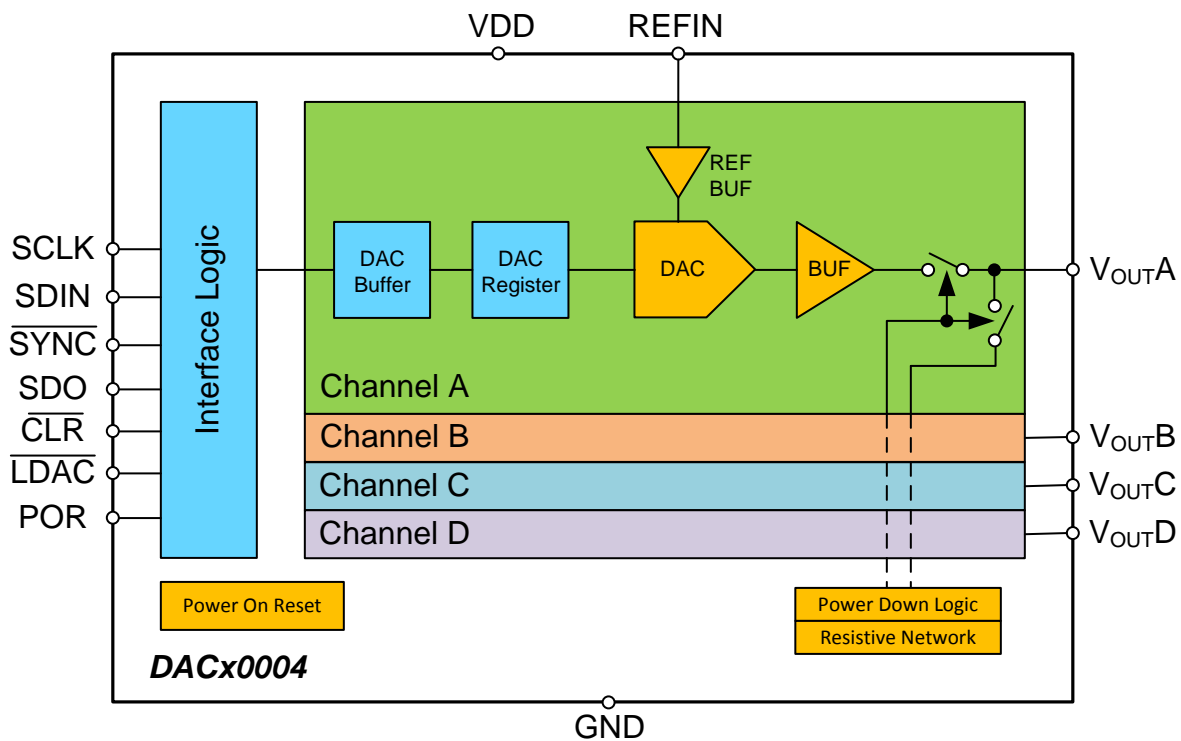
2.4.3 DAC80004 16-Bit DAC With 1 LSB INL/DNL

The DAC80004 device is low-power, quad-channel, 16-bit digital-to-analog converter. Hexadecimal values are written to the DAC using a computer which produce voltages at two channels. These voltages set the battery voltage charge and discharge rate. The four channels of the DAC80004 are used for the generation of high accuracy, user-defined voltage references.

Other important features include:

- True 16-bit performance: 1 LSB INL/DNL (maximum) which ensures accurate references for current and voltage
- Output buffer with rail-to-rail operation which provides clean references for current and voltage
- 50 MHz, 4- or 3-wire SPI-compatible which allows for simplified user interface

図 19. DAC80004 Simplified Block Diagram



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Alternatives:

The DAC80508 device is an eight channel DAC from the same family as the DAC80004.

表 3. DAC80004 Alternatives

	DAC80004	DAC80508
INL/DNL	1 LSB (Max)	1 LSB (Max)
# of Channels	4	8
Glitch Energy	1 nV-s	4 nV-s

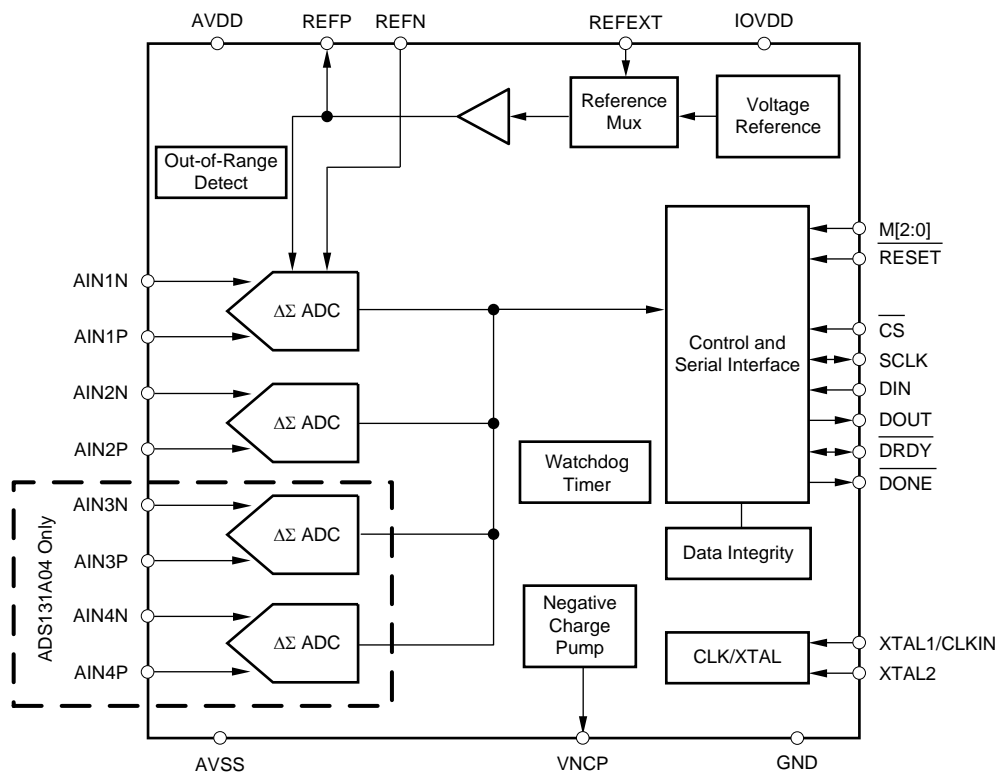
2.4.4 ADS131A04 24-Bit, 128-kSPS, 4-Channel, Simultaneous-Sampling Delta-Sigma ADC

The ADS131A04 device uses four channels to simultaneously and continuously sample voltage or current measurements. The ADC is the front-end of the battery tester and interface with a computer to display voltage and current values in TI's EvaluaTion software. The ADS131A04 device is well equipped for measuring current and voltage signals due to it being a simultaneous sampling 4-channel converter, with a flexible SPI and data integrity to check and correct single-bit errors during data transmission.

Other important features include:

- Single-channel accuracy: Better than 0.01% at 10,000:1 dynamic range which enables high accuracy data acquisition
- Effective resolution: 20.6 bits at 8 kSPS which allows for high accuracy data acquisition
- Low-drift internal voltage reference: 6 ppm/°C which limits the effects that temperature has on the data acquisition
- Multiple SPI data modes which allows for a simplified user interface

図 20. ADS131A04 Simplified Block Diagram



Alternatives:

The ADS131E08 and ADS131E04, predecessors to the ADS131A04, have a lower data rate but implement integrated buffer amplifiers.

表 4. ADS131A04 Alternatives

	ADS131A04	ADS131E08	ADS131E04
Data Rates (Max)	128 kSPS	64 kSPS	64 kSPS
# of Channels	4	8	4

表 4. ADS131A04 Alternatives (continued)

	ADS131A04	ADS131E08	ADS131E04
SNR	115 dB	107 dB	107 dB

2.4.5 Other Highlighted Products

In addition to the key products highlighted in the previous sections this reference design also showcases the following Texas Instruments devices:

1. OPA2277 precision op amp; DAC driver buffer
2. OPA827 precision op amp; ADC current and voltage measurement buffers
3. TPS709 LDO regulators; 5-V DAQ and control power rails
4. TLV07 36-V precision, rail-to-rail output, op amp; CC control amplifier
5. THS4561 low-power, 70-MHz, high-supply range, fully differential amplifier; differential signal input for ADC
6. LM2664 switched capacitor voltage converter; -5-V power rail
7. LM7705 low-noise negative bias generator; -0.2 power rail
8. LM5118 non-synchronous buck-boost controller; 10-V power rail
9. LM6142 rail-to-rail I/O op amp; CV control amplifier
10. SN74LVC1G04 single inverter; boost control logic
11. SN74LV1T32 2-input positive OR gate; boost control logic
12. SN74LV1T00 2-input positive NAND gate; buck control logic

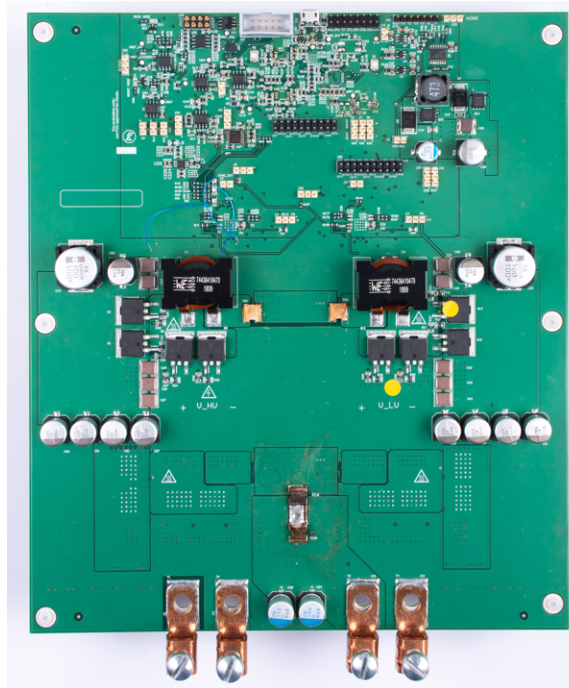
3 Hardware, Software, Testing Requirements, and Test Results

3.1 Testing and Results

3.1.1 Getting Started: Hardware

See the TIDA-01040 design guide for general details on each hardware subsystem in this design.

図 21. TIDA-01041 Hardware



This section gives brief information to set up and run the board. 図 21 shows the sections of the board.

This system has some configuration options. 表 5 highlights the purpose of each jumper as well as the default configurations.

表 5. Jumper Configuration

HEADER	SIGNAL	PINS	FUNCTION DESCRIPTION	DEFAULT
J1	UVLO	(1,2)	Enable from V_HV	Y
		(2,3)	Enable from V_LV	
J3	SYNCOUT	(1,2)	Clock output for multiphase configuration	Y
J4	V10-Aux	(1,2)	Auxiliary power	Y
J5	OPT	(1,2)	Multiphase configuration	Y
		(2,3)	No multiphase configuration	
J6	DIR	(1,2)	Buck mode	Y
		(2,3)	Boost mode	
J7	EN1	(1,2)	Onboard CH-1 enable	
		(2,3)	Onboard CH-1 disable	Y
J8	EN2	(1,2)	Onboard CH-2 enable	
		(2,3)	Onboard CH-2 disable	Y
J13	UVLO	(1,2)	Enable from V_HV	Y
		(2,3)	Enable from V_LV	

表 5. Jumper Configuration (continued)

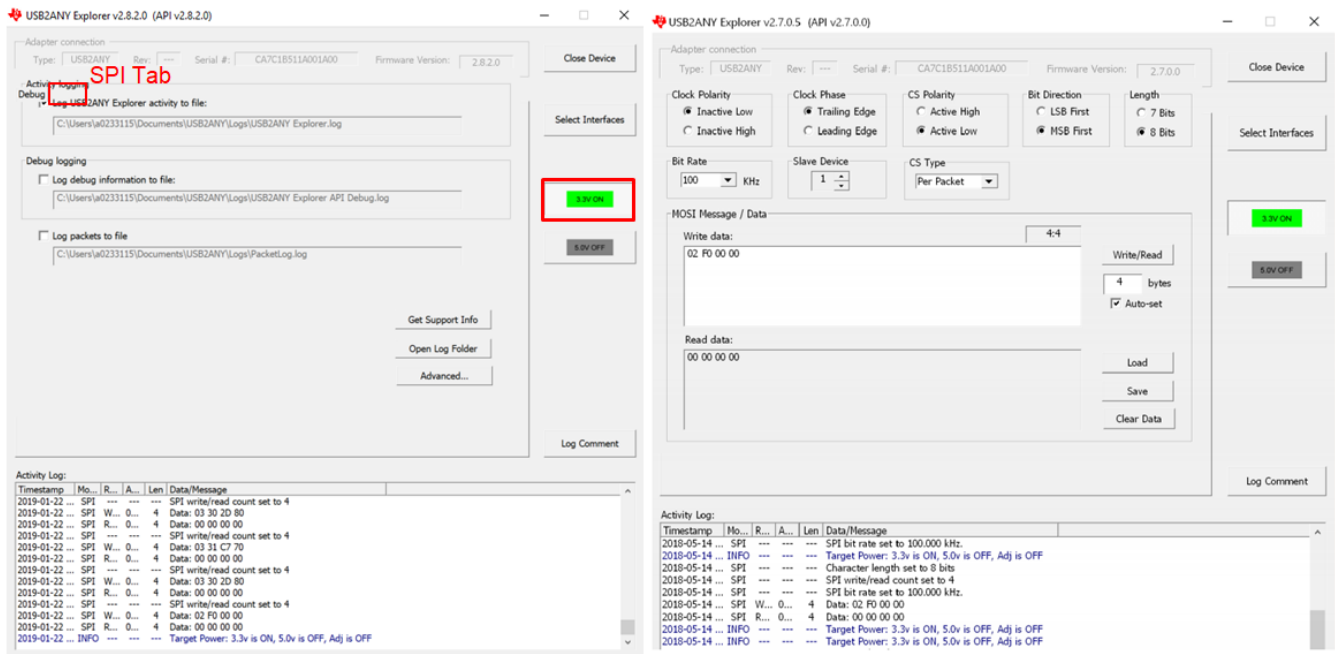
HEADER	SIGNAL	PINS	FUNCTION DESCRIPTION	DEFAULT
J14	V5	(1,2)	Enable power supply for CC control	Y
J16	V-5	(1,2)	Enable -5-V power supply	Y
J18	IREF/VREF	(1,2),(7,8)	Enable DAC output signal for CC/CV control loop	Y
J24	INA828 GAIN	(1,2)	High current (50–100 A) gain	
		(2,3)	Low current (0–50 A) gain	Y
J25	EN3	(1,2)	Onboard CH-3 enable	
		(2,3)	Onboard CH-3 disable	Y
J26	EN4	(1,2)	Onboard CH-4 enable	
		(2,3)	Onboard CH-4 disable	Y
J27	SYNCOUT2	(1,2)	Clock output for multiphase configuration	N
J29	OPT2	(1,2)	Multiphase Configuration	Y
		(2,3)	No multiphase configuration	
J34	V_HV	(1,2)	Enable CV control for bus voltage(V_HV)	N
J35	V_LV	(1,2)	Enable CV control for battery voltage(V_LV)	Y
J37	V5A	(1,2)	Enable power supply for CV control	Y

3.1.2 Getting Started: Software

3.1.2.1 DAC Setup

This reference design uses the USB2ANY interface adapter to communicate with the DAC80004 device to generate a reference signal for current and voltage control. First, open the USB2ANY Explorer, click *Select Interface* to choose the SPI, then click the 3.3V ON button. Click the *SPI* tab above the *Activity Logging* section. If the *SPI* tab does not appear, click around the words "Activity Logging" as sometimes the tabs are hidden. Configure the GUI parameters as [Figure 22](#) shows.

Figure 22. USB2ANY Configuration

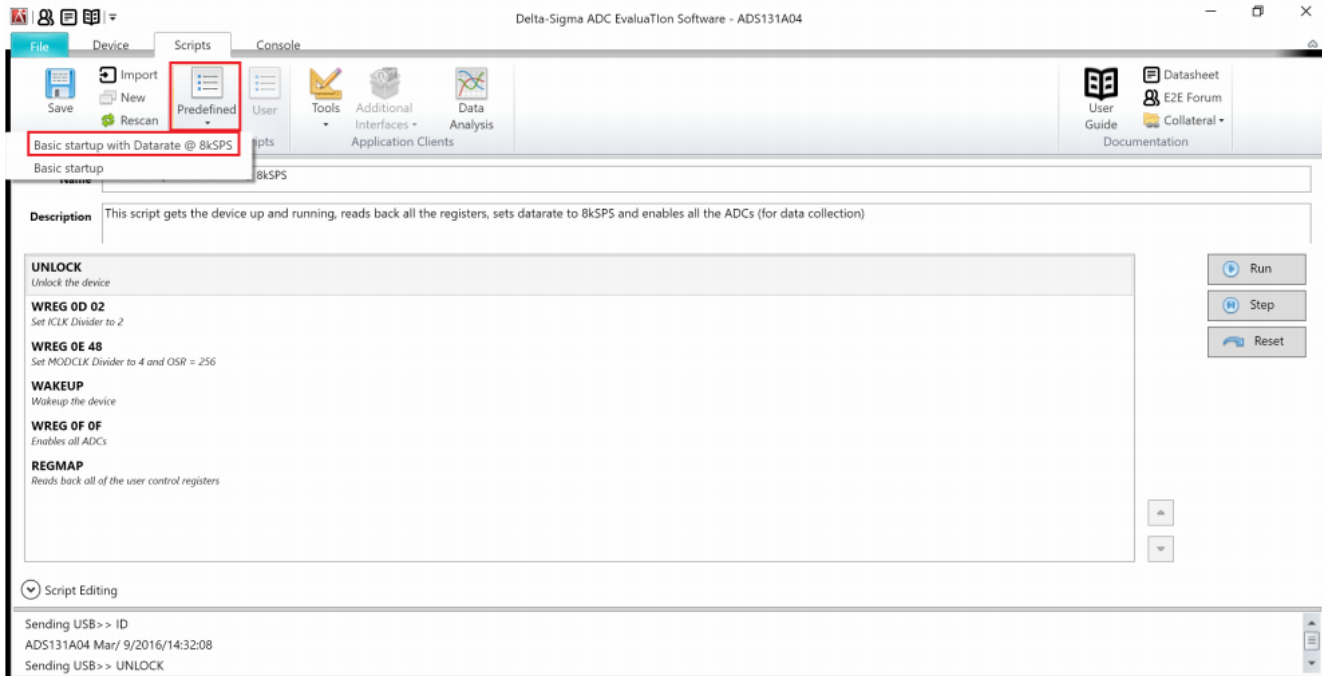


3.1.2.2 ADC Setup

Delta-Sigma ADC Evaluation Software is used to communicate with the ADS131A04 device. See the [Delta-Sigma ADC Evaluation software user's manual](#) and [ADS131A04 evaluation module user's guide](#) for detailed information.

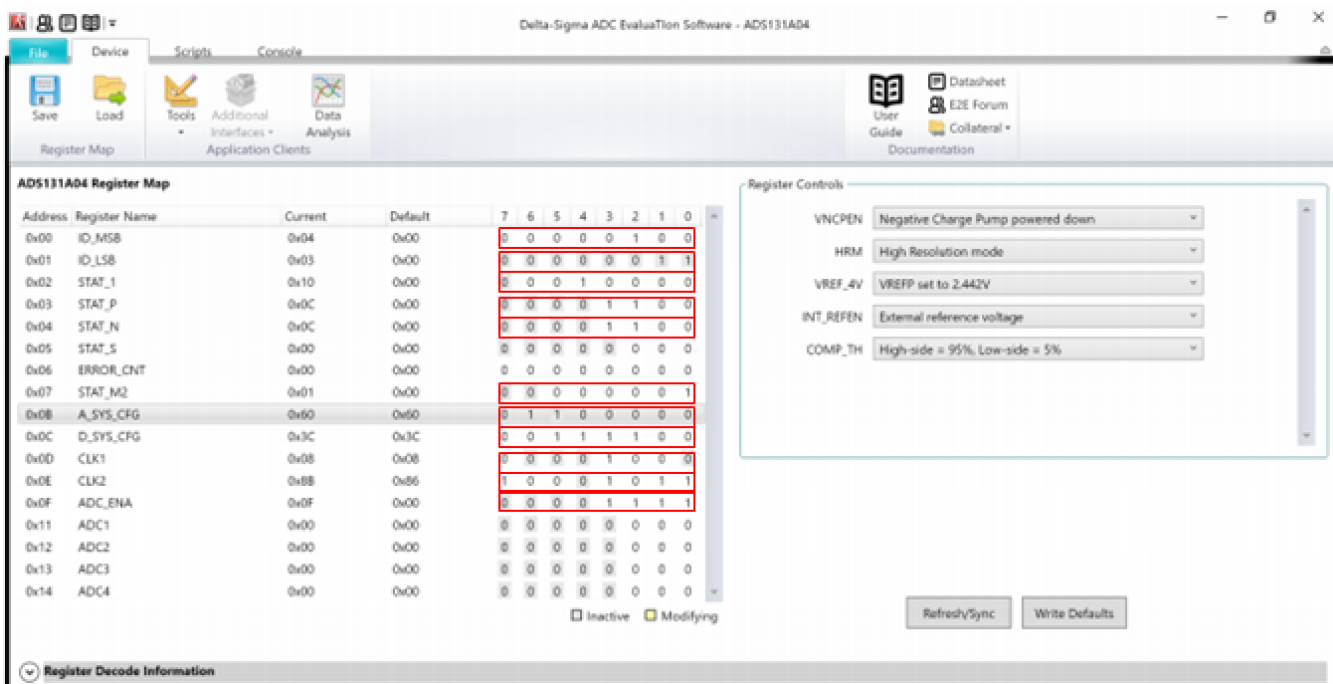
After launching this software, click the *Scripts* menu, then click *Predefined* and choose *Basic* startup with Datarate at 8 kSPS as [Figure 23](#) shows. Finally, click the *Run* button at the right side of the window.

Figure 23. ADC GUI Setting



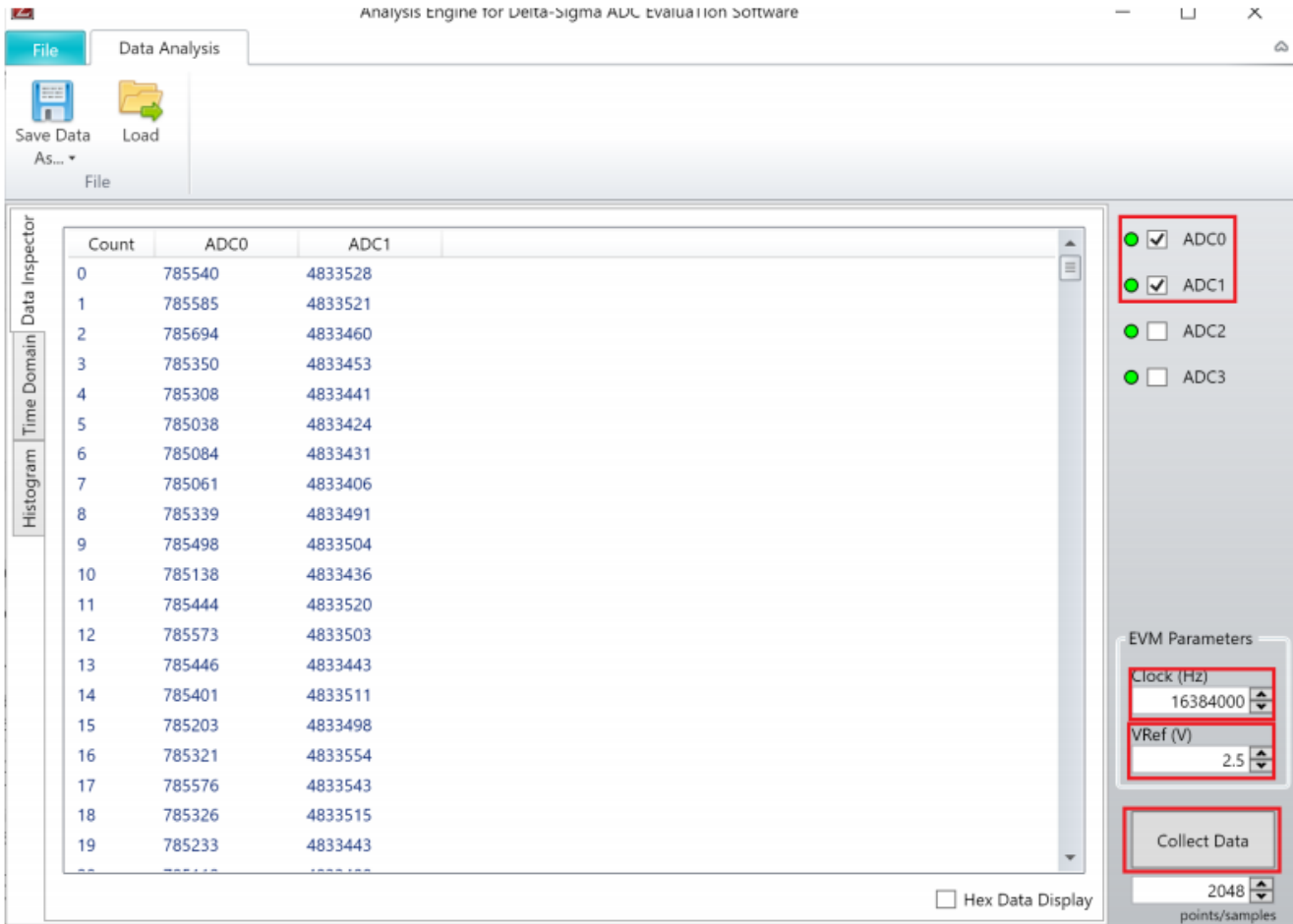
The second step is to set the registers of the ADC. [Figure 24](#) highlights the registers that need to be changed and their correct values for this design. It can also modify clock and OSR settings.

Figure 24. ADC Register Setting



After setting the GUI and registers, the software can now capture data: click the *Data Analysis* menu, choose "ADC0" and "ADC1", change the Clock and VRef (V), and click the *Collect Data* button as [Figure 25](#) shows.

Figure 25. ADC GUI Collect Data



The raw data is shown on the GUI, but the mean value of current and voltage is needed.

図 26. ADC GUI Data Analysis

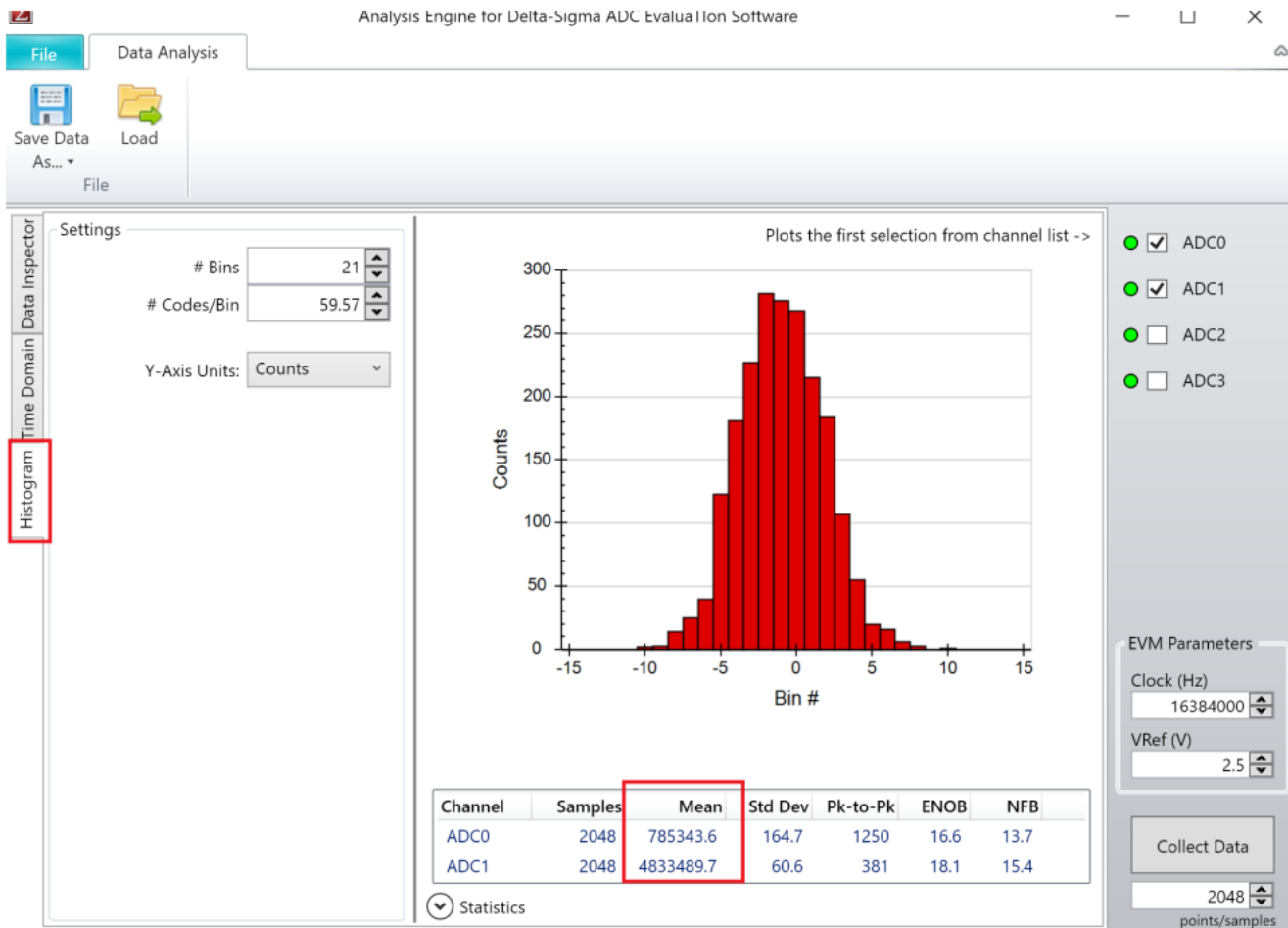


図 26 illustrates the GUI when the Histogram menu at the left corner is clicked. It shows the mean value on the bottom after analysis in full scale format. Divide by 8388607 (DEC of 0X7FFFFFFF), and multiply by the reference voltage of the ADC, resulting in the current and voltage values as seen in 式 6 and 式 7. This example was tested under CC control: the control current is 5 A, the battery voltage is 3.1 V.

$$ADC_{\text{current}} = \frac{ADC0_{\text{Mean}}}{8388607} \times V_{\text{Ref}} = \frac{785343.6}{8388607} \times 2.5 \quad V = 234.05 \text{ mV} \quad (6)$$

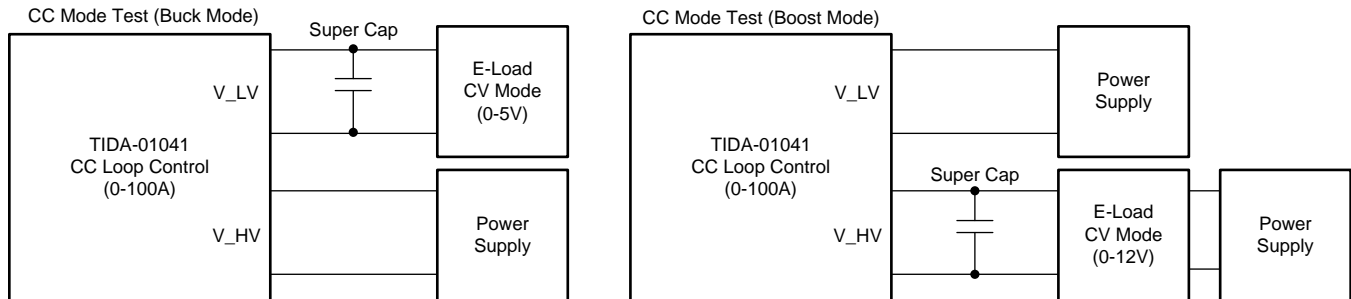
$$ADC_{\text{voltage}} = \frac{ADC1_{\text{Mean}}}{8388607} \times V_{\text{Ref}} = \frac{4833489.7}{8388607} \times 2.5 \quad V = 1.4405 \text{ V} \quad (7)$$

The expected value of channel 0 should be $(I_{\text{set}} \times R_{\text{cs}} \times \text{Gain_INA188} \times \text{Gain_ADC0}) = 5 \text{ A} \times 0.5 \text{ m}\Omega \times 88.96 \times 1 = 222.4 \text{ mV}$, and the expected value of channel 1 should be $(V_{\text{set}} \times \text{Gain_ADC1}) = 3.1 \text{ V} \times (1.5 \text{ k}/3.30 \text{ k}) = 1.4091 \text{ V}$. Those values are close to the mean value from the histograms. Due to the offset and noise of the components, refer to 3.1.4.4 to calibrate the ADC. The result is a more accurate value.

3.1.3 Test Setup

The test setup for the buck and boost mode operations of the TIDA-01041 require different setups for current and voltage control tests. [Fig 27](#) shows a block diagram of the hardware setup for the TIDA-01041 current control test.

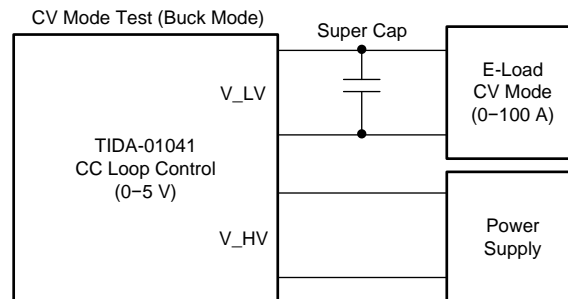
Fig 27. CC Mode Test Setup



First and foremost, the power supplies need to be able to provide enough power in both buck and boost mode or the electronic load will not operate properly. Configure the TIDA-01041 board to buck or boost mode through the "DIR" header (J6). Once configured, write to the DAC to generate current and voltage reference signals to start both control loops. Configure the electronic load to operate in CV mode, the voltage at the electronic load **must** be smaller than the constant voltage reference set by the DAC, allowing the CV control loop to give enough forward voltage for D3, and the TIDA-01041 design can work in CC mode. The super capacitor is required to clamp the output voltage and simulate the battery performance.

[Fig 28](#) shows the block diagram of the hardware setup for the TIDA-01041 voltage control loop test.

Fig 28. CV Mode Test Setup



For this design to operate in CV mode, set the electronic load to CC mode and write to the DAC to generate current and voltage reference signals to start both control loops. The current at the electronic load **must** be smaller than the constant current reference voltage set by the DAC.

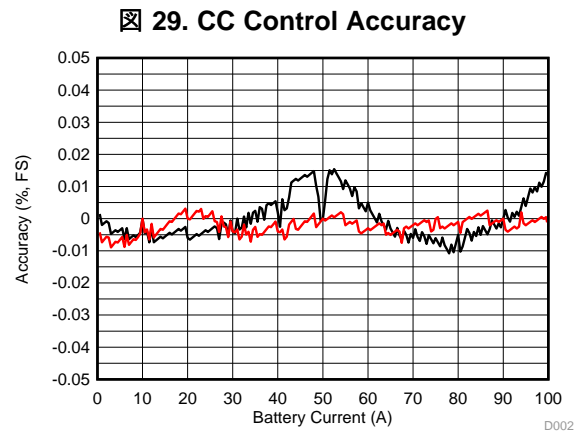
3.1.4 Test Results

Battery test equipment must possess accurate voltage and current control, often better than $\pm 0.05\%$, as well as a smooth transition between the two to maximize capacity, battery life, quality and performance. This section provides accuracy testing results for current and voltage control for this design as well as the performance of the system when transforming between CC and CV mode.

3.1.4.1 Current Control Accuracy

The current accuracy depends on the current sensing resistor, the gain, offset, and drift of the current amplifier, INA828, and TLV07 devices. For more information on current accuracy in this design as well as the calibration process for buck and boost mode operations, see the [TIDA-01040 battery tester reference design for high current applications reference design](#).

Figure 29 shows the CC control accuracy of this reference design at buck (high side is 12 V, low side is 1 V) and boost (low side is 2 V, high side is 10 V) mode conditions.



The results show that CC control can maintain $\pm 0.02\%$ accuracy within the full current range of this design 0.5 A–100 A, meeting the accuracy range requirements to maximize battery performance.

3.1.4.2 Voltage Control Accuracy

This system requires calibration due to the voltage control accuracy being affected by the gain offset, offset of the resistor divider at the output of the LM6142, and the LM6142 itself. See the [TIDA-01040 battery tester reference design for high current applications reference design](#) for more information on the calibration method for these test results.

図 30. CV Control Accuracy

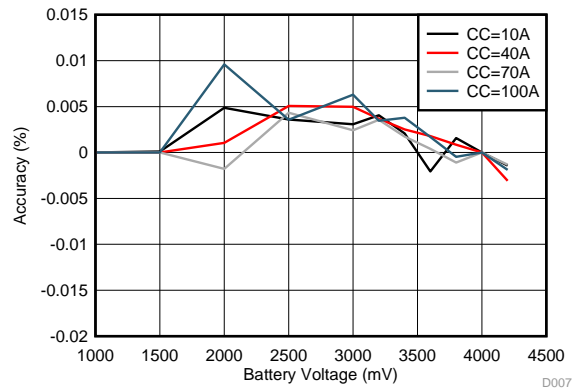


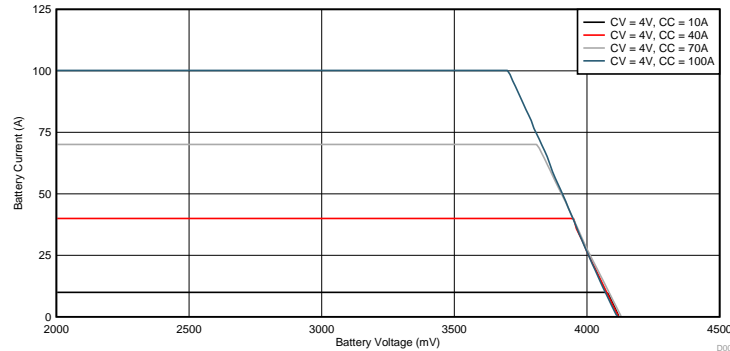
図 30 shows that the CV control can maintain $\pm 0.01\%$ accuracy within a battery voltage range of 1.0 V–4.2 V, meeting the accuracy range requirements to maximize battery performance.

3.1.4.3 CC, CV Transformation

It is critical to understand the performance of the system when transforming from CC to CV mode as this will affect its ability to eliminate overcharging in the battery.

Figure 31 and Figure 32 show the transformation under different current and different voltage settings.

Figure 31. CC, CV Transformation Under Different Current Settings



In Figure 31, with the increase in current setting, the CC control will start transforming to CV control at lower voltage. The transformation remains linear throughout testing, indicating that the ability of the design to eliminate overcharging is not affected at higher currents.

Figure 32. CC, CV Transformation Under Different Voltage Settings

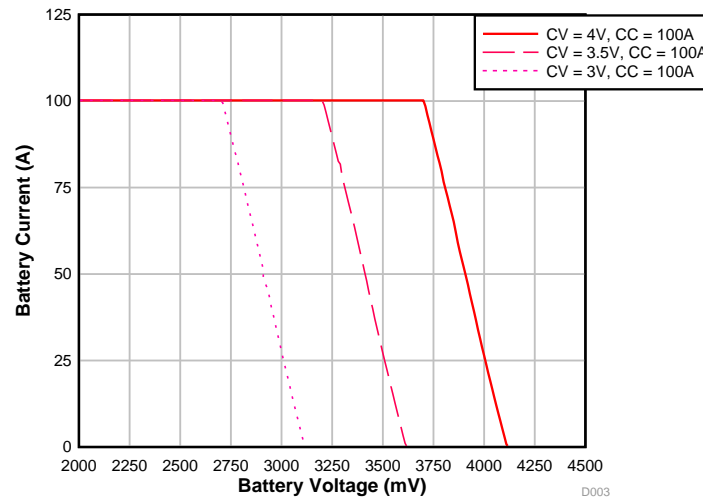


Figure 32 shows that voltage setting has less effect on the switch from CC control to CV control.

3.1.4.4 ADC Calibration

Two channels are used to monitor the battery current and voltage. The accuracy of this data acquisition depends on the gain and offset of the THS4561 device and other components, so the output of the ADC should be calibrated. Use a similar method to calibrate those two channels as the previous current and voltage control loop.

Figure 33 and Figure 34 show the accuracy of this data acquisition after calibration.

Figure 33. ADC Current Acquisition Accuracy

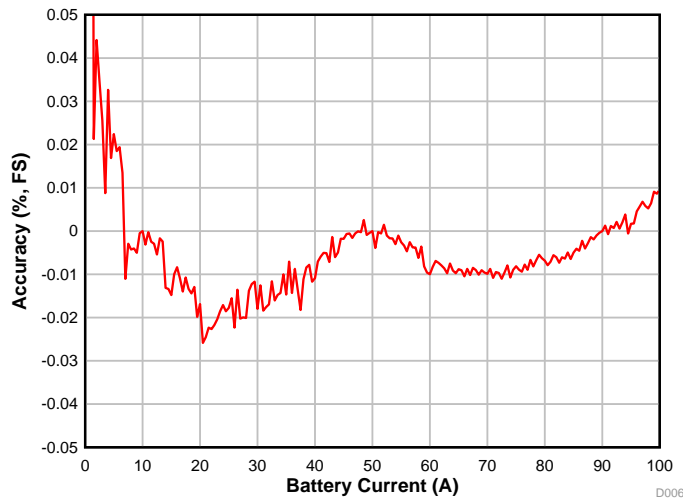
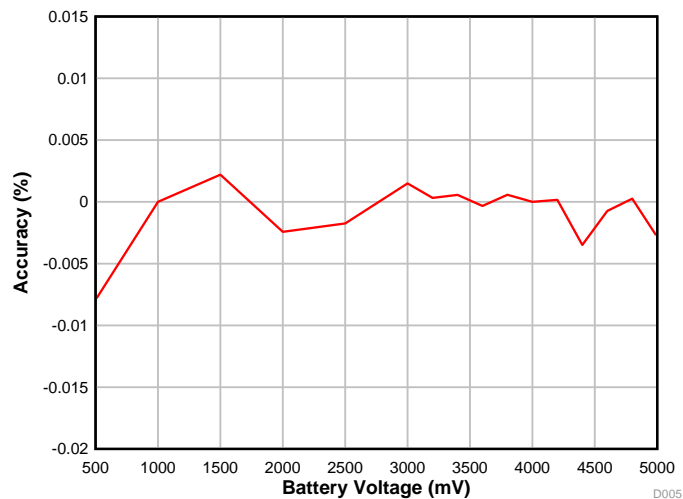


Figure 34. ADC Voltage Acquisition Accuracy



The results show the ADC current acquisition accuracy is excellent. Although the ADC current acquisition accuracy is not good in the low current range, battery tester applications usually are more concerned with the accuracy at higher currents.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at [TIDA-01041](#).

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01041](#).

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-01041](#).

4.4 Altium Project

To download the Altium Designer® project files, see the design files at [TIDA-01041](#).

4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-01041](#).

4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-01041](#).

4.7 Simulation Results

To download the simulation results, see the design files at [TIDA-01041](#).

5 Software Files

To download the software files, see the design files at [TIDA-01041](#).

6 Related Documentation

1. Texas Instruments, [TIDA-01040 battery tester reference design for high current applications reference design](#)
2. Texas Instruments, [Multiphase buck design from start to finish \(Part 1\) application report](#)
3. Texas Instruments, [Merits of Multiphase Buck DC/DC Converters in Small Form Factor Applications](#)
4. Texas Instruments, [Benefits of a multiphase buck converter application note](#)
5. Texas Instruments, [LM5170-Q1 multiphase bidirectional current controller data sheet](#)
6. Texas Instruments, [LM2664 switched capacitor voltage converter data sheet](#)
7. Texas Instruments, [TPS709 150-mA, 30-V, 1- \$\mu\$ A \$I_Q\$ voltage regulators with enable data sheet](#)
8. Texas Instruments, [LM5118 wide voltage range buck-boost controller data sheet](#)
9. Texas Instruments, [INA188 precision, zero-drift, rail-to-rail out, high-voltage instrumentation amplifier data sheet](#)
10. Texas Instruments, [DACx0004, quad 16-, 14-, 12-bit, 1 LSB INL, buffered, voltage-output digital-to-analog converters data sheet](#)
11. Texas Instruments, [ADS131A0x 2- or 4-Chan, 24-bit, 128-kSPS, simultaneous-sampling, delta-sigma ADC data sheet](#)
12. Texas Instruments, [TLV07 36-V precision, rail-to-rail output operational amplifier data sheet](#)

13. Texas Instruments, [OPAx22x high precision, low noise operational amplifiers data sheet](#)
14. Texas Instruments, [OPA827 low-noise, high-precision, JFET-input operational amplifier data sheet](#)
15. Texas Instruments, [THS4561 low-power, high supply range, 70-MHz, fully differential amplifier data sheet](#)
16. Texas Instruments, [LM6142/LM6144 17 MHz rail-to-rail input-output operational amplifiers](#)
17. Texas Instruments, [PMP15038 test results technical reference](#)

6.1 商標

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7 About the Author

Maseo Browning is an application engineer at Texas Instruments, where he is responsible for developing reference design solutions for the test and measurement industry. Maseo earned his bachelors of science in electrical engineering (BSEE) degree from the Rochester Institute of Technology in Rochester, New York.

Taras Dudar is a systems design engineer and architect at Texas Instruments, where he is responsible for developing reference design solutions for the test and measurement industry. Previously, Taras designed high-speed analog SOC integrated circuits for Gbps data communications. Taras earned his master of science in electrical engineering (MSEE) degree from the Oregon State University in Corvallis, OR.

8 Acknowledgment

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改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2019年3月発行のものから更新	Page
• TLV07 を使用してブロック図を更新。.....	1
• 'CC, CV' to 'constant current (CC) and constant voltage (CV)' 変更	2
• Updated Li-Ion Battery Formation Profile section.	3
• wording throughout the System Overview section. 変更	4
• Updated the Block Diagram section.	4
• Updated block diagram with TLV07.	5
• information in 表 5 変更	21

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