参考資料

デザイン・ガイド：TIDA-010046
IEEE 802.3at Type-1 (≤ 12.95W) PoE-PD を使用した EMC 規格準拠 10/100Mbps イーサネット PHY のリファレンス・デザイン

概要

このリファレンス・デザインは、標準的なイーサネットの伝送距離の限界とされる 100m (328 フィート) を上回る 150m の伝送距離を CAT5e ケーブルでサポートする低消費電力イーサネット物理層 (PHY) DP83825I を使用して、10～100Mbps 用にコスト最適化したソリューションを提供します。また、1 次側レギュレーション・フライバック DC/DC コントローラを内蔵した IEEE 802.3at Type-1 (13W) PoE-PD TPS23755 を使用して、イーサネット・ケーブルを介した電力供給とデータ通信も評価できます。このリファレンス・デザインは、放射エミッション、ESD、EFTについて事前認証テスト済みです。

リソース

TIDA-010046	デザイン・フォルダ
DP83825I、DP83822I	プロダクト・フォルダ
TPS23755、TPS2121	プロダクト・フォルダ
ESDS312	プロダクト・フォルダ
TPS7A26、TPS23861、TPS7A4001	プロダクト・フォルダ
MSP430F5529	プロダクト・フォルダ
TPD2E001	プロダクト・フォルダ
LM3478、LP5907、LM5160	プロダクト・フォルダ

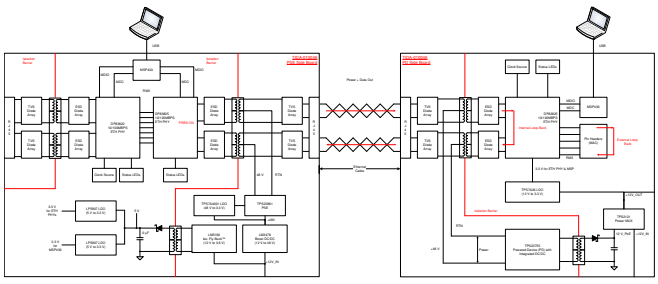
Search Our E2E™ support forums

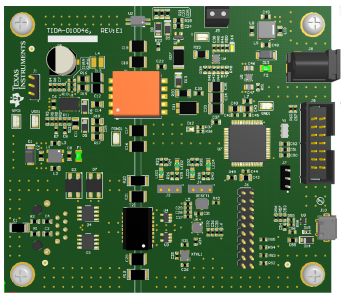
特長

- 低コスト、低消費電力、小型の 10/100Mbps イーサネット PHY DP83825I を使用、RMII 対応、ケーブル伝送距離 150m
- IEEE 802.3at Type-1 PoE-PSE および PoE-PD を使用した Power over Ethernet (PoE) による高効率電力供給システム
- 以下の放射エミッション要件に対して事前認証テスト済み
  - CISPR 22 (EN 55022)：クラス A および B の基準を満たす
  - FCC Part 15：クラス A および B の基準を満たす
- 以下の伝導イミュニティ要件に対して事前認証テスト済み
  - ±12kV 接触放電および ±15kV 気中放電 ESD IEC 61000-4-2：基準 B を満たす
  - IEC 61000-4-4 に準拠した ±2kV IO 容量結合 EFT：基準 B を満たす
- 外部絶縁変圧器と PHY 側コモンモード・チョークにより EMI および EMC 性能を向上
- リンクとアクティビティを示すプログラマブル LED のサポート

アプリケーション

- ビデオ監視
- ビル・セキュリティ・システム
- 防火システム
- HVAC (暖房、換気、空調)





1 System Description

Currently, an IP-based Ethernet network infrastructure is already in place, which means an IP-enabled device can easily be connected to the network. Simply setup the IPd address and you are up and running. Adding more IP-enabled devices to a network is as easy as the first one. From the installation perspective, there can be scenarios where you need to run a longer cable that may lie beyond the standard Ethernet distance limitation of 100 m (328 feet). Some examples may include large commercial buildings (shopping malls, offices, hospitals, airports, or schools), industrial and manufacturing applications, transportation systems, security and surveillance gates, and so on. Effective cable length, what we finally get is only about 90 m for horizontal runs because a good general rule during installation is to leave 10 m for the patch cabling. This restricted reach can severely limit the viable locations where system designers and implementers may want to operate a remote IP-enabled device. For example, IP surveillance networks behave slightly different than traditional networks. As IP surveillance cameras and network video recorders (NVR) continue to improve, the demand for extended high-data-rate transmission with minimum data loss has become increasingly important in IP surveillance networks. Due to the standard 100-m limitation of Ethernet, many network installers and system integrators have to rely on Ethernet extender solutions to deploy IP surveillance networks. Challenges include the additional cost for the Ethernet extender and also the need to ensure that the Ethernet extender solutions purchased can withstand high frequencies, large data packet transmission, and high-power consumption to support IP video and mega-pixel transmission.

For any IP-enabled device to function, it requires both Ethernet and power. It is often desirable and required to install a remote IP-enabled device in a location where electrical power is not available. This is where Power-over-Ethernet (PoE) technology supplies a solution. PoE is a mechanism for supplying power to network devices over the same cabling used to carry network traffic. Therefore, no infrastructure upgrade is necessary. PoE technology saves time and cost of installing separate power cabling, AC outlets and wall warts, as well as eliminates the need for a dedicated UPS for individual devices.

The industrial environment is very different from the commercial environment and poses its own set of challenges. Industrial environments often include harsh conditions like higher temperature ranges and voltages, higher noise, mechanical stress, and so forth. Deploying IP network cameras or any other IP-enabled device, whether indoor or outdoor, requires a robust protection scheme to safeguard the equipment against electrical transient threats often encountered at the system level – lightening-induced surge, electro-static discharge (ESD), and electrical fast transient (EFT). All semiconductor devices are susceptible to Electrostatic Discharge (ESD) events. Devices that interface to the outside world are at greater risk than devices that interface with a piece of equipment internally. Since the Ethernet network connection is often very long and typically made of Unshielded Twisted Pair (UTP) cable, the Ethernet interface is also prone to an additional ESD event called Cable Discharge Event (CDE). A CDE during the UTP cable installation can be destructive to the Ethernet PHY device.

Enabled by Texas Instruments' IEEE 802.3-compliant Ethernet PHY transceiver to support 10Base-Te and 100Base-TX protocols, power management devices and high-speed interface protection circuitry, this reference design demonstrates how to design a robust Ethernet communication interface supporting 10/100 Mbps data and power delivery (IEEE 802.3at, Type-1) together over longer cable length for harsh industrial environment with regards to standard compliance to CISPR 22 (EN 55022) Class A and B radiated emission requirements and conducted immunity requirements for ESD according to 61000-4-2 and fast transient burst (EFT) according to IEC61000-4-4.

This design guide addresses component selection, design theory, and test results of the reference design system. The scope of this design guide gives system designers a head-start in integrating TI's devices into their end-equipment systems. This reference design provides a complete set of downloadable documents such as comprehensive design guide, schematic, Altium PCB layout files, Gerber files, bill of materials (BOM) and test results that helps system designers in the design and development of their end-equipment systems. The following subsections describe the various blocks within the reference design system and what characteristics are most critical to best implement the corresponding function.

1.1 Key System Specifications

This reference design targets the following specifications and features as given in 表 1.

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Ethernet PHY	DP83825I - low power 10/100 Mbps Ethernet physical layer transceiver in ultra-small form-factor 24-pin 3 mm × 3 mm QFN package
Cable reach	150 m for data only; 100 m for power + data together
Number of ports	**Power sourcing equipment (PSE) side board:** Two ports - one port to connect with IXIA, the second port with PoE-PSE to inject power; **Powered delivery (PD) side board:** One port with PoE-PD
MAC interface	RMII(Master and Slave mode)
Termination	Integrated MDI and MAC termination resistors
Status LED	Two LEDs (Link and activity with option to configure as PU or PD)
Clock	25-MHz crystal with internal oscillator
USB virtual COM port	Onboard MSP430F5529 MCU to access to PHY registers
PHY configuration	Through-strap resistors
Power	**PSE side board:** 12 V DC; **PD side board:** IEEE 802.3at Type-1 PoE or 12 V DC
Bit error rate (BER)	No more than 10^{-11} with less than a 5% chance of error as per Fast Ethernet Consortium Physical Medium Dependent (PMD) Clause 25 Test Suite #25.2.4
Radiated emission	Pre-compliance tested for CISPR 22 (EN 55022) (30 MHz to 1 GHz) meets both class A and B limits; FCC Part 15 subpart B (30 MHz to 1 GHz) meets both class A and B limits
ESD	Pre-compliance tested for IEC61000-4-2 ESD ±12-kV contact and ±15-kV Air discharge meets criterion B
EFT	Pre-compliance tested for IEC61000-4-4 EFT ±2-kV IO capacitive coupling meets criterion B
Temperature range	Industrial: –40°C to 85°C

2 System Overview

2.1 Block Diagram

図 1 shows the system block diagram for the TIDA-010046 reference design. To demonstrate combined power and networking over longer Ethernet cable, the major building blocks of this reference design system are:

Network traffic generator: IXIA network emulator tool

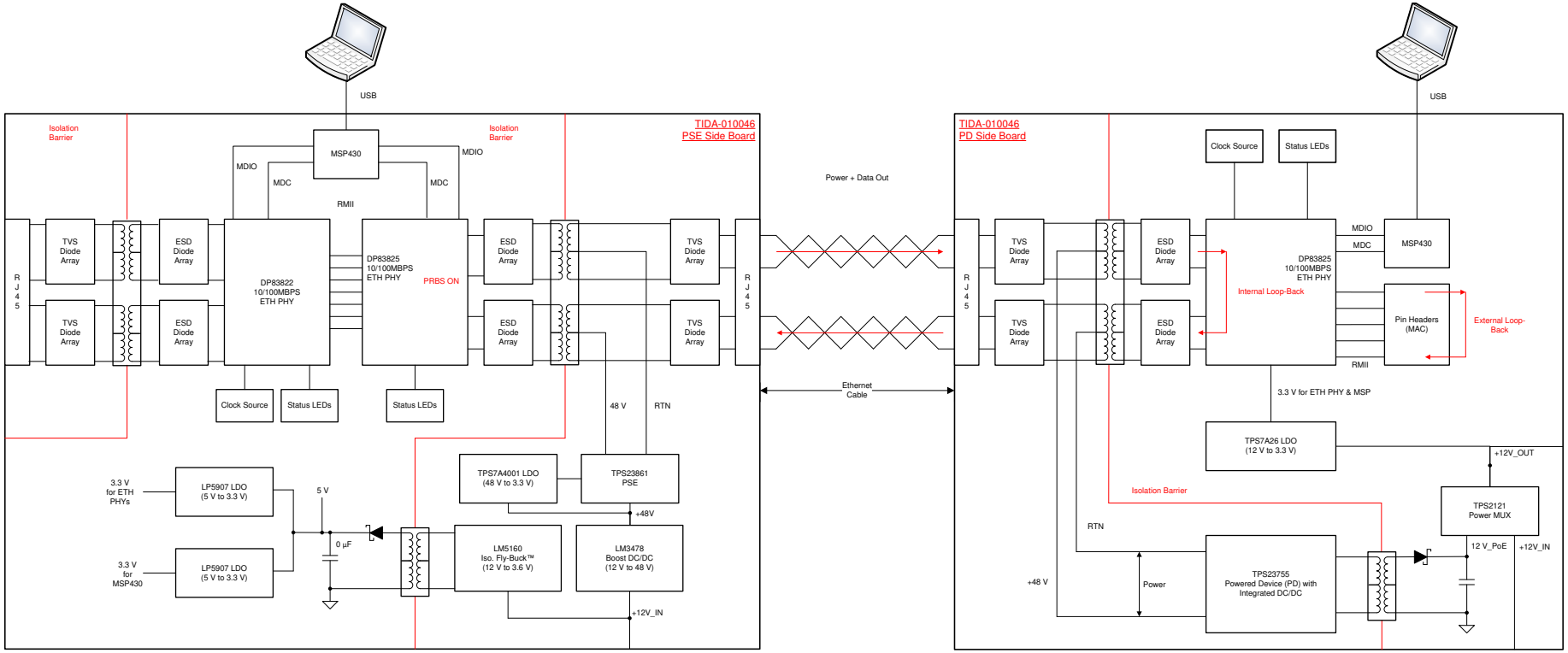
PSE Side Board or Board-1: Since this board comprises two Ethernet PHYs (DP83822I and DP83825I) connected in RMII back-to-back mode and an IEEE 802.3at Type-1 compliant (15.4 W) PSE (TPS23861), it functions as a PoE Ethernet extender. The PSE is the network PoE element that injects power onto an Ethernet cable. It may also be an endspan device, such as a PoE-enabled switch, or a single-port or multi-port midspan PoE injector located between the switch and the PD.

PD Side Board or Board-2: This board contains an IEEE 802.3at Type-1 compliant PD (TPS23755) and one Ethernet PHY (DP83825I) to receive power and data both over Ethernet cable. It could be a PoE-enabled IP phone, a wireless access point, IP network camera or any other IP device that requires power.

Ethernet cable: Up to 150 m

Laptop: USB-2-MDIO serial management GUI based tool runs on laptop that allows access to the MDIO status and control and configuration registers of Texas Instruments' Ethernet PHYs.

図 1. TIDA-010046 System Block Diagram



The IXIA network emulator generates the network traffic that is pushed in to the data input port through RJ45 connector (J9) of the PSE side board. These Ethernet packets are received by the Ethernet PHY DP83822I device , which is connected in RMII back-to-back mode (repeater mode) with another Ethernet PHY DP83825I device. The PSE side board has a local MCU for USB-2-MDIO conversion.

Both Ethernet PHYs (DP83822I and DP83825I) share the common serial management interface (SMI) providing access to the internal registers of the PHY for configuration and status information. Therefore, to distinguish between Ethernet PHYs, the DP83825I and DP83822I devices are assigned different PHY address – 00 and 01, respectively, which is determined by latching the PHY address configuration pins during the power-up or hardware reset. In repeater mode or RMII back-to-back mode, one Ethernet PHY acts as a RMII master and the other Ethernet PHY as RMII slave.

In this reference design, the DP83822I device is made RMII slave and the DP83825I device as RMII master. In RMII slave mode, a 50-MHz clock input must be supplied to the DP83822I device on XI pin that comes from the clock output of the DP83825I device. The Ethernet packets received by the DP83822I device are sent over the RMII to the DP83825I device, which are then transmitted out from the RJ45 connector (J8) over a 150-m Ethernet cable after injecting power to the PD side board.

The PSE side board is equipped with the necessary circuitry to inject PoE, which includes a boost converter (LM3478) to generate 48-V DC from 12-V DC input supply and a PoE-PSE device. The TPS23861 device is an IEEE 802.3at quad port PSE controller. However, this reference design needs only one PSE port and other ports are terminated properly as per device recommendations. The TPS23861 device automatically detects PDs that have a valid signature, determines power requirements according to classification, and applies power.

On the PD side board, the power is received by the TPS23755 IEEE 802.3at PoE-PD device with an integrated Flyback DC/DC converter generating isolated 12-V DC as an input to point-of-loads (POLs) power supplies and data is received by the DP83825I Ethernet PHY. The received network traffic is then looped-back either internally from the DP83825I device or externally to the PSE side board. From there, loopback packets finally reach the IXIA tool where they are compared with the generated packet for successful reception. There are several loopback options within the DP83825I device that test and verify various functional blocks within the PHY. Enabling loopback modes allow for in-circuit testing of the digital and analog data paths.

The DP83825I device may be configured to any one of the near-end loopback modes or to the far-end (reverse) loopback mode. MII Loopback is configured using the Basic Mode Control Register (BMCR, address 0x0000). All other loopback modes are enabled using the BIST Control Register (BISCR, address 0x0016).

2.2 Design Considerations

2.2.1 Ethernet Physical Layer Transceiver (PHY)

The standard 100-m limitation of Ethernet might severely limit the viable locations where system designers and implementers want to operate a remote IP-enabled device. IP surveillance networks should be able to withstand high frequencies and large data packet transmission with minimum data loss to support IP video and mega-pixel transmission. The IP network cameras are becoming more compact and are always a space-critical application. In this reference design, it is necessary to use a 10/100 Mbps Ethernet PHY that can support a longer cable beyond the standard Ethernet distance limitation of 100 m (328 feet) in a small form-factor at a lower cost and lower power consumption.

This reference design is based around the DP83825I device, which is an ultra-small form factor, very low power Ethernet physical layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASE-TX Ethernet protocols. It supports up to 150 m reach over CAT5e cable. The DP83825I device interfaces directly to twisted pair media via an external transformer. It interfaces to the MAC layer through RMII both in Master and Slave mode and it provides 50-MHz output clock in RMII master mode. This clock is synchronized to MDI derived clock to reduce the jitter in the system.

2.2.2 Power-over-Ethernet (PoE)

For any IP-enabled device to function, it requires both Ethernet and power. It is often desirable and required to install a remote IP-enabled device in a location where electrical power is not available. This is where PoE technology supplies a solution. PoE is a mechanism for supplying power to network devices over the same cabling used to carry network traffic. Therefore, no infrastructure upgrade is necessary. PoE technology saves time and the cost of installing separate power cabling, AC outlets and wall warts, as well as eliminating the need for a dedicated UPS for individual devices. PoE can enable fast installation and deployment, and maximum reliability for current IP-based networks. As PoE changes to meet growing technology and application requirements, it is being categorized by classes. PoE devices, on the other hand, are classified by type depending on their power requirements. The difference between PoE “types” and “classes” can sometimes cause confusion when talking about PoE applications and capabilities. IEEE PoE standards provide for signaling between the PSE and PD. PSEs are devices (such as switches) that provide power on the network cable. PDs are the devices powered by a PSE: wireless access points, IP surveillance cameras, VoIP phones, and so forth. In this reference design, the PSE and PD must demonstrate reliable power delivery along with data communication over the Ethernet cable.

This reference design uses the TPS23861 device as PoE-PSE and the TPS23755 device as PoE-PD. The TPS23861 device is an easy-to-use, flexible, IEEE802.3at PSE solution. The TPS23861 device automatically detects PDs that have a valid signature, determines power requirements according to classification and applies power. Two-event classification is supported for Type-2 PDs. The TPS23861 device supports DC disconnection and the external FET architecture allows designers to balance size, efficiency, and solution cost requirements. The TPS23755 device combines a PoE PD interface, a 150-V switching power FET, and a current-mode DC/DC controller optimized for flyback topology. The high level of integration along with primary side regulation (PSR), spread spectrum frequency dithering (SSFD), and advanced startup makes the TPS23755 device an ideal solution for size-constrained applications. The PoE implementation supports the IEEE 802.3at standard as a 13-W, Type 1 PD.

2.3 Highlighted Products

The EMC Compliant 10/100 Mbps Ethernet PHY reference design with IEEE 802.3at Type-1 (≤ 12.95 W) PoE-PD features the following devices:

PSE side board (Board-1):

- TPS23861: Quad IEEE 802.3at Power-Over-Ethernet PSE controller
- DP83825I: Low-power 10/100 Mbps Ethernet physical layer transceiver
- DP83822I: Robust low-power 10/100 Ethernet physical layer (PHY) transceiver
- ESDS312: 3.6-V Data-line surge and 30-kV ESD protection diode array
- TPS7A2633: 500-mA, 18-V, low-I_Q low-dropout (LDO) linear regulator with power good
- MSP430F5529: 25-MHz MCU with integrated USB PHY, 128KB Flash, 8KB RAM, 12-bit, 14-channel ADC, 32-bit hardware multiplier
- LM3478: 2.97-V to approximately 40-V wide-input range Boost, SEPIC, Flyback DC/DC Controller
- LP5907: 250-mA ultra-low-noise, low-I_Q low-dropout (LDO) linear regulator
- LM5160: Wide input 65-V, 2-A synchronous buck, Fly-Buck™ converter
- TPS7A4001: 100-V input, 50-mA, single output low-dropout linear regulator

PD side board (Board-2):

- TPS23755: IEEE 802.3at PoE PD with no-opto flyback DC/DC controller
- DP83825I: Low-power 10/100 Mbps Ethernet physical layer transceiver
- ESDS312: 3.6-V, data-line surge and 30-kV ESD protection diode array
- TPS2121: 2.7–22 V, 56-mΩ, 4.5-A, priority power MUX with seamless switchover
- TPS7A26: 500-mA, 18-V low-I_Q low-dropout (LDO) linear regulator with power good
- MSP430F5529: 25-MHz MCU with integrated USB PHY, 128KB Flash, 8KB RAM, 12-bit, 14-channel ADC, 32-bit hardware multiplier

For more information on each of these devices, see their respective product folders at www.ti.com.

2.4 System Design Theory

2.4.1 Reduced Media Independent Interface (RMII)

For space-critical designs, the DP83825I 10/100 Mbps single port Physical Layer device incorporates the low pin count Reduced Media Independent Interface (RMII) as specified in the RMII specification. The RMII provides a lower pin count alternative to the IEEE 802.3 defined Media Independent Interface (MII) for connecting the DP83825I PHY to a MAC or another PHY in back-to-back or repeater mode in 10/100 Mbps systems. It allows the designer to minimize the cost of the system design while maintaining all the features of the IEEE 802.3 specification. The Ethernet standard (IEEE 802.3u) defines the MII with 16 pins per port for data and control (8 data lines and 8 control signals). The RMII specification reduces the data interfaces from 4-bit data to 2-bit data. In addition, control is reduced to 3 signals. Thus, the total signal connection is reduced to 7 pins (8 pins if RX_ER is required by the MAC).

This reference design does not include a media access controller (MAC) on PD side board. Therefore, the RMII signals of the DP83825I device terminate at pin header J6 for RMII external loopback. Since the RMII transmit and receive signals are synchronous to the same clock, it is possible to implement a remote loopback using external connections. This operation allows diagnostic testing where it may be desirable to receive data on the physical media and loop that data back to the transmitter, providing a remote loopback for the far-end link partner. The following connections need to be made external to the DP83825 device:

- Connect RXD[1:0] to TXD[1:0]
- Connect RX_DV to TX_EN

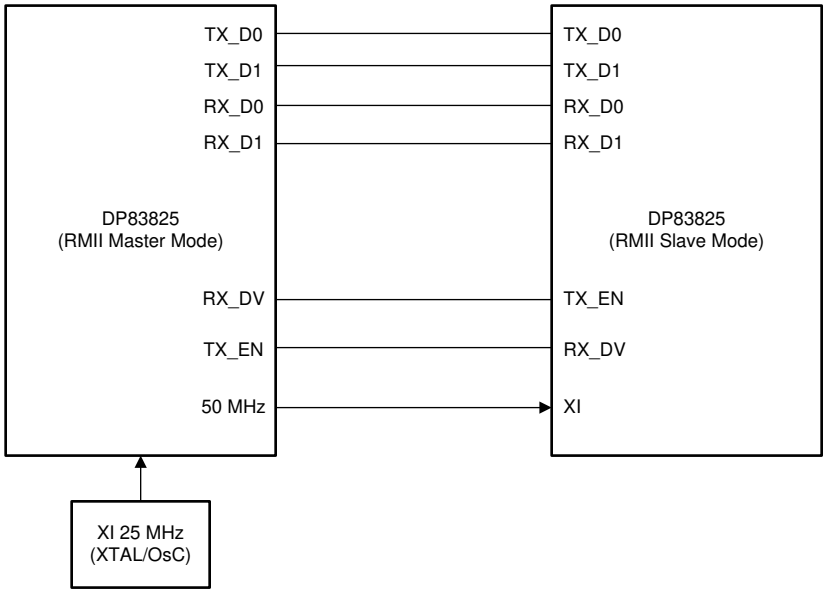
Although RMII is synchronous bus architecture, there are a number of factors limiting signal trace lengths. RMII signals are single-ended signals and the recommendations for reducing the effects of digital I/O noise coupling include:

- With a longer trace, the signal becomes more attenuated at the destination and thus more susceptible to noise interference. Longer traces also act as antennas, and if run on the surface layer, can increase EMI radiation. TI recommends keeping the trace lengths as short as possible; less than two inches is recommended and less than six inches is the maximum.
- Significant differences in the trace lengths can cause data timing issues. Match trace lengths for all RMII signals within ±10 miles.
- As with any high-speed data signal, maintaining impedance and avoiding stubs throughout the entire data path are good design practices. Route RMII signal traces with 50-Ω impedance to ground.
- To reduce the energy of digital signal sources, 50-Ω series termination resistors are recommended for all RMII output signals. Note that the DP83825I device provides integrated 50-Ω signal terminations, making external termination resistors unnecessary.

2.4.2 RMII Repeater Mode

On the PSE side board, the two Ethernet PHYs (DP83822I and DP83825I) are connected in RMII repeater mode. The DP83825I device provides the option to enable repeater mode functionality to extend the cable reach. Two DP83825I devices can be connected in back-to-back mode without the need of any external configuration. It provides a hardware strap to configure the CRS_DV pin of the RMII interface to the RX_DV pin for back-to-back operation. See 図 2 for the RMII pin connection to enable the DP83825 repeater mode.

図 2. RMII Repeater Mode



2.4.3 Hardware Bootstrap Configuration

Hardware bootstrap configuration is a convenient way to configure an Ethernet PHY device into specific modes of operation. Some of the functional pins are used as configuration inputs. The logic states of these pins are sampled during reset and are used to configure the device into specific modes of operation. Because bootstrap pins may have alternate functions after reset is de-asserted, they should not be connected directly to VCC or GND. Pullup and pulldown resistors are required for proper operation. The DP83822I device uses 4-level bootstraps (see 図 3) for hardware configuration while the DP83825I device use 2-level bootstraps (see 図 4). See the *DP83822 Robust, Low Power 10/100 Mbps Ethernet Physical Layer Transceiver* and *DP83825 Robust, Low Power 10/100 Ethernet Physical Layer Transceiver* data sheets for more information regarding bootstrap functionality and configuration.

図 3. Four-Level Bootstrap Configuration (DP83822I)

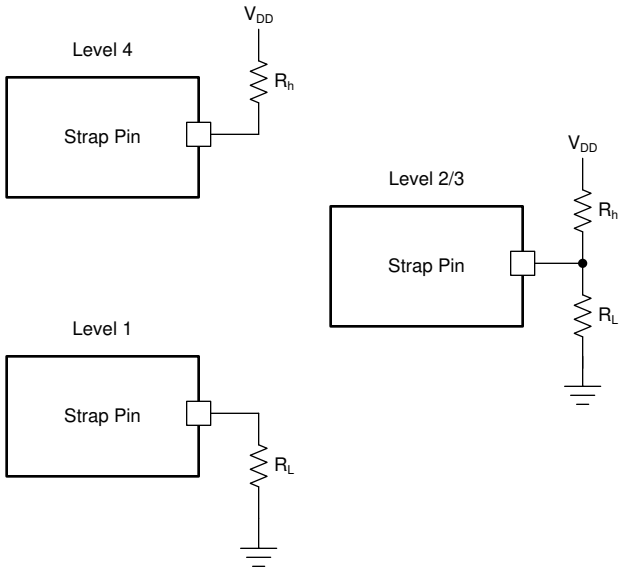
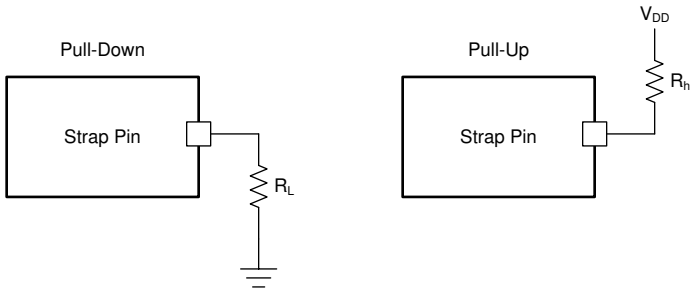


図 4. Two-Level Booststrap Configuration (DP83825I)



All the strap pins have the provision for populating the strap resistors for Ethernet PHYs on both PSE and PD side boards to place the device in to a specific configuration as desired.

2.4.3.1 Hardware Bootstrap Configuration on PSE Side Board

On the PSE side board, two Ethernet PHYs (DP83822I and DP83825I) shares the common serial management bus. To distinguish between the PHYs, each PHY must have a unique PHY address. The PHY address is latched into the device upon power up or hardware reset. The DP83822I device can be configured for any of the 32 possible PHY addresses available through bootstrap configuration. The DP83822I device supports PHY address strapping values 0x0000 (0b00000) through 0x001F (0b11111). By default, the DP83822I device will latch-in the PHY address 0x0001 (0b00001). The DP83825I device can be configured for up to 4 PHY addresses available through bootstrap configuration. By default, the DP83822I will latch-in PHY address 0x00 (0b00). The PHY address can be changed by adding the pullup or pulldown resistors as recommended by the device data sheet. In this reference design system, the default PHY addresses are used simply because both PHYs latch-in different PHY addresses upon power up or hardware reset.

Both Ethernet PHYs (DP83825I and DP83822I) offer two types of RMII operations: RMII Slave and RMII Master. In RMII Slave operation, the PHY operates off of a 50-MHz CMOS-level oscillator connected to the XI pin and shares the same clock as the MAC. In RMII Master operation, the PHY operates off of either a 25-MHz CMOS-level oscillator connected to XI pin or a 25-MHz crystal connected across XI and XO pins. In this reference design, the DP83825I device is configured as RMII master and the DP83822I device as RMII slave. In RMII master mode, the DP83825I device operates off of a 25-MHz crystal connected across XI and XO pins. In RMII Slave operation, the DP83822I device operates off of a 50-MHz reference clock output from the DP83825I device connected to the XI pin. By default, the DP83825I device is in RMII master and provides 50 MHz on pin 2. The DP83822I device should be placed in RMII slave with a 50-MHz reference clock input on the XI pin as highlighted in 表 2. This can be done using pin 26 (RX_DV), which is a strap pin with 9-kΩ pulldown resistor as 図 5 shows. Therefore, the strap function mode-4 should be used as indicated by 表 3. This is achieved by using 2.49 kΩ for R86 (RH) and do not populate R91 (RL) as highlighted in 表 4 and also shown in 図 6.

表 2. DP83822I MAC Interface Configuration

RGMII_EN	RMIIEN	XI_50	DESCRIPTION
0	0	0	MII, 25-MHz reference clock
0	0	1	**Reserved**
0	1	0	RMII, 25-MHz reference clock
0	1	1	RMII, 50-MHz reference clock
1	X	0	RGMII, 25-MHz reference clock
1	X	1	**Reserved**

図 5. DP83822I Bootstrap Circuit for RX_DV Pin

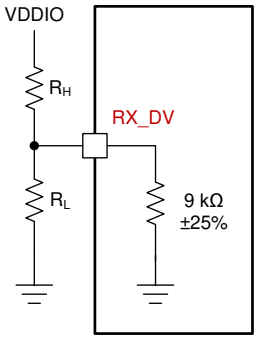


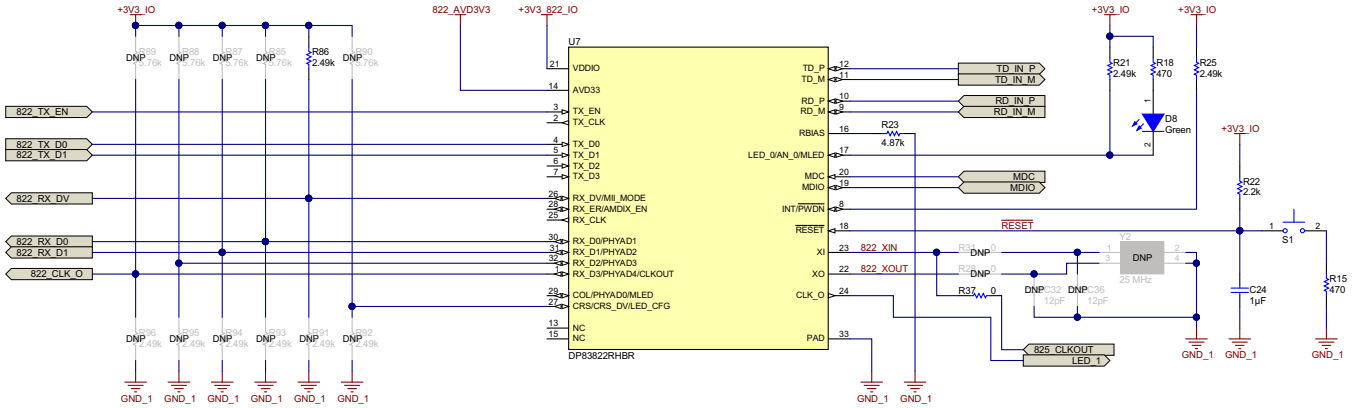
表 3. Mode-4 for 50 MHz on XI and RMII Enable

PIN NAME	PIN #	DEFAULT	STRAP FUNCTION		
			MODE	XI_50	RMII_EN
RX_DV	26	[00]	1 (Default	0	0
			2	1	0
			3	0	1
			4	1	1

表 4. Recommended 4-Level Strap Resistor Ratios for Pulldown Pin Mode-4

MODE	IDEAL R_H (kΩ)	IDEAL R_L (kΩ)
PULLDOWN PINS (9 kΩ)		
1 (Default)	**OPEN**	**OPEN**
2	10	2.49
3	5.76	2.49
4	2.49	OPEN
PULLUP PINS (50 kΩ)		
1	OPEN	1.96
2	13	1.96
3	6.2	1.96
4 (Default)	**OPEN**	**OPEN**

図 6. DP83822I Schematic for Bootstrap Settings on PSE Side Board



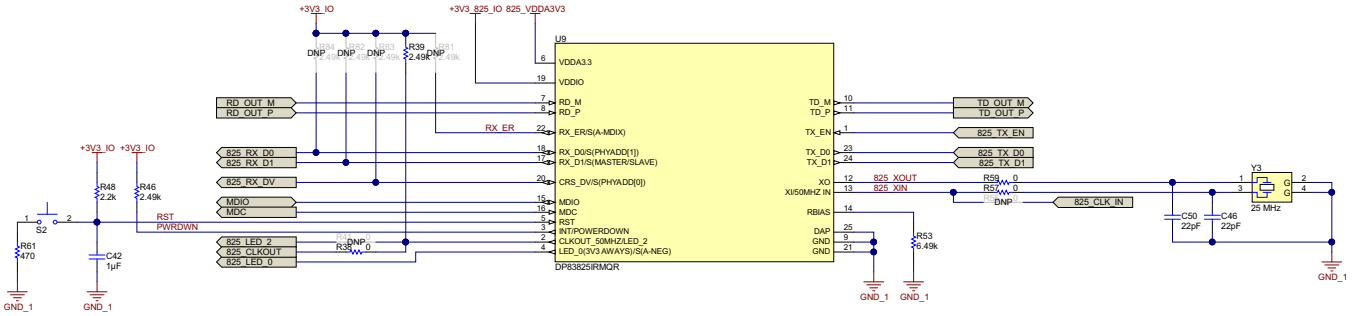
The DP83825I device is connected with the DP83822I device in back-to-back RMII mode (repeater mode). Therefore, configure pin 20 (with default function CRS_DV) as RX_DV for repeater mode. This can be achieved in one of two ways:

- Pullup resistor R39 (= 2.49 kΩ) on strap pin-2 (50MHzOut/LED2/S) as highlighted in 表 5 and also in 図 7.
- Set bit-8 of the 0x302 register

表 5. RMII MAC Mode Strap Table for DP83825I

PIN NAME	STRAP NAME	PIN #	DEFAULT		
RX_D1	Master/Slave	17	0	0	RMII Master Mode
				1	RMII Slave Mode
50MHzOut/LED2	RX_DV_En	2	0	0	Pin 20 is configured as CRS_DV
				1	Pin 20 is configured as RX_DV (for RMII repeater mode)

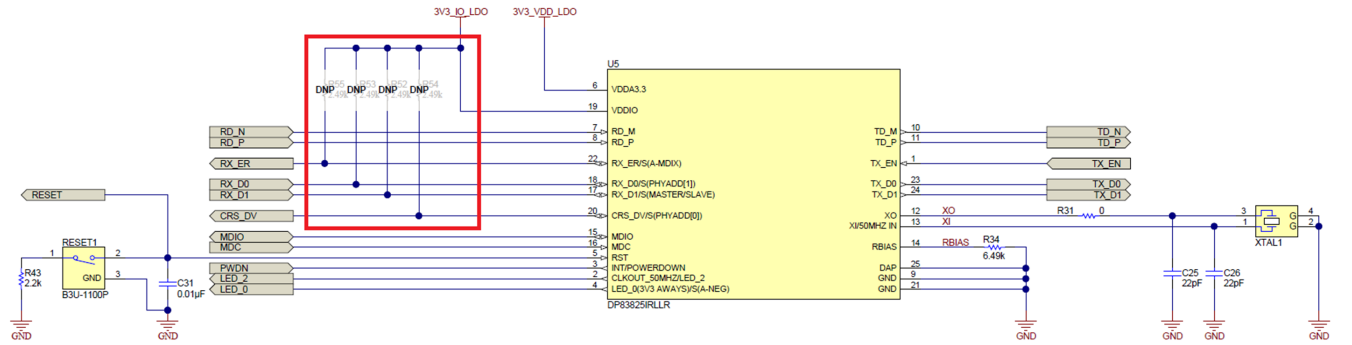
図 7. DP83825 Schematic for Bootstrap Settings on PSE Side Board



2.4.3.2 *Hardware Bootstrap Configuration on PD Side Board*

Since the DP83825I device is the only PHY on the PD side board, it operates in its default RMII master mode. However, all the strap pins have provisions for populating the pullup strap resistors just in case the device configuration needs to be changed as 図 8 shows.

図 8. DP83825I Schematic for Bootstrap Settings on PD Side Board

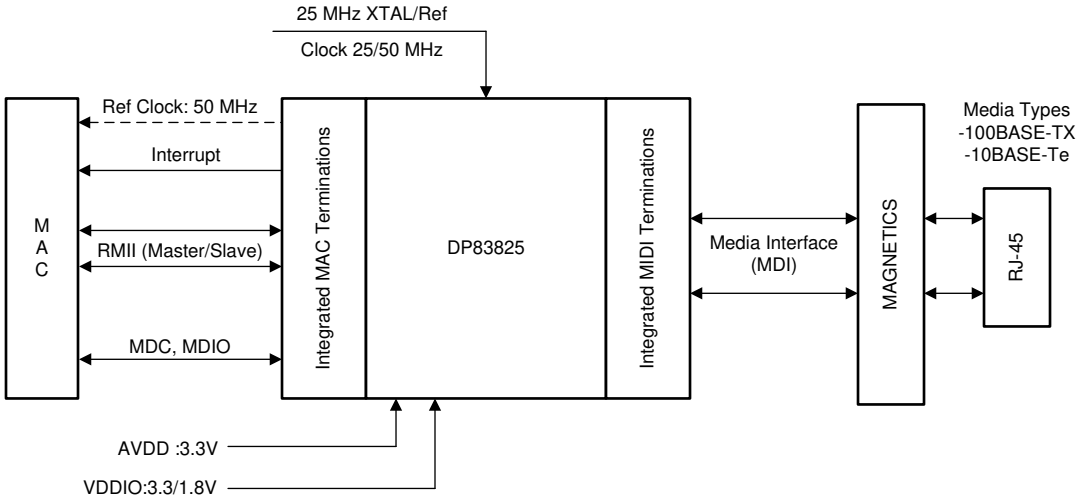


2.4.4 Termination Resistors

The DP83822I device has a built-in adjustable series termination network on MAC interface to eliminate the need for external series termination resistors. The series termination can be adjusted by accessing the IO MUX GPIO control register (IOCTRL Register, 0x0461). MAC impedance control bits [4:1] allow for a range of termination adjustments: 42.5 Ω to 99.25 Ω.

The DP83825I device offers programmable termination impedance for RMII interface and integrated MDI termination resistors as 図 9 shows. These features allow the removal of external series termination resistors. The series termination on the MAC interface can be adjusted by accessing the IO_CFG_Register register (Offset = 0x302). MAC impedance control bits [15:14] allow termination adjustments for either 50 Ω or 25 Ω.

図 9. Integrated Termination Resistors on RMII and MAC Interfaces of DP83825I

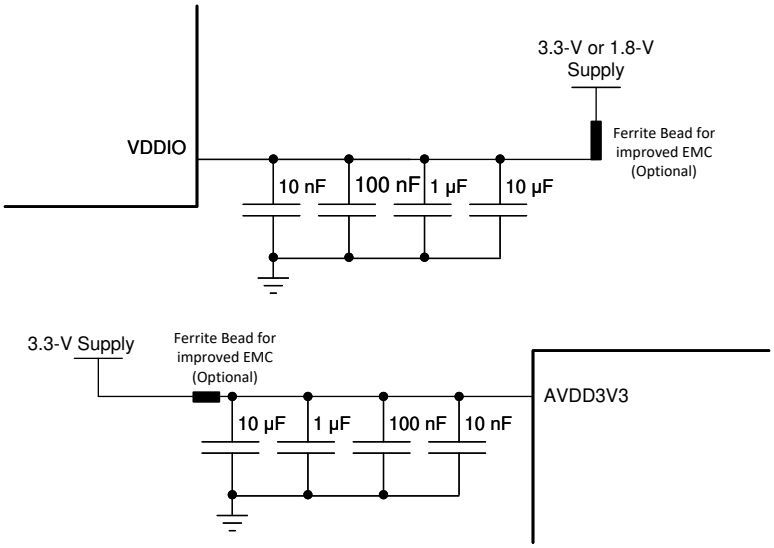


2.4.5 Power and Ground

The device supply pins should be bypassed with low impedance 10-nF, 100-nF, and 1-µF surface mount capacitors. A 10.0-µF capacitor should also be placed near the PHY component for local bulk bypassing between the supply and ground planes. To reduce EMI, place the capacitors as close as possible to the device supply pins, preferably between the supply pins and the vias connecting to the power plane. In some systems, it may be desirable to add 0-Ω resistors in series with supply pins, as the resistor pads provide flexibility if adding EMI beads becomes necessary to meet system-level certification testing requirements as 図 10 shows.

It is also important that the physical size of bead components be chosen to accommodate the current necessary to supply the physical layer device supply pins. See individual component data sheets for component current requirements. Place local bypass components (including capacitors and optionally ferromagnetic beads) between device supply pins and power sourcing vias on the PCB. TI recommends the PCB have at least one solid ground plane and one solid power plane to provide a low-impedance power source to the component. This also provides a low-impedance return path for non-differential digital RMII and clock signals. Ground vias must be placed as close to the ground pins as possible. The DP83825I is capable of operating with a 3.3-V or 1.8-V of I/O supply voltages along with the analog supply of 3.3 V. The DP83825I device needs VDDA3V3 after VDDIO is fully ramped. If power sequencing is not feasible on the customer board, then an external Reset (RST_N) is needed on pin 5 when both power VDDA3V3 and VDDIO supplies are ramped.

図 10. Power Supply Decoupling Recommendation



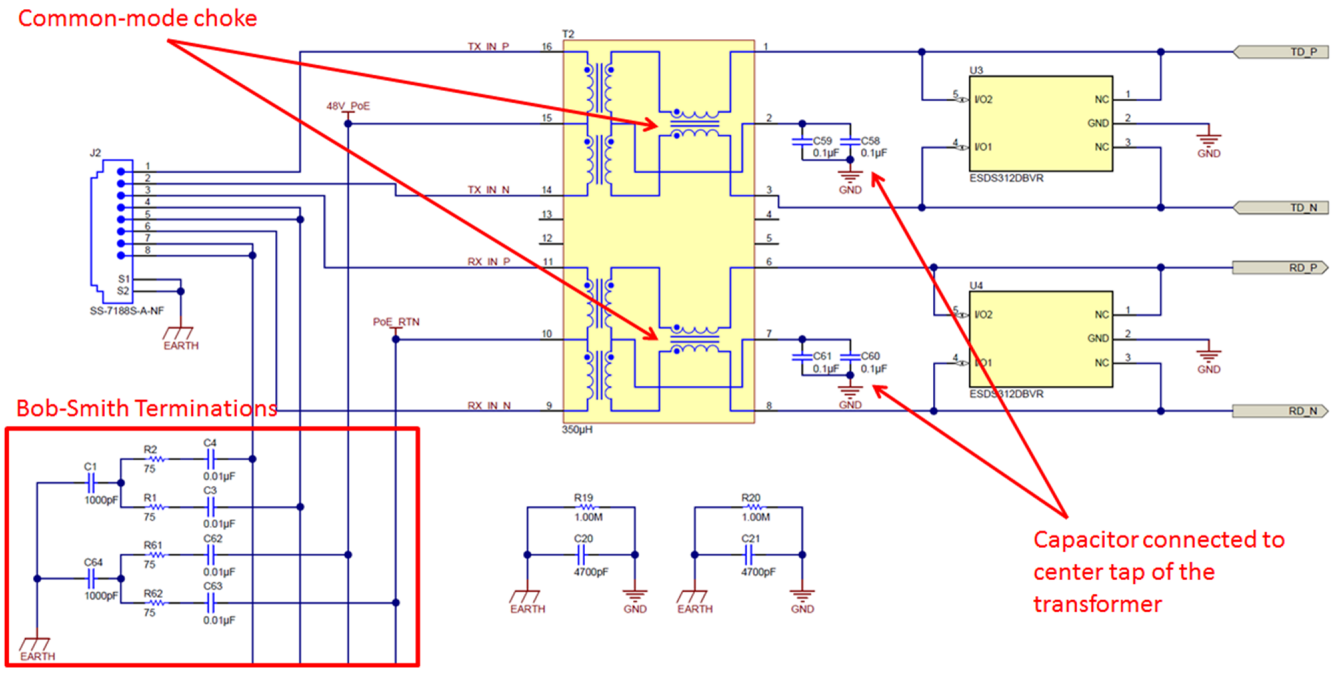
2.4.6 Magnetics

For communication on a local area network (LAN), magnetics provide electrical isolation, signal balancing, common-mode rejection, impedance matching, and EMC improvement. The 10/100Base-T Ethernet utilizes an Unshielded Twisted Pair (UTP) transmission cable consisting of four sets of twisted pairs connected in a balanced configuration. The UTP wiring is prone to pick up noise that leads to conducted and radiated noise emission. Also for human safety, the IEEE specification requires a 10/100BASE-T port to be able to withstand 1,500 VAC at 50 Hz, 60 Hz for 1 minute between ports or from each port to the chassis ground. Transformers simply and easily provide the balanced connection to each pair of a cable, provide a very effective rejection of common-mode signals and inexpensively meet this isolation requirement.

Common-mode rejection is the ability to reject a signal which, referenced to ground, has the same amplitude and phase on both inputs. This signal, which is usually the result of noise or a small impedance mismatch, produces a small differential error voltage at the input terminals of the Ethernet. Subsequently, this error gets amplified right along with the desired communications signal. The magnetics play a major role in knocking down common-mode noise down to an acceptable level. The common-mode rejection of a transformer functions in both signal directions of a port. This common-mode rejection attenuates common-mode signals coming both from the cable to the PHY and also from the PHY to the cable. Reduction of the common-mode signals picked up by the cable from its environment improves the signal-to-noise ratio of the system, thus allowing AFE and DPS inside PHY to more easily recover the data signal and achieve the desired bit error rate. The noise from the board circuits can couple to the sensitive signal traces going from the PHY to the magnetics, coupling equally to both signals of a differential pair and creating common-mode noise. This noise will be attenuated by the magnetics and improves the EMC performance.

The purpose of the transformer with a 1:1 ratio is to create galvanic isolation between the cable and the system. The PHY-side center tap of the transformer should connect through a capacitor to ground, forming a low pass filter with common-mode choke as 図 11 shows. The CMRR cutoff frequency can be changed by common-mode choke selection and through the adjustment of the capacitor. The isolation transformer used in this reference design is the HX1198FNL from Pulse Electronics. The key performance metric affecting the transformer is winding tolerance. Winding tolerances affect amplitude step-up and step-down from the primary to secondary side of the transformer, and should remain within ±2%.

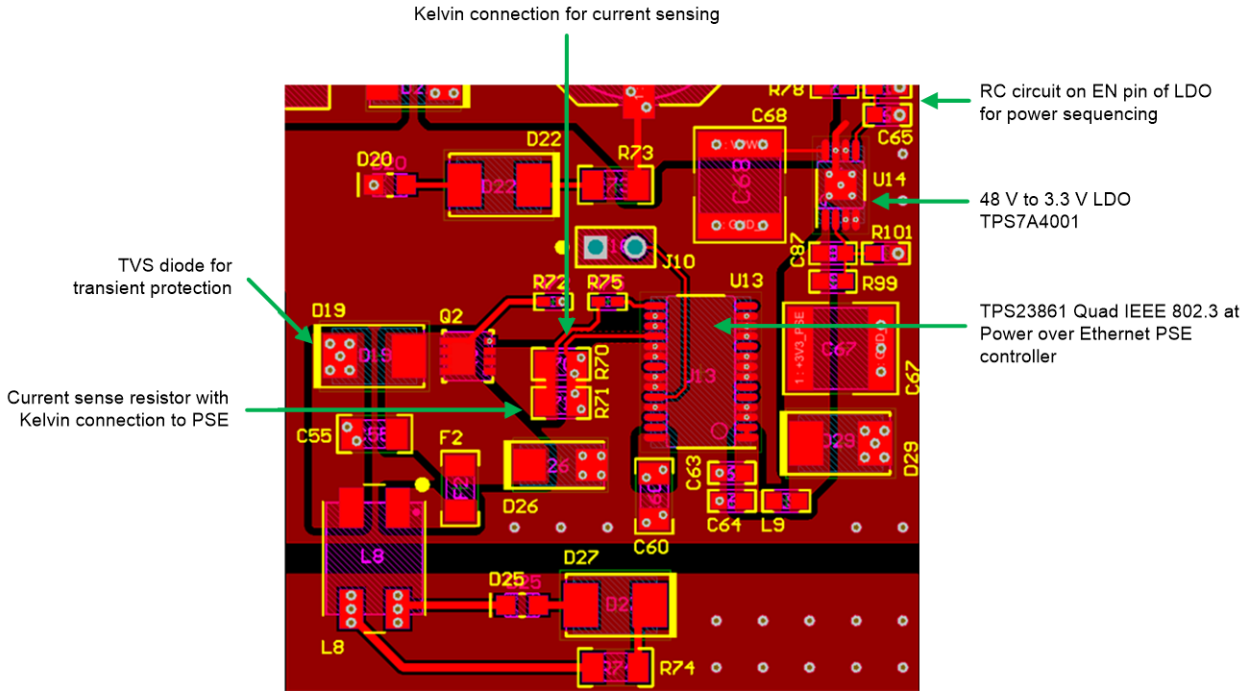
図 11. LAN Magnetics



2.4.7 PoE Power Injector Circuit on PSE Side Board

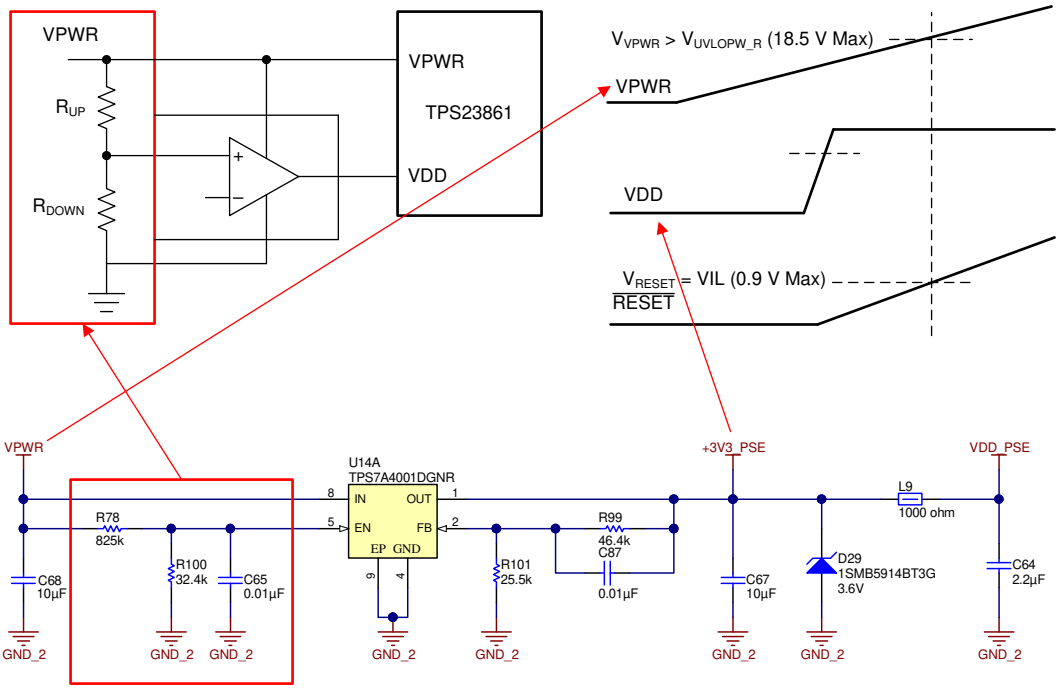
For the TPS23861 PoE-PSE based circuit design for injecting power onto any Ethernet cable for PoE powered loads up to 30 W, refer to the TIDA-00465 - *Single Port, Power-over-Ethernet, Type 2 Auto-Mode PSE Reference Design*. 図 12 shows the board layout for the TPS23861 PoE-PSE device.

図 12. TPS23861 PoE-PSE on PSE Side Board Layout



注: Be sure the VPWR and VDD rails follow the proper power-up sequence. In this reference design, the VPWR starts rising before the VDD rail which is the typical case because the VDD rail is usually derived from the VPWR rail. The VDD rail will turn on when VPWR reaches the externally programmed UVLO of the VDD rail. Also of note in 図 13 is that RESET starts rising when VDD starts rising because the RESET pin is connected to the VDD pin externally. Since only a single TPS23861 device is used in the system, then a TPS7A4001 (LDO) can be used with R78 (RUP) = 825 kΩ and R100 (RDOWN) = 32.4 kΩ. For more details, see the *TPS23861 Power-On Considerations* application report.

図 13. TPS23861 Power On Sequence



2.4.8 PoE-PD Circuit Design on PD Side Board

See TIDA-0010034 for more details about PoE PoE implementation supporting IEEE 802.3at standard as a 13 W, Type 1 PD using the TPS23755 device.

2.4.9 Clock Requirement

The DP83825I device supports an external CMOS-level oscillator source or an internal oscillator with an external crystal. The use of a 25-MHz, parallel, 20-pF load crystal is recommended if a crystal source is desired. 図 14 shows a typical connection diagram for a crystal resonator circuit. Note that the load capacitor values will vary with the crystal vendors. Check with the vendor for the recommended loads. For more details, see the *Selection and Specification of Crystals for Texas Instruments Ethernet Physical Layer Transceivers* application report. Adjust the series resistance value to meet the crystal drive level. The design uses the oscillator circuit to drive a crystal with a maximum drive level of 100 µW. If a crystal is specified for a lower drive level, a current-limiting resistor must be placed in series between XO and the crystal. As a starting point for evaluating an oscillator circuit, if the requirements for the crystal are not known, set the values for CL1 and CL2 at 20 pF. Set R1 at 0 Ω. Specifications for a 25-MHz crystal are listed in 表 6.

図 14. Crystal Oscillator Circuit

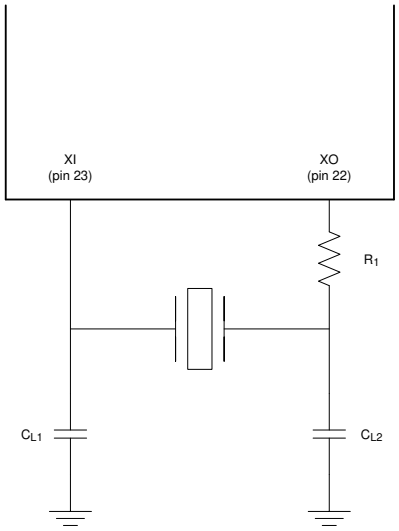


表 6. Crystal Specification - 25 MHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency tolerance	Including operational temperature, aging and other factors	–50		50	ppm
Load capacitance			15	40	pF
ESR				50	Ω

2.4.10 Electrical Transient Immunity

2.4.10.1 Electrical Transient Immunity for PoE

For electrical transient immunity for PoE, see the *Electrical Transient Immunity for Power-Over-Ethernet* application report.

2.4.10.2 Electrical Transient Immunity for Ethernet PHY

The network or Medium Dependent Interface (MDI) connection via transmit (TD+ and TD–) and receive (RD+ and RD–) is ESD protected. This reference design uses a shielded RJ45 connector without an internal isolation transformer. RJ45 is the standard cable used for all the Ethernet and LAN applications. An external isolation transformer is interfaced. The TIDA-010046 design uses the HX1198FNL transformer from Pulse Electronics. The device is a 1:1 transformer with an isolation of 1.5 kV_{RMS} (for 60 seconds).

Based on the application, it may be necessary to connect a common-mode choke along with the isolation transformer. The HX1198FNL device has an integrated common-mode transformer. The network or MDI connection is through the transmit (TX+ and TX–) and receive (RX+ and RX–) differential pair terminals. The transmit and receive terminals connect to a termination network, then to a 1:1 magnetic transformer, then to ESD protection devices and an RJ45 connector.

This reference design uses the ESDS312 as ESD protection diodes in between the isolation transformer and Ethernet PHY. The ESDS312 devices are unidirectional TVS ESD protection diode arrays for Ethernet, USB and general purpose data line surge protection up to 25 A (8/20 µs) . The ESDS312 devices are rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4). The devices features a 4.5-pF IO capacitance per channel making it ideal for protecting high-speed interfaces such as 10/100/1000 Mbps Ethernet. Another reason for using ESDS312 is its low surge clamping voltage 6.5 V at 25-A IPP.

2.5 Board Design Guideline

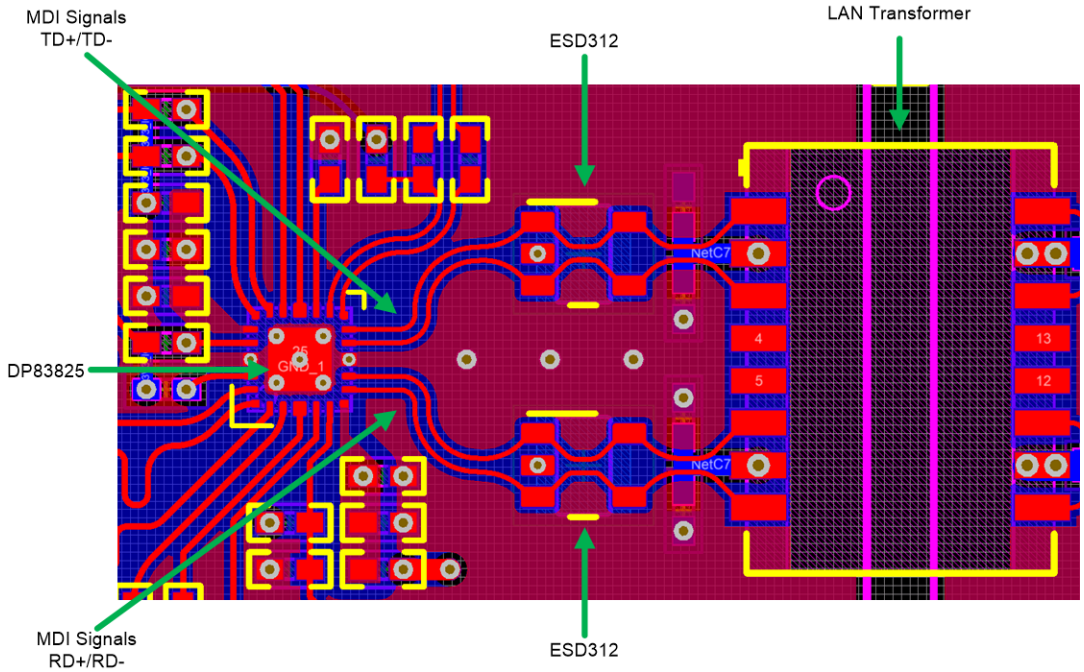
This section provides approaches for optimal board design.

2.5.1 MDI Connections

2.5.1.1 MDI Connections Between Ethernet PHY and Isolation Transformer

The MDI connection is via transmit (TD+/TD–) and receive (RD+/RD–) differential pair pins. These differential pairs connect to a termination network, ESD protection devices, then to 1:1 magnetics (transformer) as 図 15 shows.

図 15. MDI Connections Between Ethernet PHY and Isolation Transformer



General MDI layout guidelines and key design recommendations for reduced EMI:

- Depending on the PHY device, parallel termination might be needed for each of the MDI differential signal pairs. The termination impedance is typically 100 Ω differentially.
  - Newer devices like the DP83825I include integrated MDI termination so no external termination resistors are required.
  - For the DP83822 device, place the 49.9 Ω, 1% resistors, and 0.1-µF decoupling capacitor, near the TD+/TD– and RD+/RD– pins and via directly to the AVDD plane as 図 16 shows.
  - To reduce the crosstalk interference on signals, keep differential MDI network signals physically

separated from single-ended digital signals. Place digital signals far away from the analog traces to help maintain signal integrity. A good general rule to follow is that no digital signal should be located within 300 mils (7.5 mm) of the differential pairs.

- MDI signals are differential. Within the pairs (for example, TD+/TD– or RD+/RD–) the trace lengths should run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common-mode noise and increased EMI. To ensure data integrity, match the trace length within ±50 mils, see 表 7 through 表 9.
- The separation between the TD+/TD– and the RD+/RD– differential pairs must be at least 0.5 mm. It is best to separate them with a ground plane.
- Route single-ended traces with 50-Ω impedance to ground, whereas, the differential traces are routed with 100-Ω controlled impedance. Many online tools are available to calculate controlled impedance for micro strip and stripline traces. For more details, see the *AN-1469 PHYTER Design and Layout Guide* application report.
- Route MDI traces to the transformer on the same layer.
- Never use 90° traces. Use 45° angles or radius curves in traces.
- Keep PCB trace lengths as short as possible. Keeping the traces as short as possible also helps reduce capacitive loading.
- Avoid supplies and ground beneath the magnetics.
- Do not overlap the circuit ground and chassis ground planes. Keep chassis ground and circuit ground isolated by turning chassis ground into an isolated island by leaving a gap between the planes. Connecting a 1206 (size) capacitor between chassis ground and circuit ground is recommended to avoid floating metal. Capacitors less than 0805 (size) can create an arching path for ESD due to a small air-gap.
- Do not run signal traces such that they cross a plane split as 図 17 shows. A signal crossing a plane split may cause unpredictable return path currents and would likely impact signal quality as well, potentially creating EMI problems.
- Avoid stubs on all signal traces, especially the differential signal pairs (see 図 18).

図 16. DP83822I TPI Network Interface

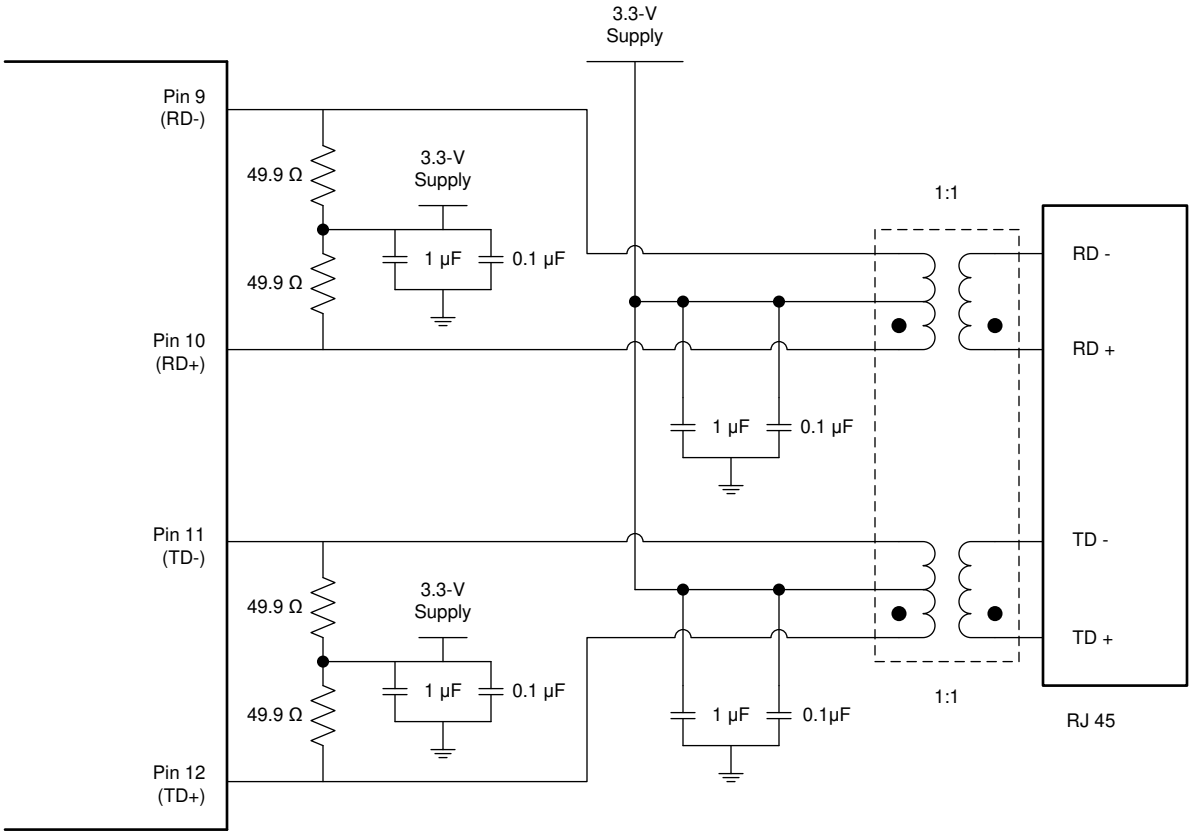


表 7. Differential Signal Trace Length From DP83822I Ethernet PHY to Magnetics on PSE Side Board

MDI DIFFERENTIAL PAIR NAME	TRACE LENGTHS FROM DP83822I ETHERNET PHY TO MAGNETICS ON PSE SIDE BOARD
TD_IN_P	833.060 mils
TD_IN_N	831.054 mils
RD_IN_P	790.948 mils
RD_IN_N	793.119 mils

表 8. Differential Signal Trace Length from DP83825I Ethernet PHY to Magnetics on PSE Side Board

MDI DIFFERENTIAL PAIR NAME	TRACE LENGTHS FROM DP83825I ETHERNET PHY TO MAGNETICS ON PSE SIDE BOARD
TD_OUT_P	600.481 mils
TD_OUT_M	607.136 mils
RD_OUT_P	594.252 mils
RD_OUT_M	594.170 mils

表 9. Differential Signal Trace Length from DP83825I Ethernet PHY to Magnetics on PD Side Board

MDI DIFFERENTIAL PAIR NAME	TRACE LENGTHS FROM DP83825I ETHERNET PHY TO MAGNETICS ON PD SIDE BOARD
TD_P	646.238 mils

表 9. Differential Signal Trace Length from DP83825I Ethernet PHY to Magnetics on PD Side Board (continued)

MDI DIFFERENTIAL PAIR NAME	TRACE LENGTHS FROM DP83825I ETHERNET PHY TO MAGNETICS ON PD SIDE BOARD
TD_N	650.510 mils
RD_P	646. 203 mils
RD_N	644.074 mils

図 17. Differential Signal Pair and Plane Crossing

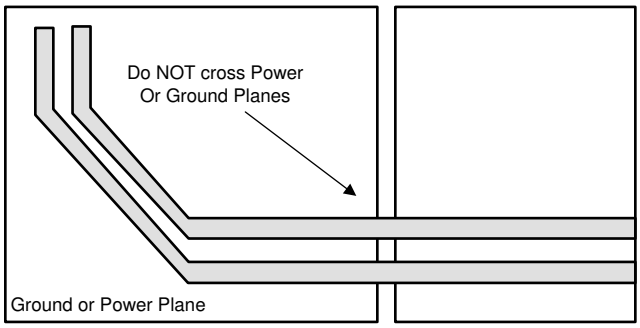
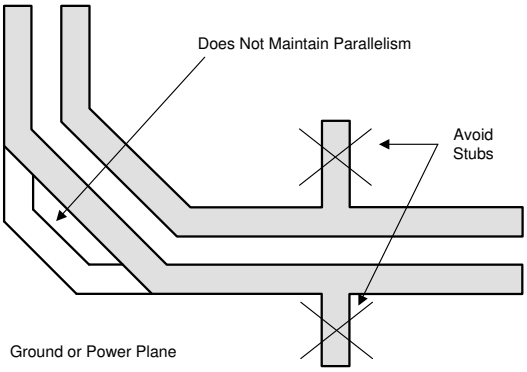


図 18. Differential Signal Traces



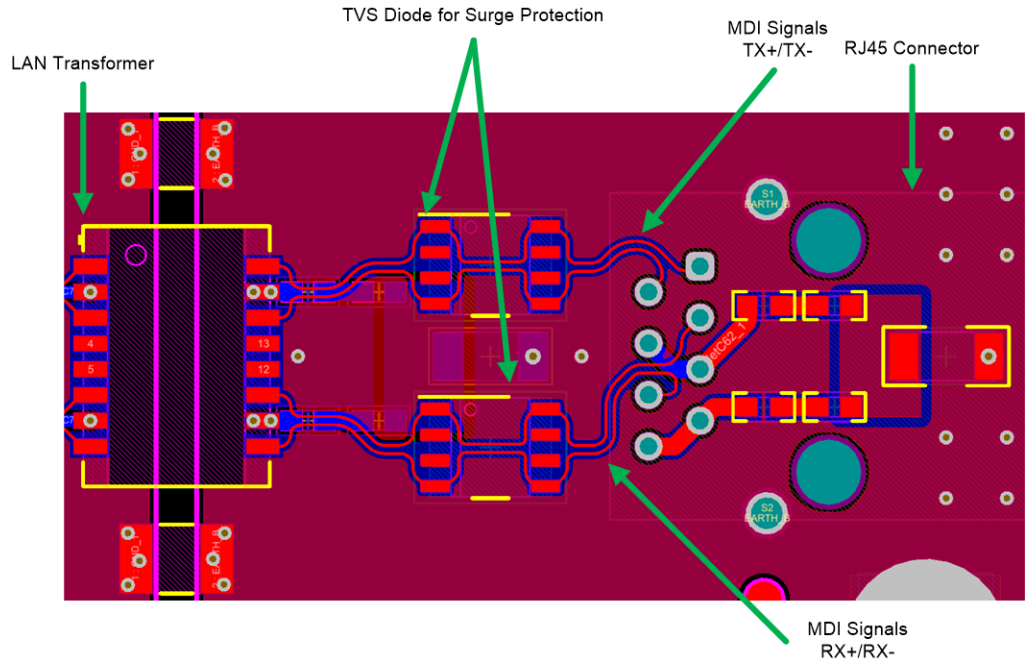
2.5.1.2 MDI Connections Between Isolation Transformer and RJ45 Connector

図 19 shows the MDI connections between magnetics and the RJ45 connectors.

For non-PoE ports like J9 on the PSE side board, the center tap of the isolated winding has Bob-Smith termination through a 75-Ω resistor and a 1000-pF capacitor to chassis ground. The termination capacitor should be rated to a voltage of at least 2-kV. The “Bob Smith” termination is used to reduce noise resulting from common-mode current flows. The initial ESD, EFT transient hits circulate through Bob-Smith terminations to chassis ground.

PoE enables ports like J8 on the PSE side board and J2 on the PD side board, the Bob-Smith termination network should be modified to block the DC common-mode voltage between pairs from creating a large current through the termination resistors, which would blow up the termination resistors. This is done by inserting 10-nF blocking capacitors in series with the termination resistors.

図 19. MDI Connections Between Isolation Transformer and RJ45 Connector



For EMI considerations, the following guidelines were used for this section of the circuit:

- Congregate the input-related components toward the RJ45 input connector.
- Use a metal shielded RJ45 connector, and connect the shield to chassis ground.
- Use of magnetics with integrated common-mode choke is preferred.
- The distance between the magnetic module and the RJ45 jack is the most critical and must always be as short as possible (must be less than one inch).
- Never use 90° traces. Use 45° angles or radius curves in traces.
- The separation between the TX+/TX– and the RX+/RX– differential pairs must be at least 0.5 mm. It is best to separate them with a ground plane.
- MDI signals are differential. Within the pairs (for example, TX+/TX– or RX+/RX–) the trace lengths should be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common-mode noise and increased EMI. To ensure data integrity, the trace length should be matched within ±50 mils, see 表 10.
- Do not overlap the circuit and chassis ground planes, keep them isolated. Connect chassis ground and system ground together using two size 1206 0-Ω resistors across the void between the ground planes on either side of the RJ45. These resistors can be removed or replaced with alternative components (that is, capacitors or EMI beads) during system level certification testing, if necessary.
- For non-PoE ports, include the 75-Ω as Bob Smith cable terminations at the center tap of the isolated winding as 図 20 shows.
- For PoE enabled ports, include the 75-Ω and 0.01-µF as Bob Smith cable terminations on the input power lines at the center tap of the isolated winding as 図 21 and 図 22 show.
- Include the 1000-pF, 2-kV bypass capacitor to tie the Bob-Smith cable terminations to a copper plane (shield) which is commonly referred to as the Bob Smith plane (BS plane). Connect a 1000-pF, 2-kV bypass capacitor to the Bob Smith plane using dedicated vias located directly at the capacitor

termination.

- To maintain 1500-V_{RMS} isolation between two adjacent layers of a NEMA FR-4 multi-layer PCB, a minimum of 15 mils isolation thickness is recommended. This provides a safe margin for high-potential requirements. The isolation thickness used in this design is 94 mils.
- Use a number of perimeter vias to stitch the top and bottom layers of the Bob Smith plane together.
- Additional capacitors are required to interconnect chassis ground and signal ground. The suggested technique is to use plane coupling capacitor values (for example, from 1000 pF to 4700 pF). Depending on available board space, place one set of capacitors on each side of the Ethernet magnetic.

表 10. Differential Signal Trace Length From Magnetics to RJ45 Connector on PSE Side Board

MDI DIFFERENTIAL PAIR NAME	TRACE LENGTH FROM MAGNETICS TO RJ45 CONNECTOR ON PSE SIDE BOARD
TX_OUT_P	1106.097 mils
TX_OUT_M	1063.192 mils
RX_OUT_P	1236.934 mils
RX_OUT_M	1202.549 mils

図 20. Recommended 10/100 Mbps Twisted Pair Interfaces and Bob Smith Termination for non-PoE Port as on PSE Side Board

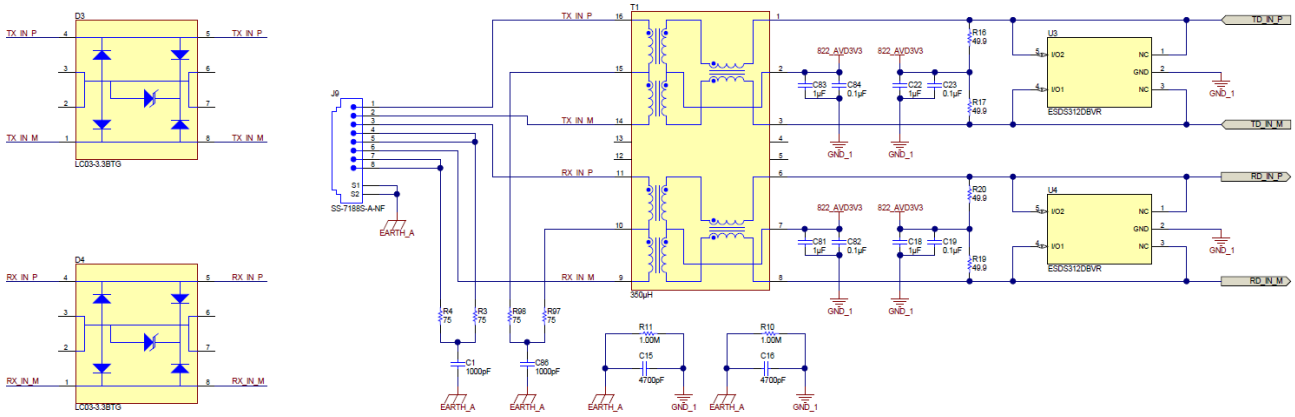


図 21. Recommended 10/100 Mbps Twisted Pair Interfaces and Bob Smith Termination for PoE Port as on PSE Side Board

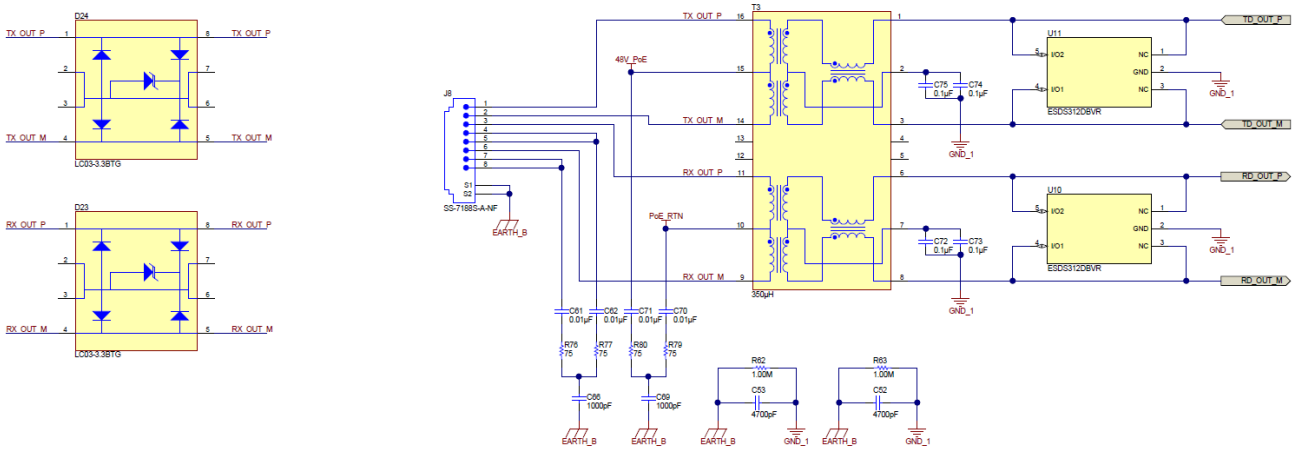
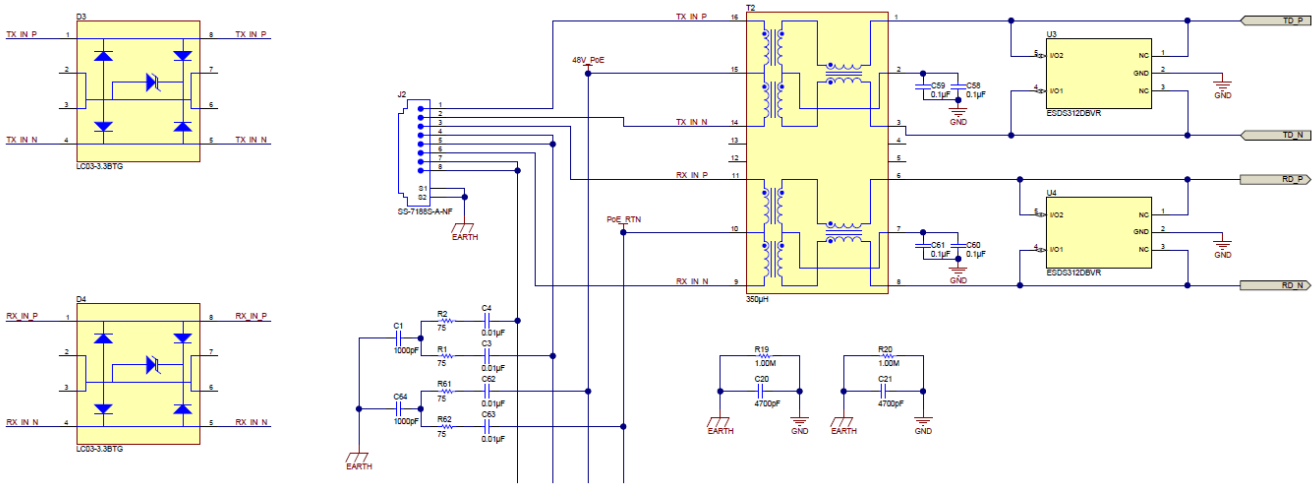


図 22. Recommended 10/100 Mbps Twisted Pair Interfaces and Bob Smith Termination for PoE Port as on PD Side Board



3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

3.1.1.1 PSE Side Board - Top and Bottom Views

図 23 shows the top view of the PSE side board. All the ICs and most of the discrete components are placed on the top side only, except the RJ45 connectors as shown in 図 24, which are placed on the bottom side of the board for easy and straight routing of MDI signals without any crisscross.

図 23. PSE Side Board (Top View)

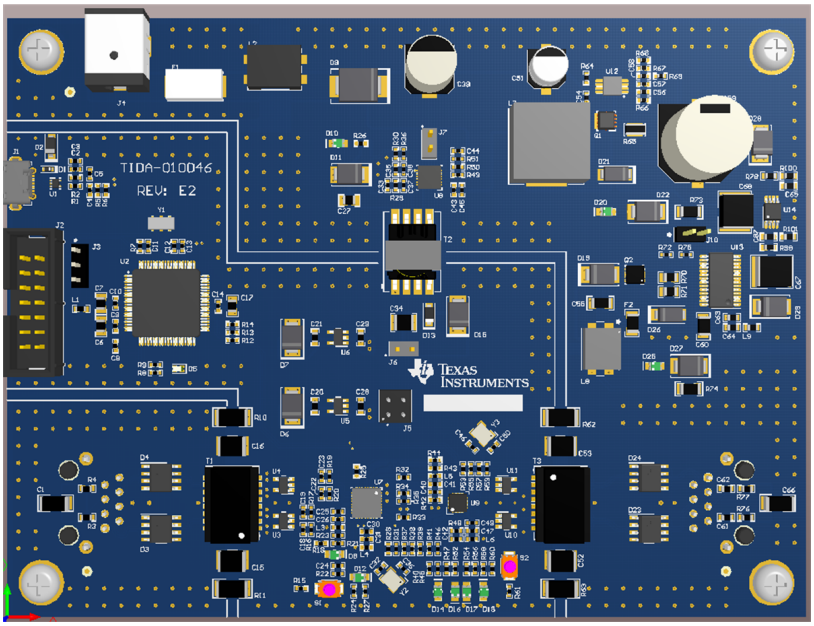
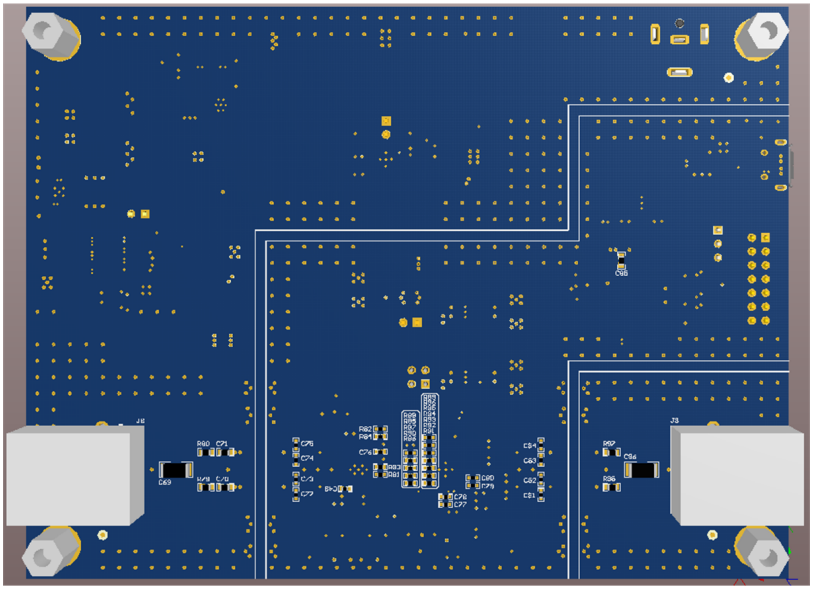


図 24. PSE Side Board (Bottom View)



3.1.1.2 PD Side Board - Top and Bottom Views

図 25 and 図 26 show the top and bottom view of the PD side board respectively.

図 25. PD Side Board (Top View)

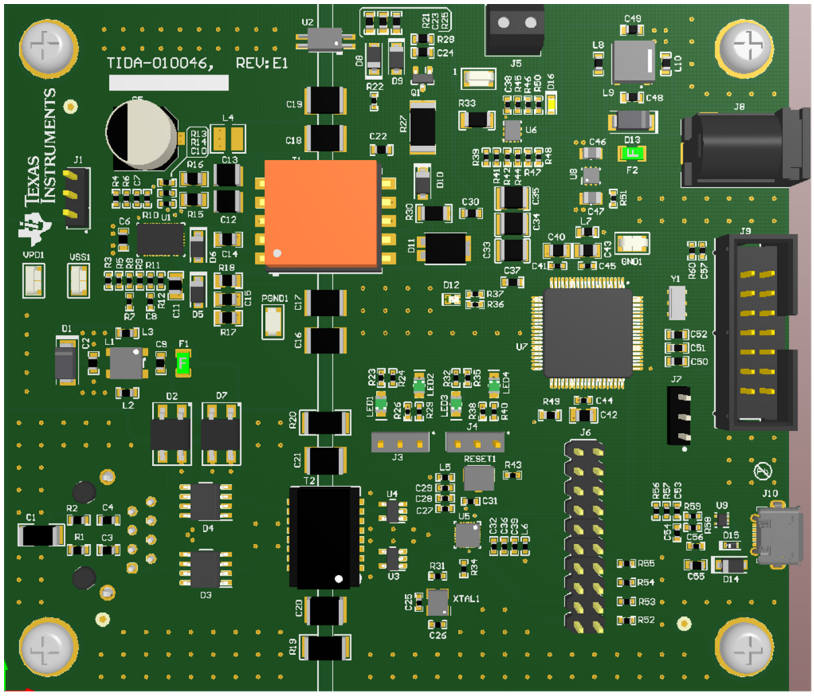
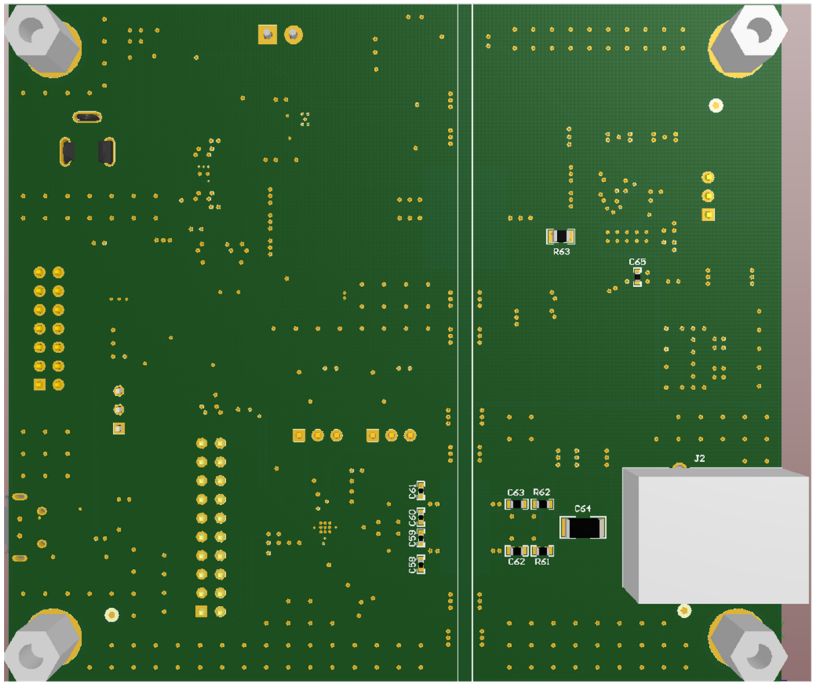


図 26. PD Side Board (Bottom View)



3.1.2 Software

The onboard MSP430F5529 comes pre-programmed and ready to use. When using this reference design hardware for the first time on a Microsoft® Windows® 7 (or above) PC, the MSP430 drivers and the USB-2-MDIO software utility must be installed. The USB-2-MDIO software can be used for accessing registers.

3.1.2.1 MSP430 Driver

The MSP430 drivers are required to properly connect the onboard MSP430F5529 or MSP430 LaunchPad™ to a user's computer. Download the latest MSP430 drivers from http://www.ti.com/tool/MSPDRIVERLIB.

3.1.2.2 USB-2-MDIO GUI

The USB-2-MDIO software tool lets Texas Instruments' Ethernet PHYs access the MDIO status and device control registers. The USB-2-MDIO tool includes a LaunchPad Development kit for TI's MSP430 MCUs or an onboard MSP430 MCU that is interfaced with a lightweight GUI through the USB interface. The MPS430 MCU implements an MDIO bus controller that can manipulate registers on the PHYs attached to the bus. The USB-2-MDIO tool allows users to read, write, script register read and write transactions and log data coming from the MDIO bus.

Download the *USB to MDIO serial management tool* from http://www.ti.com/tool/usb-2-mdio. See the *USB-2-MDIO Software Tool* user's guide for instructions on installing and using the software. Because the MSP430F5529 MCU is onboard, a separate MSP430 LaunchPad kit does not have to be purchased. and connected to the PHY with wires. The MSP430F5529 and USB-2-MDIO utility can be used even when power is not supplied via the USB. If the onboard MSP430 MCU cannot be used for any reason, the MDIO and MDC pins are also broken out on the J5 connector on the PSE side board. Customers can connect a MSP430 LaunchPad or their own MDIO-MDC utility on J5 to access the PHY registers. See the *USB-2-MDIO Software Tool* user's guide for setting up and using the USB-2-MDIO GUI.

3.1.2.3 CDC Driver

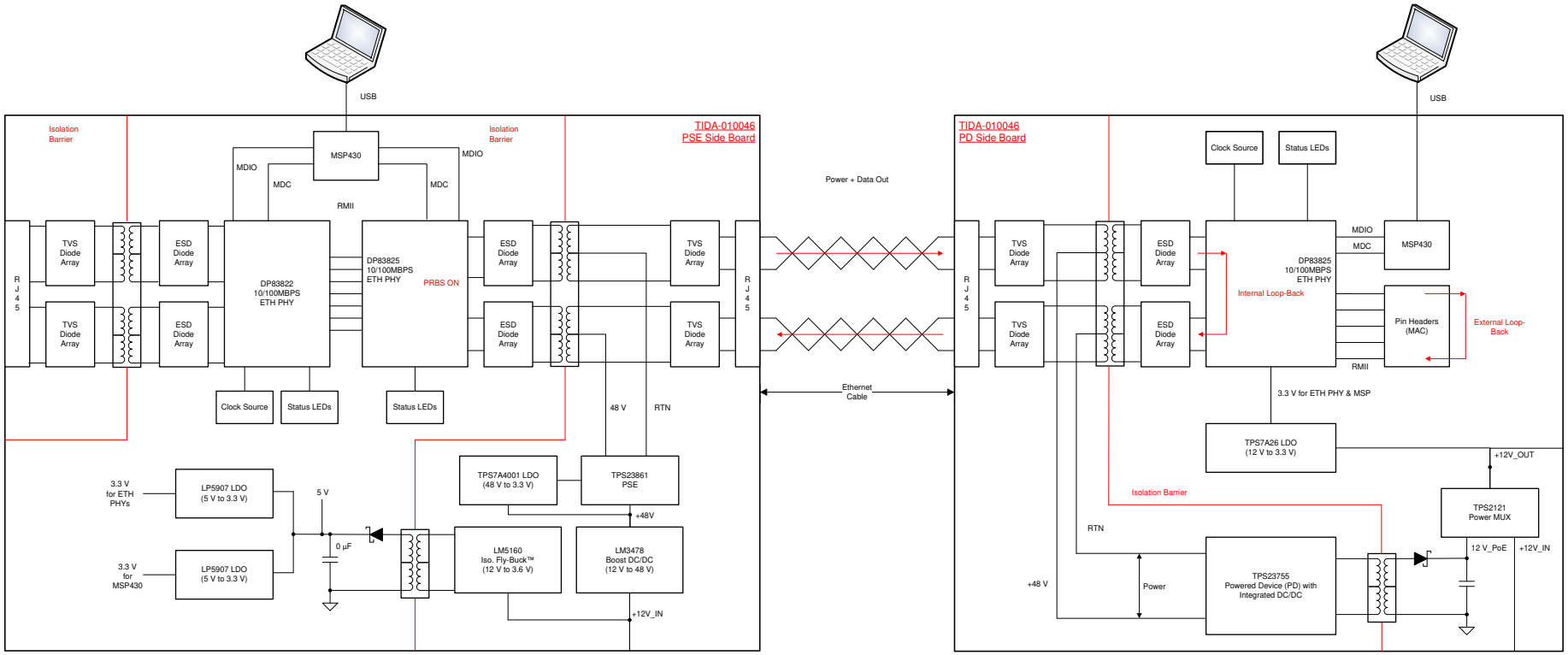
Download the CDC driver from http://www.ti.com/lit/zip/snlc061. Unzip and save the folder to your hard drive where it will not be deleted. When you plug the flashed MSP into your computer, the device manager will show the pound icon, then right-click it. Select the option for finding the driver on your PC. Go to the folder that you downloaded the zip file to and install. After the installation finishes, unplug the USB cable and then re-plug it. The USB-2-MDIO controller should appear in your device manager under 'Port'.

3.2 Testing and Results

This section provides details of the different functional, performance, and EMC tests performed.

3.2.1 Test Setup

図 27. Functional Test Setup of TIDA-010046



3.2.2 Test Results

3.2.2.1 Eye Diagram

Because the serial communication links of today operate at very high transmission frequencies, a number of variables that can affect the signal integrity are transmission-line effects, impedance mismatches, signal routing, termination schemes, and grounding schemes. An eye diagram created using an oscilloscope helps to quickly evaluate system performance and gain insight into the nature of channel imperfections that can lead to errors when a receiver tries to interpret the value of a bit. As high-speed serial data travels from a transmitter to a receiver, it can suffer impairments. The transmitter, PCB traces, connectors, and cables will introduce interference that will degrade a signal both in its amplitude and timing.

An eye diagram is a common indicator of the quality of signals in high-speed digital transmissions and might be helpful in locating the source of the problem. An oscilloscope generates an eye diagram by superimposing positive and negative pulses. Overlaying many bit transitions over time result in an image that looks like an eye-shaped pattern. An eye diagram can reveal important information. It can indicate the best point for sampling, divulge the SNR (signal-to-noise ratio) at the sampling point, and indicate the amount of jitter and distortion. Additionally, it can show the time variation at zero crossing, which is a measure of jitter. 図 28 shows the eye diagram for the DP83825 Ethernet PHY. 表 11 shows different eye diagram measurements.

注: A Tektronix FastAcq was used with positive edge trigger and infinite persistence that will result in this stacked eye waveform.

図 28. Eye Diagram

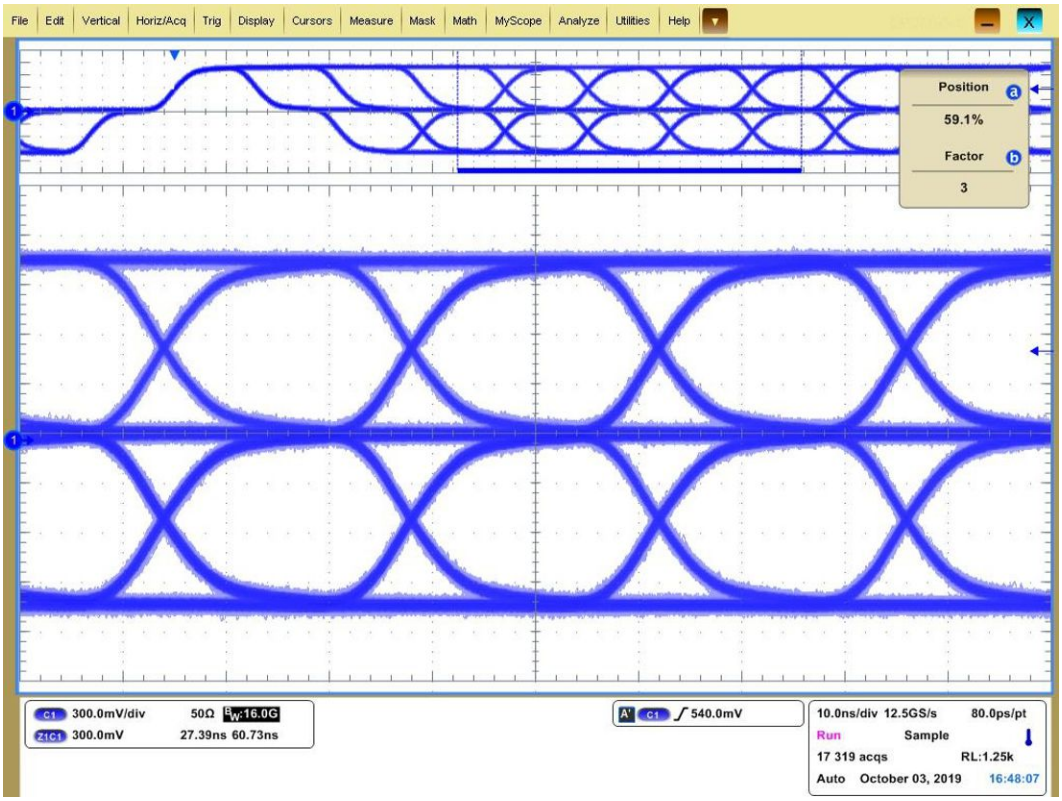


表 11. Eye Diagram Measurement Results

PARAMETER	SPECIFICATION RANGE	MEASURED VALUE
Positive Amplitude (+Vout)	950 mV to 1050 mV	1037.7 mV
Negative Amplitude (–Vout)	–950 mV to –1050 mV	–1027.8 mV
Rise time (+ve)	3 ns to 5 ns	3.64 ns
Rise time (–ve)	3 ns to 5 ns	3.55 ns
Fall time (+ve)	3 ns to 5 ns	3.72 ns
Fall time (–ve)	3 ns to 5 ns	3.55 ns
Jitter (+ve)	< 1.4 ns	420 ps
Jitter (–ve)	< 1.4 ns	430 ps

3.2.2.2 Bit Error Rate (BER)

Bit Error Rate verification was performed as per Fast Ethernet Consortium Physical Medium Dependent (PMD) Clause 25 Test Suite #25.2.4. This test attempts to verify a much lower BER in the presence of poor signal-to-noise ratio. As per PMD Test Suite #25.2.4, the bit error rate is verified for cable lengths of 75 and 100 m. However, in this reference design, the BER test was performed with 150-m cable length for data only and with 100-m cable length for power plus data together.

BER Test Criterion: If more than 7 errors are observed in 3×10^{11} bits (about 19,770,000 packets each with 1,518-byte - approximately 20 million packets), it can be concluded that the error rate is greater than 10^{-11} with less than a 5% chance of error. Note that if no errors are observed, it can be concluded that the BER is no more than 10^{-11} with less than a 5% chance of error.

Test Procedure #1: 150-m Cable Length for Data Only

- Configure the IXIA link simulator to generate more than 20 million packets with random data
- Use 150-m long CAT5e Ethernet cable
- Generated packets are sent to the repeater board (PSE side board) powered by a 12-V DC adaptor to pass through the packets
- Only data, no power: Disable PoE-PSE by shorting pin-1 and 2 of J10 connector on PSE side board
- Connect PD side board on the other end of the cable powered by a separate 12-V DC adaptor locally
- Configure the DP83825 Ethernet PHY on the PD side board to loopback the received packets internally
- Loopback packets are finally received by IXIA via repeater board and gets compared with the originally transmitted packet for any error

Observation: No errors are observed over multiple iterations as 図 29 shows. That concludes the BER is no more than 10^{-11} with less than a 5% chance of error.

Test Procedure #2: 100-m Cable Length for Power plus Data

- Configure the IXIA link simulator to generate more than 20 million packets with random data
- Use 100-m long CAT5e Ethernet cable
- Generated packets are sent to repeater board (PSE side board) powered by a 12-V DC adaptor to pass through the packets
- Power plus data together: Enable PoE-PSE to inject power over Ethernet cable by removing the shorting between pin 1 and 2 of J10 connector on PSE side board
- Connect the PD side board on the other end of the cable that gets powered from PoE

- Configure the DP83825 Ethernet PHY on the PD side board to loopback the received packets internally
- Loopback packets are finally received by IXIA via repeater board and gets compared with the originally transmitted packet for any error

Observation: No errors are observed over multiple iterations as 図 29 shows. That concludes the BER is no more than 10^{-11} with less than a 5% chance of error.

図 29. Bit Error Rate (BER) Test

Stats For 172.24.179.71:01.05	Count	Rate
Link State	Link Up	
Line Speed	100 Mbps	
Duplex Mode	Full	
Frames Sent	25,000,000	0
Valid Frames Received	25,000,000	0
Bytes Sent	19,775,716,...	0
Bytes Received	19,775,716,...	0
Fragments	0	0
Undersize	0	0
Oversize and Good CRCs	0	0
CRC Errors	0	0
Vlan Tagged Frames	0	0
Flow Control Frames Received	0	0
Alignment Errors	0	0
Dribble Errors	0	0
Collisions	0	0
Late Collisions	0	0
Collision Frames	0	0
Excessive Collision Frames	0	0
Oversize and CRC Errors	0	0
User Defined Stat 1	0	0
User Defined Stat 2	0	0
Capture Trigger (UDS 3)	25,000,000	0
Capture Filter (UDS 4)	25,000,000	0
ProtocolServer Transmit	0	
ProtocolServer Receive	0	
Transmit Arp Reply	0	
Transmit Arp Request	0	
Transmit Ping Reply	0	
Transmit Ping Request	0	
Receive Arp Reply	0	
Receive Arp Request	0	
Receive Ping Reply	0	
Receive Ping Request	0	
IPv4 Packets Received	0	0
UDP Packets Received	0	0
TCP Packets Received	0	0
IPv4 Checksum Errors	0	0

3.2.2.3 EMI/EMC Tests

This reference design is tested for EMI/EMC according to standards:

- Radiated emission: CISPR 22 (EN 55022) and FCC Part 15 Subpart B - Class A and B limits
- Conducted immunity: IEC61000-6-2 for ESD and IEC61000-4-4 for EFT

3.2.2.3.1 Radiated Emission Test

Any electronic products must pass applicable EMC requirements for the area where that product is to be sold. Several factors determine the type of EMI testing to be performed, including where the product will be sold, the classification of the product(industrial, scientific, medical, automotive or information technology (IT)) and how the product will be used. For example, in the US, the FCC and the American National Standards Institute (ANSI) have established extensive regulations for EMI testing. The part 15 requirements of the FCC apply to broadcast receivers, digital devices, switching power supplies and fluorescent lights, while its Part 18 requirements apply to industrial, scientific and medical products.

In Europe, Comite International Special des Perturbations Radioelectriques (CISPR) and European Norm (EN) regulations provide the guidelines for EMI testing. For example, CISPR 11 and EN 55011 regulations apply to scientific and medical products. CISPR 14 and EN 55014 apply to electric-motor-based products, while CISPR 22 and EN 55022 apply to IT equipment.

This reference design is targeted for information technology equipment product sectors as highlighted in 表 12. So, the applicable test standards are CISPR 22 (EN 55022) and FCC Part 15 Subpart B - Class A and B limits.

表 12. Main Product Standards for Radiated Emissions

PRODUCT SECTOR		IEC | CISPR STANDARD	EN STANDARD	FCC STANDARD
Vehicles, boats, and devices with internal-combustion engines	Offboard receivers	CISPR 12	EN 55012	—
	Onboard receivers	CISPR 25	EN 55025	—
Information Technology Equipment (ITE) – computers, telephones, other telecommunication products, video camera, multimedia equipment		CISPR 22 CISPR 32 (Latest)	EN 55022 EN 55032 (Latest)	Part 15
Industrial, Scientific, and Medical (ISM) equipment		CISPR 11	EN 55011	Part 18
Household appliances, electric tools, and similar apparatus		CISPR 14-1	EN 55014-1	—
Luminaires, lighting equipment		CISPR 15	EN 55015	Part 15, Part 18
Equipment with no product-specific standard	Light industrial	IEC 61000-6-3	EN 61000-6-3	—
	Heavy industrial	IEC 61000-6-4	EN 61000-6-4	—

The radiated emissions maximum measurement frequency is chosen based on the highest frequency of the internal clock source of the EUT. The following list shows the clock source used in the reference design on the PD side board (DUT):

- TPS23755 PoE-PD DC/DC switching frequency = approximately 500 kHz
- XTAL1 = 25 MHz for DP83825I
- REF CLOCK OUT = 50 MHz (Used for MAC interface; all RMII signals are disabled in this case)
- XTAL2 = 4 MHz for MSP430

Therefore, the measurement frequency band that is applicable for radiation testing is from 30 MHz to 1 GHz as highlighted in 表 13.

注: Since this reference design does not have a MAC, any activity on the RMII (including 50-MHz reference clock output) was disabled during the radiated emission testing.

表 13. Radiated Emissions Maximum Measurement Frequency

PRODUCT SECTOR		IEC | CISPR STANDARD	EN STANDARD	FCC STANDARD
Vehicles, boats, and devices with internal-combustion engines	Offboard receivers	CISPR 12	EN 55012	—
	Onboard receivers	CISPR 25	EN 55025	—
Multimedia equipment		CISPR 22	EN 55022	Part 15
ISM		CISPR 11	EN 55011	Part 18
Household appliances, electric tools, and similar apparatus		CISPR 14-1	EN 55014-1	—
Luminaires, lighting equipment		CISPR 15	EN 55015	Part 15, Part 18
Equipment with no product-specific standard	Commercial and light industrial	IEC 61000-6-3	EN 61000-6-3	—
	Heavy industrial	IEC 61000-6-4	EN 61000-6-4	—

Then, how are class A or class B limits selected?

- Class A: Equipment, device and apparatus, that is marketed for use in commercial, business, and industrial environments
- Class B: Equipment, device and apparatus, that is marketed for use in the home or a residential environment by the customer

The emissions standards are more severe for Class B devices because they are more likely to be located close to a radio or TV receiver in the home environment. Therefore, for Class B emission limits are more restrictive than Class A by a factor of 3 (approximately 10 dB).

The radiated test setup shown in 図 30 incorporates a measurement antenna that is placed 1 to 4 m above the ground plane. The DUT is placed on a nonconductive table that is 80 cm high. The antenna and DUT first should be separated by 3 m (or 10 m if required by the regulations). Both CISPR and ANSI requirements call for the DUT to be in a worst-case operating mode, that is, a mode in which it is likely to radiate an EM field. 図 31 shows the CISPR 22 / EN55022 and FCC Part 15 limits using quasi-peak and average detectors, respectively. The test distance for radiated emission from the DUT to the antenna is 3 m. The test was performed in an aneochic chamber, which conforms to the Volumetric Normalized Site Attenuation (VNSA) for both 3- or 10-m measurements. 図 32 and 図 33 show the actual pictures of test setup for radiated emission test with antenna positioned at 3-m distance in horizontal and vertical polarizations, respectively.

図 30. Radiated Emissions Measurement Setup for FCC Part 15 and CISPR 22

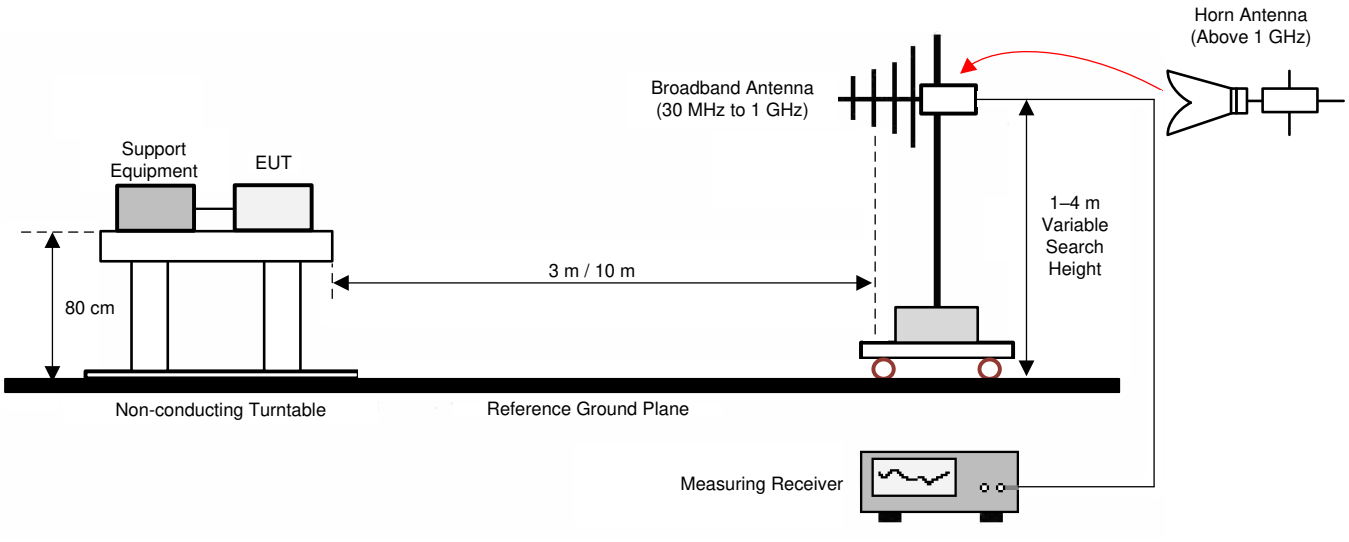
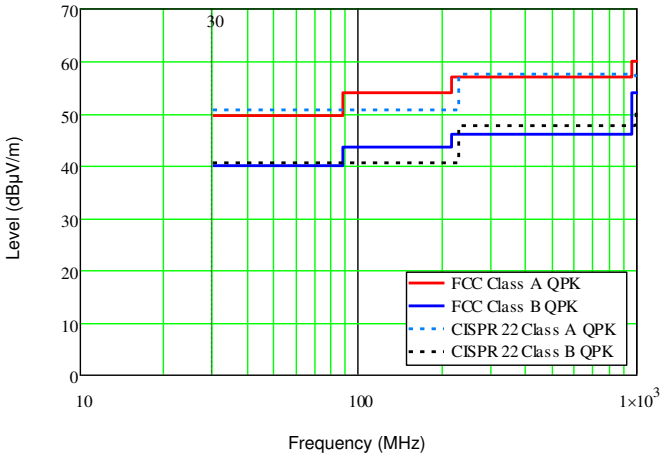


図 31. FCC Part 15 and CISPR 22 Radiated Limits for Class A and Class B Using QPK and AVG Detectors



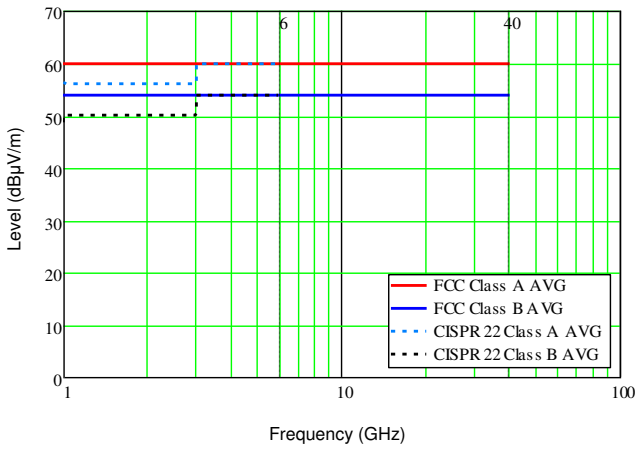


図 32. Actual Test Setup for Radiated Emission Test With Antenna Positioned at 3-m Distance in Horizontal Polarization

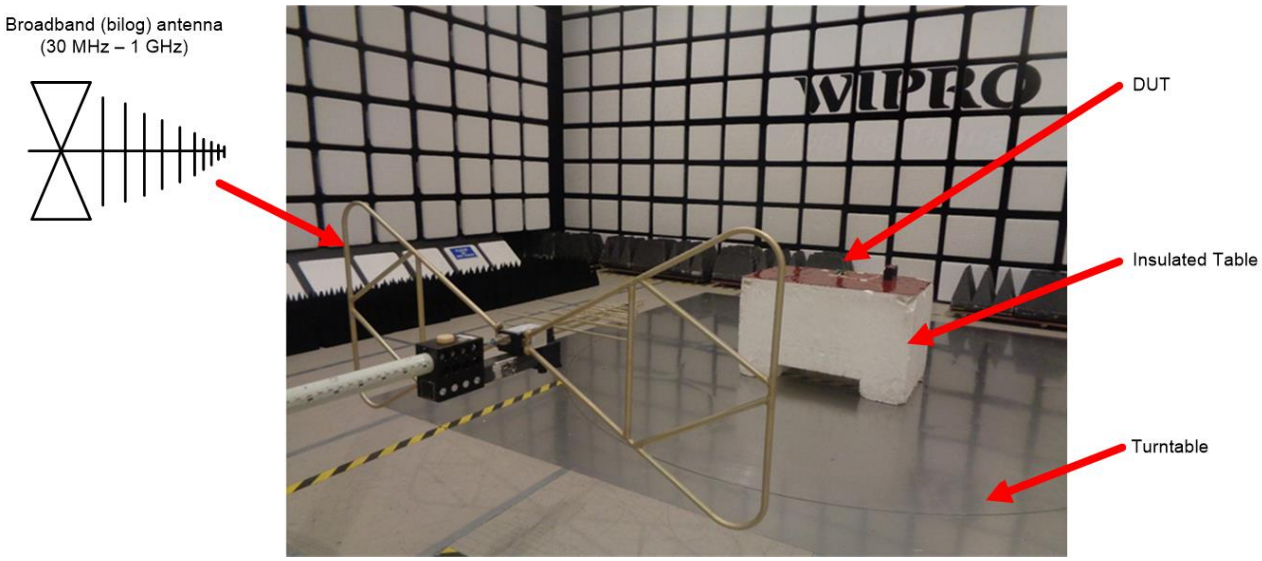
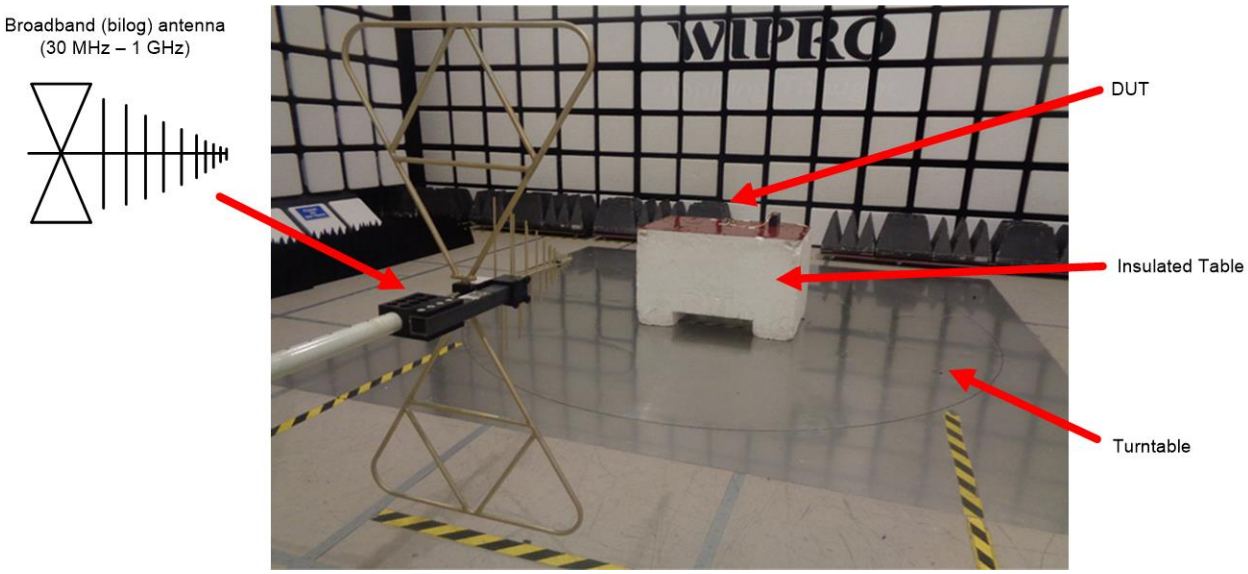


図 33. Actual Test Setup for Radiated Emission Test With Antenna Positioned at 3-m Distance in Vertical Polarization



To evaluate the radiated emissions of the DUT, ambient EM levels at the test site first must be determined. The ideal situation is for all of the ambient signals to be below the measurement limit line. So these signals should be measured with the DUT turned off. The ambient signals were found at least 25 dB below the limits throughout the measurement frequency band for both polarizations as 図 34 shows.

図 34. Ambient Scan

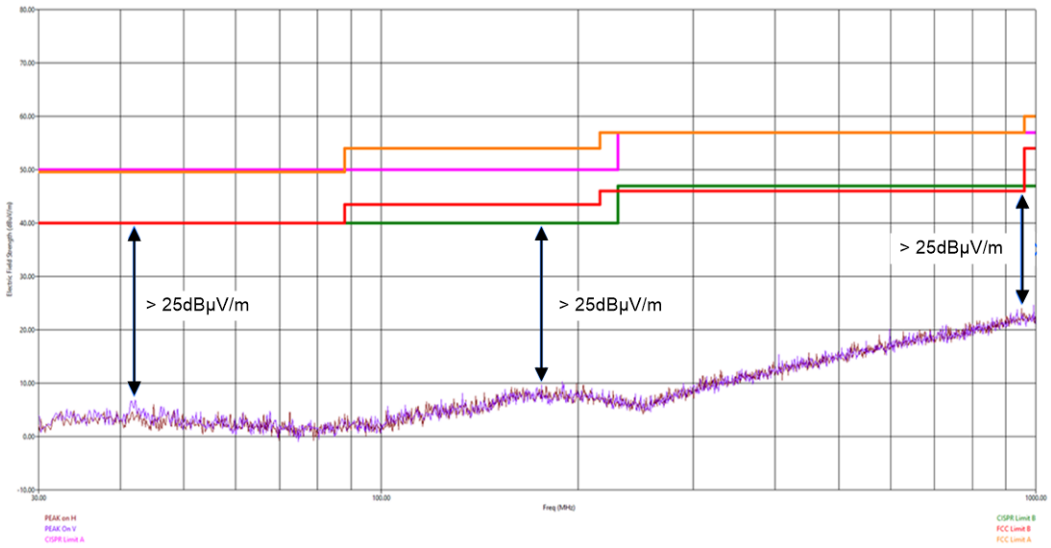


図 35 shows the DUT configuration for radiated emission testing. The DUT (PD side board) was placed on the nonconductive table inside the chamber, whereas the PSE side board was kept outside the chamber connected through a long CAT5e cable. The CAT5e cable was externally shielded just to debug or focus on the radiated emissions coming through the DUT rather than radiated emission coming from cable itself. The PSE side board was powered by a 12-V lead-acid battery. The PD side board was powered from PoE, which means the DC/DC power supply on the DUT was ON. The DP83825I Ethernet PHY on PSE side board was configured to generate pseudo-random binary sequence (PRBS), while the DP83825I Ethernet PHY on PD side board was configured to internally loopback the PRBS packets. Therefore, the radiated emission testing was performed when the DUT is continuously communicating with the PSE side board (link partner). Disturbance field strength limits (peak) according to CISPR 22 (EN 55022) and FCC Part 15 Subpart B, normalized to a distance of 3 m. 図 36 shows the radiated emission plot with both horizontal and vertical polarizations in a single graph.

図 35. DUT Configuration for Radiated Emission Testing

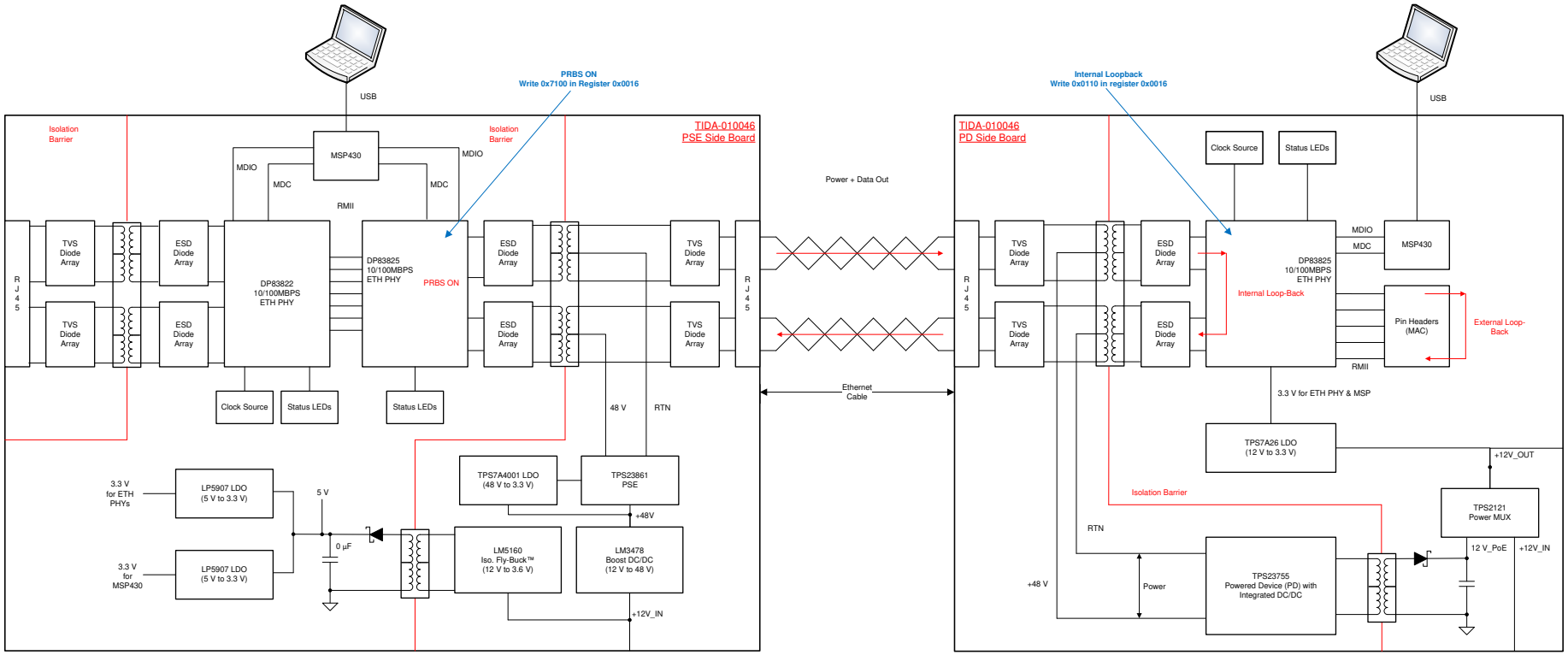
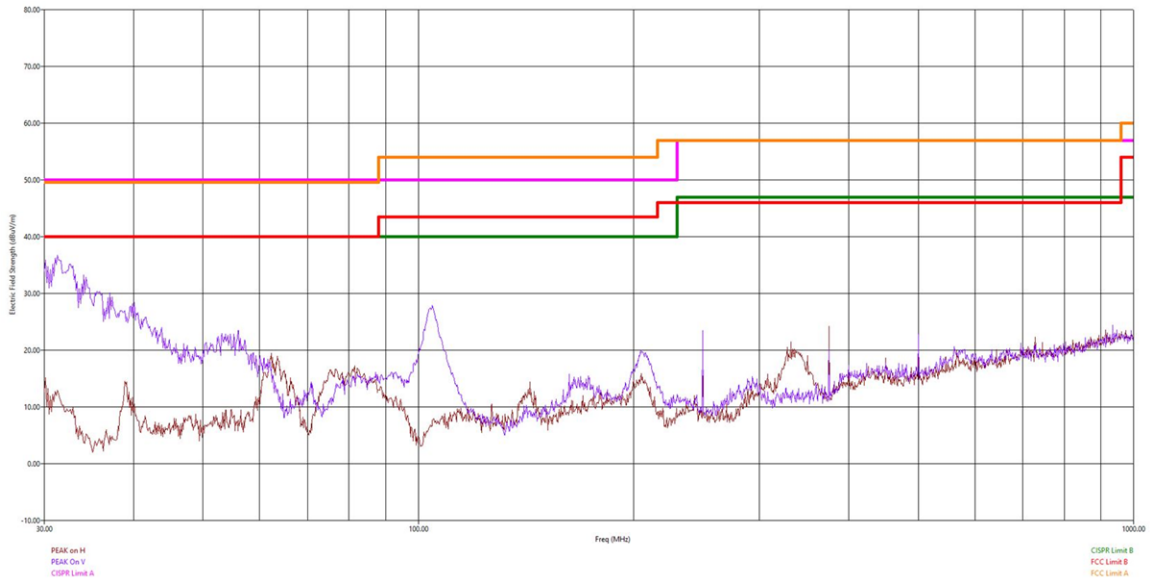


図 36. Measured EMI Spectrum According to CISPR 22 (EN 55022) and FCC Part 15 Subpart B; 3-m Near-Field, Horizontal and Vertical Polarizations



3.2.2.3.2 Conducted Immunity

The TIDA-010046 reference design is pre-compliance tested for ESD and EFT with reference to standards IEC61000-4-2 and IEC61000-4-4, respectively. The performance (acceptance) criterion is defined as in 表 14.

表 14. Performance (Acceptance) Criterion

PERFORMANCE (ACCEPTANCE) CRITERION	DESCRIPTION
A	The module will continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, the module will continue to operate as intended without manual intervention.
C	Temporary degradation of performance is accepted. After the test, the module will continue to operate as intended without manual intervention.

3.2.2.3.2.1 ESD IEC-61000-4-2 ESD Test

図 37 shows the ESD test setup. The IEC 610004-2 ESD test simulates an electrostatic discharge of an operator directly onto an adjacent electronic component. An electrostatic charge usually develops in low relative humidity and on low-conductivity carpets, or vinyl garments. To simulate a discharge event, an ESD generator applies ESD pulses to the DUT, which can happen through direct contact with the DUT (contact discharge), or through an air-gap (air-discharge). This is applied across signal inputs only. A series of 10 negative and positive pulses were applied to the DUT in both power-on and power-off conditions. The ESD strikes were given to the RJ45 connector metallic body and its pins. After the test, the DUT was verified for functionality. The test results show the TIDA-010046 reference design can withstand the required discharge (see 表 15). There were no signs of any permanent failure or damage. The DUT was found working normal as intended before and after the ESD strikes.

図 37. IEC61000-4-2 ESD Test Setup for TIDA-010046

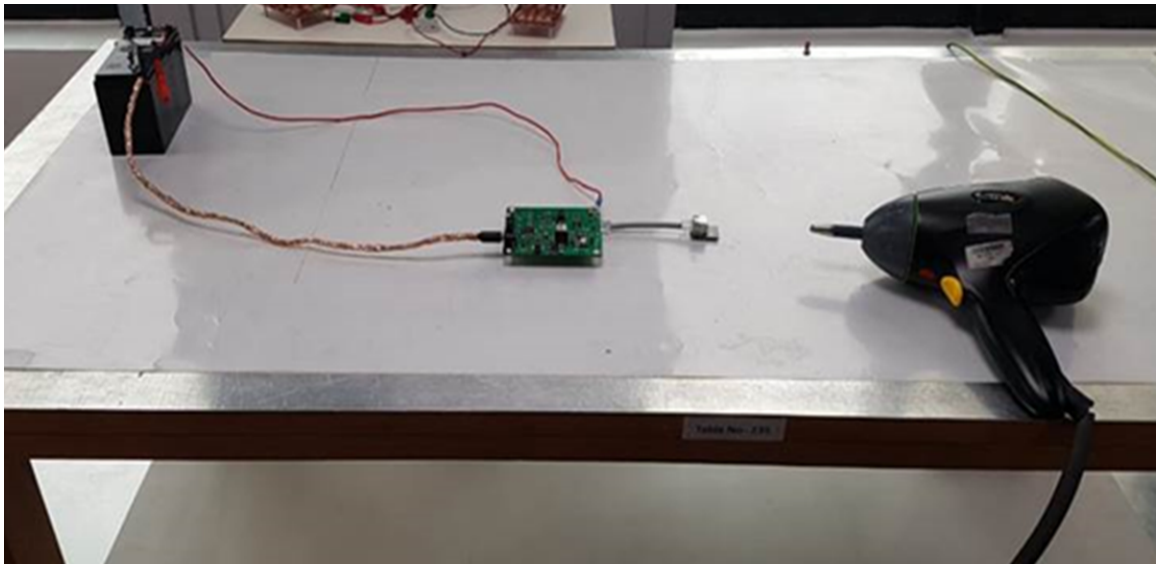


表 15. ESD Test Summary

DISCHARGE TYPE	LEVEL	TEST CONDITION	CRITERIA | RESULT
IEC61000-4-2 ESD air-discharge	±15 kV	DUT is powered-on 10 strikes of each polarity on RJ45 connector body	B | Pass
IEC61000-4-2 ESD air-discharge	±15 kV	DUT is powered-off 10 strikes of each polarity on RJ45 connector body	B | Pass
IEC61000-4-2 ESD air-discharge	±15 kV	DUT is powered-on 10 strikes of each polarity on pins	B | Pass
IEC61000-4-2 ESD air-discharge	±15 kV	DUT is powered-off 10 strikes of each polarity on pins	B | Pass
IEC61000-4-2 ESD contact discharge	±12 kV	DUT is powered-on 10 strikes of each polarity on RJ45 connector body	B | Pass
IEC61000-4-2 ESD contact discharge	±12 kV	DUT is powered-off 10 strikes of each polarity on RJ45 connector body	B | Pass
IEC61000-4-2 ESD contact discharge	±12 kV	DUT is powered-on 10 strikes of each polarity on pins	B | Pass
IEC61000-4-2 ESD contact discharge	±12 kV	DUT is powered-off 10 strikes of each polarity on pins	B | Pass

3.2.2.3.2.2 IEC-61000-4-4 EFT Test

図 38 shows the EFT test setup. During the EFT test, both the PSE side and PD side boards were used, connected using a 3-m long CAT5e Ethernet cable pass through a capacitive clamp as 図 38 shows. The EFT burst signals were injected on the Ethernet cable as a common-mode noise. Both the boards were powered by two separate 12-V batteries. During the test, one board was generating the pseudo-random packets and the other board was simply looping back those packets. After the test, the DUT was verified for functionality. The test results show the DUT can withstand up to ±2 kV. The DUT performed normally after each test. Because functionality could not be verified during the test, the result is noted as passing criteria B. 表 16 shows the test results. Packet errors were observed during the application of the EFT bursts but that recovers aa soon as the EFT pulses are removed. No link drop was observed.

図 38. IEC61000-4-4 EFT Test Setup for TIDA-010046

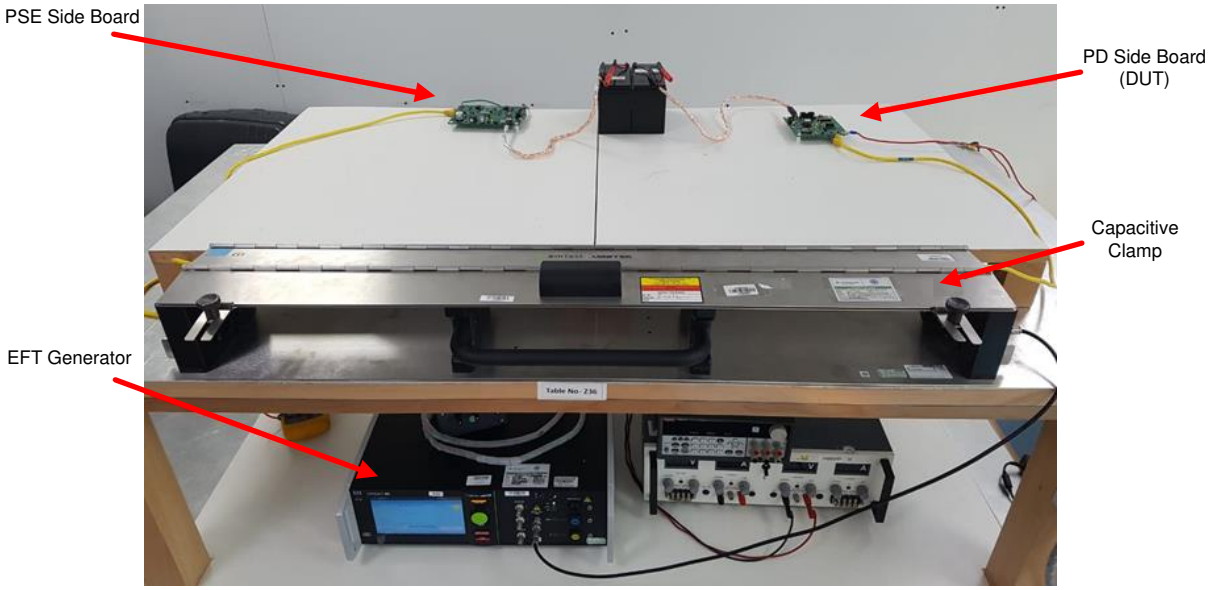


表 16. EFT Test Summary

IMMUNITY TEST	STANDARD	PORT	TEST CONDITION	CRITERIA | RESULT
EFT	IEC 61000-4-4 Level 4: ±2 kV with capacitive clamp and 5 kHz	Communication cable	PSE side board generated PRBS and PD side board (DUT) loops back the packets	B | Pass (Link does not drop)
EFT	IEC 61000-4-4 Level 4: ±2 kV with capacitive clamp and 5 kHz	Communication cable	PD side board (DUT) generated PRBS and PSE side board loops back the packets	B | Pass (Link doesn't drop)

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010046.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010046.

4.3 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010046.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDA-010046.

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010046.

5 Related Documentation

1. Texas Instruments, *DP83822 Robust, Low Power 10/100 Mbps Ethernet Physical Layer Transceiver Data Sheet*
2. Texas Instruments, *DP83825I Low Power 10/100 Mbps Ethernet Physical Layer Transceiver Data Sheet*
3. Texas Instruments, *TPS23861 Power-On Considerations Application Report*
4. Texas Instruments, *Selection and Specification of Crystals for Texas Instruments Ethernet Physical Layer Transceivers Application Report*
5. Texas Instruments, *Electrical Transient Immunity for Power-Over-Ethernet Application Report*
6. Texas Instruments, AN-1469 PHYTER Design & Layout Guide
7. Texas Instruments, *USB-2-MDIO Software Tool User's Guide*

5.1 商標

5.2 Third-Party Products Disclaimer

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2019年10月発行のものから更新 **Page**

- 最初のページの文法の誤りを 変更 1

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265