参考資料

デザイン・ガイド: TIDA-010081
5G テレコム整流器用の効率 > 95% の 1kW アナログ制御 AC/DC のリファレンス・デザイン

概要

この小型で高効率の DC 54V、1000W 出力のリファレンス・デザインは、5G テレコムおよび産業用 AC/DC 電源を対象としています。この回路は、UCC28180 を使用したフロントエンドの連続導通モード (CCM) 力率補正 (PFC) 回路と、UCC256403 を使用した絶縁型 DC/DC コンバータ用の堅牢な LLC 段とで構成されています。高効率の要求を満たすため、UCC24624 は同期整流を行います。このリファレンス・デザインは、UCC28911 (高電圧 MOSFET を内蔵) による補助電源フライバックを使用しています。このリファレンス・デザインは 95.9% のピーク効率を実現しているため、システムは強制冷却を使わずに動作できます。システム全体は iTHD が低く (30% 負荷で 12% 未満、50% 負荷で 8% 未満、100% 負荷では 5.5% 未満)、負荷過渡性能が優れています。このリファレンス・デザインは、別のリファレンス・デザイン (TIDM-SERVER-PWR-MON) を使用して、10%～100% の負荷で ±1% 精度を達成できる入力電力測定を行っています。

リソース

TIDA-010081	デザイン・フォルダ
UCC256403、UCC28180	プロダクト・フォルダ
UCC27517、UCC24624	プロダクト・フォルダ
UCC28911、MSP430I2021	プロダクト・フォルダ

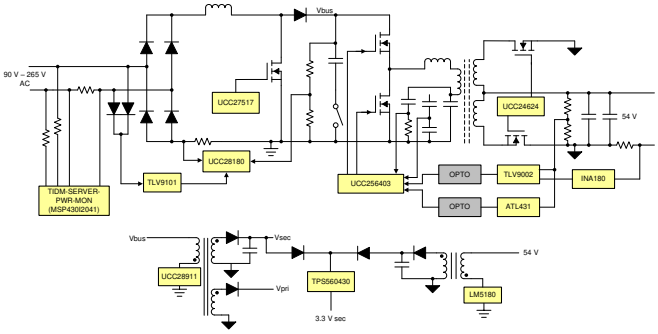
Search Our E2E™ support forums

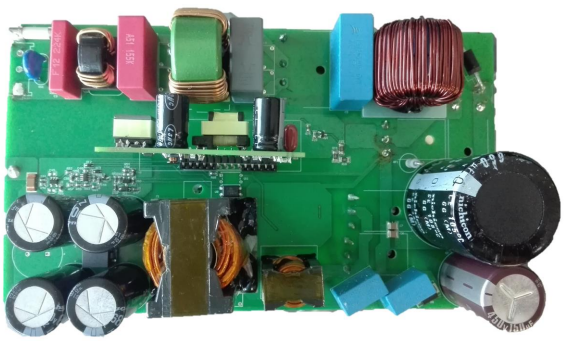
特長

- ピーク効率:AC 230V で 95.9%、30%～100% の負荷にわたって 95%
- CCM PFC、ハーフブリッジ LLC を採用 (UCC28180、UCC256403)
- 低い iTHD:30% 負荷で 12% 未満、50% 負荷で 8% 未満、100% 負荷で 5.5% 未満
- 1% 未満のレギュレーションで優れた負荷過渡性能
- 負荷範囲全体にわたって ±1% 以内の入力電力測定精度を達成
- 密閉型金属ケースによる受動冷却

アプリケーション

- 商用テレコム整流器
- 産業用AC/DC





1 System Description

This compact, high efficiency AC/DC reference design has a 54-V DC, 1000-W output at 230-V AC and derates to 500-W output at 115-V AC. The circuit consists of a front-end continuous conduction mode (CCM) power factor correction (PFC) circuit based on the UCC28180, followed by a robust LLC stage for an isolated DC/DC converter based on the UCC256403. For high efficiency needs, synchronous rectification is done with the UCC24624. This design uses an auxiliary power supply flyback with the UCC28911 which has an internal high-voltage MOSFET (HV MOS). This design also has the input power meter function using MSP430I2021 which can achieve ±1% accuracy from 10% load to 100% load range. This design enables 95.9% peak efficiency and allows the system to work without forced cooling. This design has low iTHD, with 30% load at <12%, 50% load at <8%, 100% load at <5.5%, and good load transient performance.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS					
Input voltage		85	230	265	VAC
Frequency		47	50	63	Hz
No load power				4000	mW
OUTPUT CONDITIONS					
Output voltage			54		V
Output current	V_O = 54-V		18.7		A
Line regulation	V_O = 54-V			1	%
Load regulation	V_O = 54-V			1	%
Output voltage ripple	V_O = 54-V, Peak-Peak			277	mV
Output power (nominal)				1000	W
SYSTEM CHARACTERISTICS					
Efficiency	Vin = 230-V AC RMS and full load at 54-V output		95		%
	Vin = 115-V AC RMS and full load at 54-V output		93		%
Power factor	Vin = 230-V AC RMS and full load at 54-V output		0.98		
	Vin = 115-V AC RMS and full load at 54-V output		0.99		
Protections	Output overcurrent				
	Output overvoltage				
	Output undervoltage				
Operating ambient	Open frame	-10	25	55	°C
Standards and norms	Power line harmonics (THD)	IEC 61000-3-2 Class A			
	Conducted emissions	EN 55022 Class B			
	EFT	As per IEC 61000-4-4			
	Surge	As per IEC 61000-4-5			

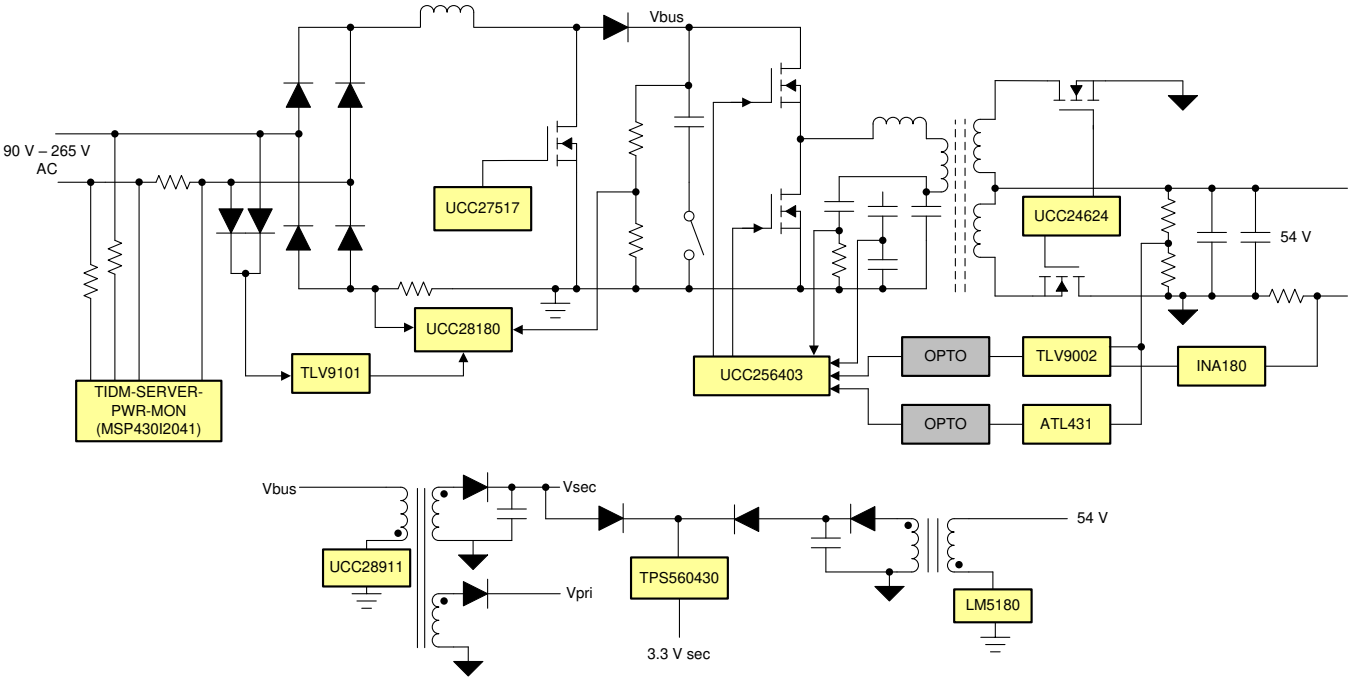
表 **1. Key System Specifications (continued)**

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Board form factor (FR4 material, 2 layer)	Length × Breadth × Height	190 × 110 × 50			mm

2 System Overview

2.1 Block Diagram

図 1. TIDA-010081 Block Diagram



2.2 Highlighted Products

The following highlighted products are used in this reference design. These sections also highlight the key features for selecting the devices for this reference design. For the complete details of these highlighted devices, see the respective product data sheet.

2.2.1 UCC28180

The UCC28180 is a high-performance, continuous conduction mode (CCM), 8-pin programmable frequency power factor correction (PFC) controller. The wide and programmable operating frequency of the controller provides flexibility to design at a high frequency to optimize the components. The UCC28180 uses trimmed current loop circuits to achieve less than a 5% THD from a medium-to-full load (50% to 100%). A reduced current sense threshold enables the UCC28180 device to use a 50% smaller shunt resistor, resulting in lower power dissipation while maintaining low THD. The UCC28180 also consists of an integrated fast gate driver, with a drive of 2-A source current and –1.5-A sink current, which eliminates the need for an external gate driver. The UCC28180 device also has a complete set of system protection features that greatly improves reliability and further simplifies the design:

- Soft overcurrent
- Cycle-by-cycle peak current limit
- Output overvoltage
- VCC undervoltage lockout (UVLO) protection
- Open pin protections (ISENSE and VSENSE pins)

2.2.2 UCC25640X

An LLC resonant converter is one of the most widely used topologies for implementing medium- to high-power, isolated, DC/DC power stages in industrial power supplies. These converters are popular due to their ability to achieve soft-switching (ZVS turn on) for the high-voltage MOSFET and hence improving the overall efficiency of the system. The UCC25640x is a fully featured LLC controller. The UCC25640x includes a range of features designed to make LLC converter operation well controlled and robust. The part aims to unburden the LLC designer and allow mainstream applications to benefit from efficiency advantages of the LLC topology. This device uses hybrid hysteretic control to provide best-in-class line and load transient response. The control effort is approximately linear proportional to the average input current in one cycle. The control makes the open loop transfer function a first-order system so that it's very easy to compensate. The system is always stable with proper frequency compensation. Ensure that the LLC converter does not enter capacitive (ZCS) region during the low input voltage condition; otherwise, it could make damage to the system.

The UCC25640x with its ZCS avoidance feature can ensure that the system does not enter the ZCS region under all operating conditions and hence ensures the safety of the system. Apart from this, the power supplies typically need a tunable input or output voltage with a wide range. The UCC25640x provides a wide operating frequency range from 35 kHz to 1MHz to make it easier to design a wide output voltage range using an LLC converter. Its wide frequency range can reduce the PFC bulk capacitor required to meet the holdup time requirement in the industrial power supplies. With the integrated high-voltage gate drive, X-Cap discharge function, and additional output OVP, the UCC256401x reduces the amount of external discreet components required to implement a high-efficiency industrial PSU.

2.2.3 UCC24624

The UCC24624 high-performance synchronous rectifier (SR) controller is dedicated for LLC resonant converters to replace the lossy diode output rectifiers with SR MOSFETs and improve the overall system efficiency. Two independent SR control channels are integrated into the single package to minimize the external components and allow for easy PCB layout.

The UCC24624 SR controller uses drain-to-source voltage sensing method to achieve on and off control of the SR MOSFET. Proportional gate drive is implemented to extend the SR conduction time, minimize the body diode conduction time, and improve efficiency. To compensate for the offset voltage caused by the SR parasitic inductance, the UCC24624 implements an adjustable positive turn-off threshold to accommodate different SR MOSFET packages. The UCC24624 has a built-in 450-ns minimum on-time blanking and a fixed 650-ns minimum off-time blanking to avoid SR false turn-on and -off. The UCC24624 also integrates a two-channel interlock function that prevents the two SRs from being on at the same time.

With the built-in standby mode detection based on average switching frequency, the UCC24624 enters the sleep mode automatically without using external components. The low standby mode current of 175 μA supports meeting modern no-load standby power requirements such as CoC and DoE regulations.

With a 1.5-A peak source and 4-A peak sink driving capability, the UCC24624 is able to support LLC converters up to 1-kW. With 230-V voltage-sensing pins and a 26-V maximum VDD rating, it can be directly used in converters with an output voltage of up to 26 V. The internal clamp allows the controller to support a 36-V output voltage easily by adding an external current limiting resistor on VDD.

2.2.4 UCC27517

The UCC27517 single-channel, high-speed, low-side gate driver devices can effectively drive MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, the UCC27517 can source and sink high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay, typically 13 ns. The UCC27517 provides 4-A source, 4-A sink (symmetrical drive) peak-drive current capability at VDD = 12 V.

2.2.5 TLV9002

The TLV9002 is dual-channel, low-voltage (1.8 V to 5.5 V) operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. This op amp provides a cost-effective solution for space-constrained applications where low-voltage operation and high capacitive-load drive are required. The capacitive-load drive of the TLV9002 is 500 pF, and the resistive open loop output impedance makes stabilization easier with much higher capacitive loads. This op amp is designed specifically for low-voltage operation (1.8 V to 5.5 V) with performance specifications. The robust design of the TLV9002 simplifies circuit design. The op amps feature unity-gain stability, an integrated RFI and EMI rejection filter, and no-phase reversal in overdrive conditions. Micro-size packages, such as SOT-553 and WSON, are offered, along with industry-standard packages such as SOIC, MSOP, SOT-23, and TSSOP packages.

2.2.6 MSP430I2021

The MSP430I2021 is an ultra-low-power mixed signal microcontroller. It integrates with two independent, differential-input, 24-bit, sigma-delta, analog-to-digital converters (ADCs) with programmable gain amplifiers, a 16-bit hardware multiplier. An eUSCI_A0 supports universal asynchronous receiver/transmitter (UART) and serial peripheral interface (SPI) communication interfaces. An eUSCI_B0 supports SPI, inter-integrated circuit (I2C) communication interfaces, two 16-bit timers, and 12 general-purpose input and output GPIO pins in a 28-pin TSSOP or 16 GPIO pins in a 32-pin QFN package. The peripheral set is a good combination for embedded electricity power measurement. In such an application, the device is embedded in the end application and measure the electricity, which provides the device information about the voltage, current, power consumption, and so forth.

2.3 System Design Theory

This reference design provides a universal AC, mains-powered, 1-kW nominal output at 54 V. This design is derating to 500 W at a low line input. The UCC28180 controls a PFC boost front end, while the UCC25640 LLC resonant half-bridge converts the PFC output to an isolated 54 V. The total system efficiency is 95% with a 230-V AC input and over 93% with a 115-V AC input at full load. In addition, several protections are embedded into this design, which include input undervoltage protection and output short-circuit protection. Low EMI, high efficiency, a high power factor, and a reliable power supply are the main focus of this design for targeted applications.

2.3.1 PFC Stage Design

The CCM boost PFC is a popular choice for the 1-kW design because of the low number of components and cost. This design, with the UCC28180, operates at a fixed frequency in CCM and requires minimal external components for high-wattage PFC implementation which helps reduce the cost. The design process and component selection for this design are illustrated in the following sections.

2.3.1.1 Design Parameters

表 2 shows the design goal parameters for the PFC stage.

表 2. Design Parameters for PFC Stage

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
INPUT					
High line input voltage	VAC_high	180	230	265	VAC
Low line input voltage	VAC_low	90	115	127	VAC
Input frequency	f_{LINE}	47	50	63	Hz
OUTPUT					
Output voltage	V_{blk}		390		VDC
Output power	PDCBUS	500	1000		W
Line regulation				5	%
Load regulation				5	%
Power factor	PF		0.99		
Hold up time	t_{holdup}			20	ms
Minimum switching frequency	fSW		65		kHz
Targeted efficiency	η_{PFC}		98		%

2.3.1.2 Current Calculation

The input fuse, bridge rectifier, and input capacitor are selected based on the input current calculations. First, determine the maximum average output current, $I_{out(max)}$, allowing for an overload to 110% of maximum load power.

$$I_{out(max)} = \frac{110\% \times P_{out}}{V_{blk}} = \frac{110\% \times 1000\ W}{390} = 2.82\ A \quad (1)$$

The PFC stage is 1 kW at high-line input at 180 V to 265 V and is derating to 500 W at low-line input at 90 V to 127 V. The maximum input RMS line current, $I_{in\_rms(max)}$, is calculated with minimum input voltage, the efficiency and power factor initial assumptions, allowing for an overload to 110% of maximum load power.

$$I_{in\_rms(max)} = \frac{110\% \times P_{out}}{V_{in(min)} \times \eta_{PFC} \times PF} = \frac{110\% \times 1000\ W}{180\ V\ AC \times 0.98 \times 0.99} = 6.3\ A \quad (2)$$

The maximum input peak current is:

$$I_{in\_pk(max)} = \sqrt{2} \times I_{in\_rms(max)} = \sqrt{2} \times 6.3\ A = 8.9\ A \quad (3)$$

The maximum input average current is:

$$I_{in\_avg(max)} = \frac{2}{\pi} \times I_{in\_pk(max)} = \frac{2}{\pi} \times 8.9\ A = 5.67\ A \quad (4)$$

2.3.1.3 Bridge Rectifier

The maximum input AC voltage is 265-V AC. For safety, the voltage rating of the bridge must be at least 600 V. The input bridge rectifier must have an average current capability that exceeds the input average current, $I_{in\_ave(max)}$. The bridge rectifier also carries the full inrush current as the bulk capacitor charges when the line is connected. The amplitude and duration of this current is difficult to determine in advance because it depends on parameters that are hard to predict.

2.3.1.4 Boost Inductor Design

To dimension the boost inductor, first calculate the maximum-allowed ripple current. The maximum ripple current is observed at the lowest input voltage and maximum load. Assuming a maximum 30% ripple in the inductor current gives a ripple current of:

$$I_{ripple(max)} = 0.3 \times I_{in\_pk(max)} = 2.67\ A \tag{5}$$

The maximum duty cycle is:

$$D_{max} = \frac{V_{out} - V_{in\_peak(min)}}{V_{out}} = 0.674 \tag{6}$$

The minimum boost inductor value is calculated from the maximum duty cycle:

$$L_{PFC} \geq \frac{V_{blk} \times D_{max} \times (1 - D_{max})}{fsw \times I_{ripple(max)}} = 566\,uH \tag{7}$$

The boost inductor must be able to support a maximum current of:

$$I_{L\_pk(max)} = I_{in\_pk(max)} + \frac{I_{ripple(max)}}{2} = 10.24\ A \tag{8}$$

2.3.1.5 Switching MOSFET

The drain source breakdown voltage of the switching MOS is ≥600 V. The drain-to-source RMS current through the MOS is calculated as:

$$I_{ds(max)} = \frac{P_{out}}{\sqrt{2} \times V_{in(min)}} \times \sqrt{2 - \frac{16 \times \sqrt{2} \times V_{in(nim)}}{3\pi \times V_o}} = 4.08\ A \tag{9}$$

The key specifications of the MOS that must be taken into consideration are:

- Low R_{dson} for reducing the conduction loss
- Low Q_g for fast turnon and turnoff in the hard switching in this topology
- Low output capacitance for reducing the switching loss

2.3.1.6 Boost Diode

The output diode must have a blocking voltage that exceeds the output overvoltage of the converter and an average current that exceeds $I_{out(max)}$. In CCM PFC topology, the boost diode undergoes hard turnoff and hence suffers from reverse recovery loss. To reduce the reverse recovery loss, it is better to select an ultra-fast diode or silicon-carbide diode. Silicon-carbide diodes have no reverse recovery loss, but the cost is higher than silicon ultra-fast diodes.

2.3.1.7 Output Capacitor

The value of the output capacitor is determined by two factors. One is that the value must be large enough to provide the required hold-up time. The other is that the value must be large enough to keep the ripple at twice the line frequency within the required limits. The holdup time required in this design is 20 ms. During this time, the minimum voltage that the PFC output can reach at full load is designed to be 300 V. Substituting the known values in 式 10, the minimum C_{out} is:

$$C_{out} \geq 2 \times P_{out} \times \frac{T_{holdup}}{V_{out(max)}^2 - V_{out(min)}^2} = 644\,uF \tag{10}$$

The output capacitor is selected to be 680 uF in this design.

2.3.1.8 Sense Resistor

To accommodate the gain of the non-linear power limit, the sense resistor, R_{SENSE}, is sized such that it triggers the soft overcurrent at 10% higher than the maximum peak inductor current using the minimum soft overcurrent threshold of the I_{SENSE} pin, VSOC, of I_{SENSE} equal to 0.259 V.

$$R_{sense} = \frac{V_{soc(min)}}{1.1 \times I_{L(max)}} = 0.021\Omega \tag{11}$$

2.3.2 LLC Stage Design

LLC topology has been widely used in telecom and server power supplies. LLC topology can get a wide gain range by changing the frequency. LLC topology usually applies to generation of a constant output voltage for a wide-input DC voltage range or generation of a variable output voltage for a constant input DC voltage. The wider the frequency range is, the more different the LLC design is. The DC/DC stage in this design must support 20-ms holdup time. LLC topology can achieve both ZVS for the primary MOSFET and ZCS for the secondary diode under resonant frequency. Considering efficiency, therefore, the converter is designed to operate at a frequency slightly lower than resonance frequency at full load.

2.3.2.1 Design Parameters

表 3 shows the design parameters for the LLC stage.

表 3. Design Parameters for LLC Stage

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
INPUT					
Input voltage	V_{INDC}	310	390	410	V_{DC}
OUTPUT					
Output voltage	V_{OUT}		54		V_{DC}
Max output power	P_{OUT}			1000	W
Nominal switching frequency	f_{SWNOM}		100		kHz
Line regulation			1		%
Load regulation			1		%
Targeted efficiency			97		%

2.3.2.2 Determining Mg

The transformer turns ratio is determined by 式 12:

$$n = \frac{\frac{V_{DCIN\_nom}}{2}}{V_{OUT}} \tag{12}$$

From the specifications, the nominal values for input voltage and output voltage are 390 V and 54 V, respectively, so the turns ratio can be calculated as:

$$n = \frac{\frac{390}{2}}{54} = 3.61 \tag{13}$$

No additional diode drop must be accounted for because a synchronous rectifier is used. The value used for turns ratio (n) for further calculations is 3.6.

2.3.2.3 LLC Gain Range Mg_{min} and Mg_{max}

Mg_{min} and Mg_{max} can be determined by using 式 14 and 式 15, respectively:

$$Mg\_min = n \times \left(\frac{V_{OUT\_min}}{\frac{V_{DCIN\_max}}{2}} \right) = 3.6 \times \left(\frac{54\ V}{\frac{410\ V}{2}} \right) = 0.948 \tag{14}$$

$$Mg\_max = n \times \left(\frac{V_{OUT\_max}}{\frac{V_{DCIN\_max}}{2}} \right) = 3.6 \times \left(\frac{54\ V}{\frac{300\ V}{2}} \right) = 1.296 \tag{15}$$

2.3.2.4 Determine Equivalent Load Resistance of Resonant Network

To determine the equivalent load resistance at nominal and peak load under nominal output voltage and peak output voltage, use 式 16:

$$R_E = \frac{8 \times n^2}{\pi^2} \times \left(\frac{V_{OUT_{nom}}}{I_{OUT_{nom}}} \right) = \frac{8 \times 3.6^2}{\pi^2} \times \left(\frac{54}{18.52} \right) = 30.63\ \Omega \tag{16}$$

2.3.2.5 Select L_M/L_R Ratio (L_N) and Q_E

L_N is the ratio between the magnetizing inductance and the resonant inductance.

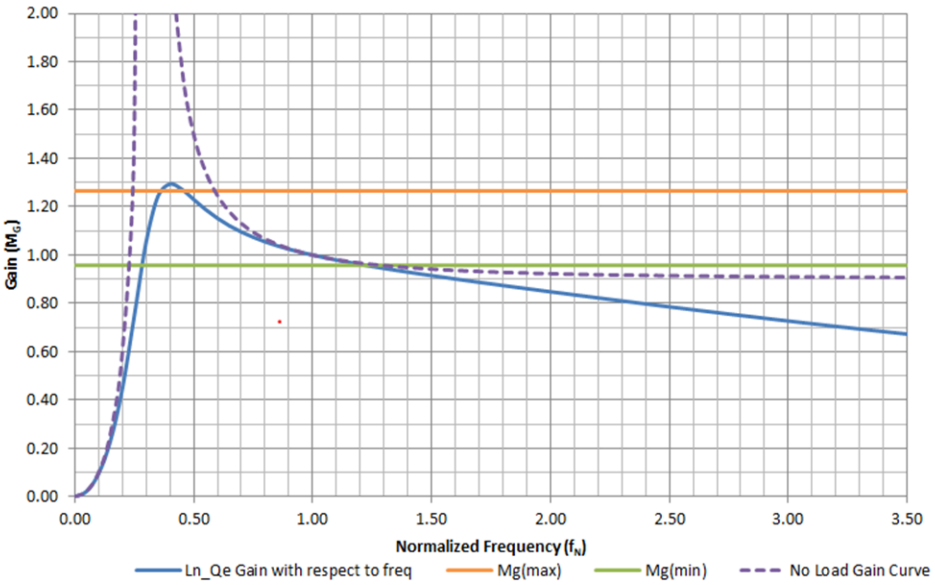
$$L_N = \frac{L_M}{L_R} \tag{17}$$

Q_E is the quality factor of the resonant tank.

$$Q_E = \frac{\sqrt{\frac{L_R}{C_R}}}{R_E} \tag{18}$$

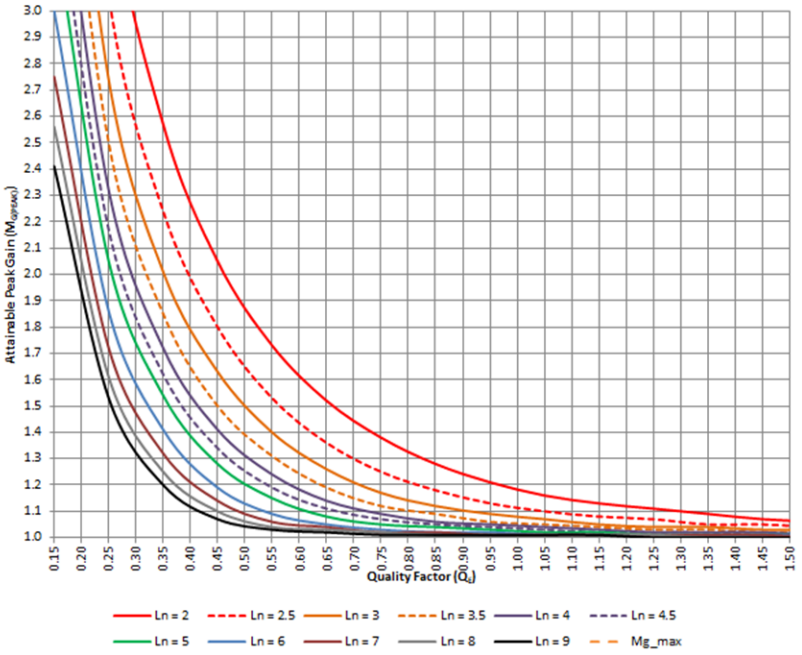
Selecting L_N and Q_E values must result in an LLC gain curve, as shown in 図 2, that intersects with Mg_{min} and Mg_{max} traces. The peak gain of the resulting curve must be larger than Mg_{max}.

図 2. LLC Gain Curve for Selected L_N and Q_E



The relationship between Mg_{peak} and Q_E with respect to L_N is shown in 図 3:

図 3. MG_{peak} and Q_E With Respect to L_N



L_N = 8

Q_E = 0.24

Use the spreadsheet to get optimized values of L_N and Q_E.

2.3.2.6 Switching Frequency

The wide switching frequency of the UCC256403 is from 35 kHz to 1 MHz, which makes this reference design more flexible. To ensure that the temperature rise of the LLC stage is not too high, reduce the loss of the transformer, inductor, and power MOS. The resonant frequency is chosen to be 100 kHz for the consideration of magnetic loss and switching loss.

$$f_0 = 100\,kHz \tag{19}$$

$$C_R = \frac{1}{2\pi \times Q_E \times f_0 \times R_E} = \frac{1}{2\pi \times 0.31 \times 100\,kHz \times 30.63\,\Omega} = 0.168\,uF \tag{20}$$

$$L_R = \frac{1}{(2\pi \times f_0)^2 \times C_R} = \frac{1}{(2\pi \times 100\,kHz)^2 \times 0.164\,uF} = 15.45\,uH \tag{21}$$

$$L_M = L_N \times L_R = 9 \times 15.45\,uH = 139\,uH \tag{22}$$

After the preliminary parameters are selected, find the closest actual component value that is available, recheck the gain curve with the selected parameters, and then run the time domain simulation to verify the circuit operation. This results in the following resonant tank parameters:

$$C_R = 0.164\,uF \tag{23}$$

$$L_R = 16\,uH \tag{24}$$

$$L_M = 144\,uH \tag{25}$$

Based on the final resonant tank parameters, the resonant frequency can be calculated as follows:

$$f_0 = \frac{1}{2\pi \times \sqrt{C_R \times L_R}} = \frac{1}{2\pi \times \sqrt{0.164\,uF \times 16\,uH}} = 98.3\,kHz \tag{26}$$

2.3.2.7 LLC Primary Side Currents

The primary-side RMS load current at full load is determined by:

$$I_{pri} = \frac{\pi}{2\sqrt{2}} \times \frac{I_o}{n} = \frac{\pi}{2\sqrt{2}} \times \frac{1.1 \times 18.52\,A}{3.6} = 6.286\,A \tag{27}$$

The RMS magnetizing current at $f_{sw(min)}$ = 44.2 kHz is determined by:

$$I_m = \frac{2\sqrt{2}}{\pi} \times \frac{n \times V_{OUT}}{2\pi \times fsw(min) \times L_M} = \frac{2\sqrt{2}}{\pi} \times \frac{3.6 \times 54\,V}{2\pi \times 44.2\,kHz \times 144\,uH} = 4.375\,A \tag{28}$$

The current of the resonant circuit is determined by:

$$I_r = \sqrt{I_m{}^2 + I_{pri}{}^2} = 7.658\,A \tag{29}$$

This calculation is also the transformer's primary winding current at $f_{sw(min)}$.

2.3.2.8 LLC Secondary Side Currents

The total secondary-side RMS load current is the current referred from the primary-side current to the secondary side.

$$I_{sec} = n \times I_{pri} = 3.6 \times 6.286\,A = 22.629\,A \tag{30}$$

Because the transformer's secondary side has a center-tapped configuration, this current is split equally into two transformer windings on the secondary side. The current of each winding is then calculated as:

$$I_{sw} = \frac{\sqrt{2} \times I_{sec}}{2} = \frac{\sqrt{2} \times 22.629\,A}{2} = 16\,A \tag{31}$$

The corresponding half-wave average current is:

$$I_{savg} = \frac{\sqrt{2} \times I_{sec}}{\pi} = \frac{\sqrt{2} \times 22.629\ A}{\pi} = 10.185\ A \quad (32)$$

2.3.2.9 Select the Transformer

The transformer can be built or purchased from a catalog. The specifications for this example are as follows:

- Turns ratio (n): 3.6
- Primary terminal voltage: 450-V AC
- Primary magnetizing inductance: L_M = 144 µH
- Primary winding's rated current, I_{wp} = 7.658 A
- Secondary terminal voltage: 54-V AC
- Secondary winding's rated current, I_{ws} = 16 A (center-tapped configuration)
- Minimum switching frequency: 44.2 kHz
- Maximum switching frequency: 118 kHz
- Insulation between primary and secondary sides: IEC 60950 reinforced insulation

2.3.2.10 Select the Resonant Inductor

The inductor can be built or purchased from a catalog with these specifications:

- Series resonant inductance, Lr = 16 µH
- Rated current, I_{Lr} = 7.658 A
- Terminal AC voltage: 34 V

$$V_{Lr} = \omega \times L_R \times I_r = 2\pi \times 44.2\,kHz \times 16\,H \times 7.658\ A = 34\ V \quad (33)$$

2.3.2.11 Select the Resonant Capacitor

This capacitor carries the full-primary current at a high frequency. A low dissipation factor part is needed to prevent overheating in the part.

The AC voltage across the resonant capacitor is given by its impedance times the current.

$$V_{CR} = \frac{I_r}{\omega \times C_R} = \frac{7.658\ A}{2\pi \times 44.2\,kHz \times 0.164\,uF} = 168.1\,V \quad (34)$$

$$V_{CR(rms)} = \sqrt{\left(\frac{V_{IN(max)}}{2}\right)^2 + {V_{CR}}^2} = \sqrt{\left(\frac{410\ V}{2}\right)^2 + 168.1\,V^2} = 265.1\,V \quad (35)$$

$$V_{CR(peak)} = \frac{V_{IN(max)}}{2} + \sqrt{2} \times V_{CR} = \frac{410\ V}{2} + \sqrt{2} \times 168.1\,V = 442.7\ V \quad (36)$$

$$V_{CR(valley)} = \frac{V_{IN(max)}}{2} - \sqrt{2} \times V_{CR} = \frac{410\ V}{2} - \sqrt{2} \times 168.1\,V = -32.7\ V \quad (37)$$

Rated current I_r = 7.658 A

2.3.2.12 Select the Primary Side MOSFETs

Each MOSFET detects the input voltage as its maximum applied voltage. Choose the MOSFET voltage rating to be 1.5 times of the maximum bulk voltage.

$$V_{DS} = 1.5 \times V_{IN(max)} = 1.5 \times 410 = 615\ V \quad (38)$$

Choose the MOSFET current rating to be 1.1 times of the maximum primary side RMS current.

$$I_D = 1.1 \times I_r = 1.1 \times 7.658 = 8.424\ A \quad (39)$$

For the LLC power stage working in ZVS, the turnon losses can be neglected. The choice of MOSFET must be based on R_{dson} and C_{oss}. Optimizing the Coss helps in minimizing the dead time required for achieving ZVS, thereby minimizing duty cycle loss. The feature that optimizes the adaptive dead time of the UCC256403 helps in maximizing the duty cycle, thereby improving efficiency.

2.3.2.13 Select the Secondary Side MOSFETs

The secondary-side rectifier voltage rating is determined by:

$$V_{DS\_sec} = 1.2 \times 2 \times V_{OUT\_max} = 1.2 \times 2 \times 54\ V = 130\ V \quad (40)$$

The current rating of the secondary-side MOSFET is determined by:

$$I_{D\_sec} = 10.185\ A \quad (41)$$

This reference design uses 150-V MOS with its low R_{dson} (7.6 mΩ) and Q_g (21 nC). The very low R_{dson} helps in reducing the overall loss in the synchronous rectifier.

2.3.2.14 LLC Output Capacitors

The LLC converter topology does not require an output filter, although a small second-stage filter inductor can be useful in reducing peak-to-peak output noise. Assuming that the output capacitors carry the full wave output current of the rectifier, the capacitor ripple current rating is:

$$I_{RECT} = \frac{\pi}{2\sqrt{2}} \times I_O = 1.11 \times 18.52 = 20.56\ A \quad (42)$$

Use an 80-V rating for a 54-V output voltage.

The RMS current rating of the capacitor is:

$$I_{C(out)} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times I_O\right)^2 - {I_O}^2} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times 18.52\ A\right)^2 - 18.52\ A^2} = 8.95\ A \quad (43)$$

The ripple current rating for a single capacitor may not be sufficient, so multiple capacitors are often connected in parallel.

$$ESR_{max} = \frac{V_{OUT(pk-pk)}}{I_{RECT(pk)}} = \frac{0.2\ V}{\frac{\pi}{2} \times 18.52\ A} = 6.875\ m\Omega \quad (44)$$

The capacitor specifications are:

- Voltage rating: 80 V
- Ripple current rating: 8.95 A
- ESR is less than 6.875 mΩ

2.3.2.15 BLK Pin Voltage Divider

The BLK pin senses the LLC input voltage and determines when to turn on and off the LLC converter. Different versions of the UCC25640 have different BLK thresholds. Choose the bulk startup voltage at 360 V, then the BLK resistor divider ratio can be calculated:

$$K_{BLK} = \frac{360\ V}{3.05\ V} = 118 \tag{45}$$

The desired power consumption of the BLK pin resistor is P_{BLKsns} = 10 mW. The total value of the BLK sense resistor is given by:

$$R_{BLKsns} = \frac{V_{IN(nom)}^{2}}{P_{BLK(sns)}} = \frac{390^{2}}{0.01} = 15.21M\Omega \tag{46}$$

The lower BLK divider resistor value is given by:

$$R_{BLKlower} = \frac{R_{BLKsns}}{K_{BLK}} = \frac{15.21M\Omega}{118} = 129\,k\Omega \tag{47}$$

The actual value used is 142.1 kΩ. The higher BLK divider resistor value is given by:

$$R_{BLKUPPER} = R_{BLKsns} - R_{BLKlower} = 15.1M\Omega \tag{48}$$

The actual value used is 15.3 MΩ.

2.3.2.16 Current Sense Circuit (ISNS Pin)

The ISNS pin sets the overcurrent protection level. OCP1 is peak current protection level; OCP2 and OCP3 are average current protection levels. The threshold voltages are 0.425 V, 0.56 V, and 4.03 V, respectively. Set the OCP3 level at 140% of full load. Thus, the sensed average input current level at full load is given by:

$$V_{ISNSfullload} = \frac{0.425\ V}{150\%} = 0.3\ V \tag{49}$$

The current sense ratio can then be calculated:

$$K_{ISNS} = \frac{V_{ISNSfullload}}{\frac{P_{OUT}}{\eta} \times \frac{1}{V_{DCBUS\_nom}}} = \frac{0.3\ V}{\frac{1000\ W}{0.97} \times \frac{1}{390\ V}} = 0.11\Omega \tag{50}$$

Select a current sense capacitor first because there are fewer high-voltage capacitor choices than resistors. C_{ISNS} = 330 pF

Then calculate the required ISNS resistor value:

$$R_{ISNS} = \frac{K_{ISNS} \times C_R}{C_{ISNS}} = 56\,\Omega \tag{51}$$

To realize the power boost function, the current sense resistor must be smaller. The actual value of the current sense resistor used is 51 Ω.

2.3.2.17 Auxiliary PSU

This reference design has the additional auxiliary PSU to provide the bias power to the PFC, LLC, SR, meter circuit, and other logic circuits on the board. The converter is powered from the output of the PFC pre-regulator stage and must be able to start up prior to the PFC stage being operational. For this reason, the circuit is designed to operate over a wide input voltage, 100- to 450-V DC. The flyback transformer has three output windings, which are isolated to each other.

2.3.3 Input Power Meter Design

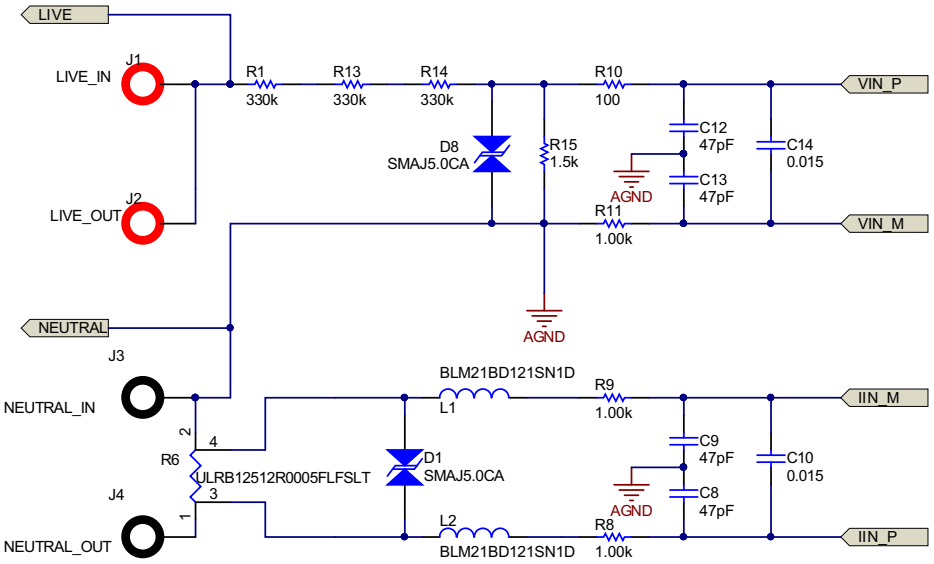
The MSP430I2021 is an ultra-low-power mixed signal microcontroller. It integrates with two independent, differential-input, 24-bit, sigma-delta, analog-to-digital converters (ADCs) with programmable gain amplifiers, a 16-bit hardware multiplier. An eUSCI_A0 supports universal asynchronous receiver/transmitter (UART) and serial peripheral interface (SPI) communication interfaces. An eUSCI_B0 supports SPI, inter-integrated circuit (I2C) communication interfaces, two 16-bit timers, and 12 general-purpose input and output GPIO pins in a 28-pin TSSOP or 16 GPIO pins in a 32-pin QFN package. The peripheral set is a good combination for embedded electricity power measurement. In such an application, the device is embedded in the end application and measure the electricity, which provides the device information about the voltage, current, power consumption, and so forth.

2.3.3.1 Interface Circuit Design

In the design of a metering circuit, a key success factor is to yield sufficient accuracy and is dependant on a good sampling circuit. The 24-bit, sigma-delta AD Converter (SD24) on the MSP430I2021, together with the on-chip programmable gain amplifier, provides the critical hardware for getting high quality AD conversion results from both the current and voltage sensor. Moreover, the interface circuit, the component selection, and the circuit layout also play a crucial role for a successful design. Due to the nature of a sigma-delta AD converter, and of the voltage and current signal being measured, an external interface circuit is needed to interface the voltage and current to keep the SD24 ADC to work properly and provide proper filtering for band of interest. In TIDM-SERVER-PWR-MON reference design, it uses MSP430i2041 whereas in this 5G telecom power supply application, we recommend MSP430i2021 since only two ADCs are required, not four ADCs.

The hardware of the interface circuit is simple, which is composed of passive components apart from the protection diode. The protection diode is not required unless, for example, a high shunt resistor value or a current transformer is in use instead of the current sensor, and a significant current surge that causes enough voltage across the sensor to damage the MCU is anticipated. L1, R9, and C9 form a low-pass filter, having bandwidth of a few MHz. The purpose of this filter is to reject radio frequency interference from going into the sigma-delta ADC. The filter formed by L2, R8, and C8 has the same characteristic, which is balanced for the differential signal. The filter formed by R9, R8, and C10 is a filter that gives the bandwidth of about 10 kHz, which is the filter for the band of interest. The order of magnitude of these capacitors should be observed; the actual value of the capacitance is not critical. The voltage sensor interface is a resistor ladder. The ratio of the resistance in the resistor ladder allows up to 265-V AC to be measured.

図 4. Voltage and Current Sensor Interface Circuit



2.3.3.2 *Shunt Resistor*

For an accurate measurement, the choice of shunt is another important factor. In general, it is suggested that a shunt of smaller value is a better choice. Smaller shunt value benefits the power dissipated on the shunt and the respective rise in temperature. The lower rise in temperature reduces the need for a very low temperature coefficient shunt resistor to sustain the accuracy over temperature. However, there is also the drawback of using a small value shunt that the signal-to-noise ratio of a small value shunt is worse than using a larger value one. In this sense, there may be chance that a shunt of higher value is desired, for example, when measuring a very small current and the range of current to be measured is also in a small range. In this design, a few factors are considered: the maximum current, the current dynamic range, and the power dissipation. In this application, the maximum current for each socket is 6.5 A, and the desired dynamic range of current keeping a flat error percentage is 1000:1. It is preferred that the power dissipated on the shunt resistor be as small as possible.

To achieve the best accuracy, have the current signal present to the SD24 ADC the maximum swing when measuring maximum current because the SD24 ADC has an input range of approximately 900 mV at x1 gain. Using x16 gain, the input range for the AC root mean square is:

$$\frac{\left(\frac{900}{16}\right)}{\sqrt{2}} = 39.77\,\text{mV}_{\text{rms}} \tag{52}$$

With this number, 5-mΩ shunt resistance should be good for this input range.

In addition to value, the physical size of the shunt is also an important factor for accuracy— not the size directly, but the heat generated when current is flowing. A smaller-sized shunt heats up more easily due to the limited surface area. If there is significant current to flow though the shunt, TI suggests having a large-enough sized shunt. There should also be sufficient ventilation on the PCB to prevent heat being accumulated. In this design, a 2512-size shunt is chosen.

2.3.3.3 Voltage Divider Circuit

For the voltage sensor circuit, the matter is a little simpler. In this design, the major consideration is that the voltage divider should be able to prevent arcing between the terminals. To reduce the voltage difference between resistor terminals, this design uses 4 resistors to form the voltage divider. Then, the voltage across the top 3 resistors each takes about 1/3 of the AC voltage. Using the 1206 resistor for these 3 resistors provides a greater equivalent distance of separation between the live voltage and bottom resistor.

The installation of the protection diode in the voltage sensor circuit is more important than in the current circuit. The reason is that the resistor ladder on the voltage sensor circuit is more likely to see a voltage surge across bottom low-voltage resistor high enough to damage the MCU. In other cases, if this resistor is an open circuit or in bad contact causing a higher resistance, the voltage across the input of the voltage channel ADC also causes damage to the MCU.

2.3.3.4 TIDM-SERVER-PWR-MON reference design

This TIDM-SERVER-PWR-MON reference design could be a very good example for power metering board design. This design could be directly used to do the power metering. Just put the reference design board at the input port of the power board and connect the power metering board to the computer. The detailed instructions could be found online Energy Measurement Design Center (EMDC). This EMDC tool could help to generate the code based on your own hardware configuration and there is also the library where you can find the example code.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 Hardware

- Power metering: EVM430-i2040S

3.1.2 Software

- Example code is in the EMDC library. Refer to the instruction in Energy Measurement Design Center (EMDC) to download the example code (EVM430-i2040S_SH_1V_1C_50Hz) or generate the code needed.

3.1.3 Testing Conditions

- Input conditions: VIN: 85-V to 265-V AC. Set the input current limit to 8 A.
- Output conditions: Electronic load, 0 to 70 V, 1000 W
- Power metering calibration point: VIN = 230V AC, 4A AC, for example

3.1.4 Equipment Needed

- Isolated AC source
- Single-phase power analyzer
- Digital oscilloscope
- Multimeter
- Electronic load

3.2 Testing and Results

3.2.1 Efficiency and Regulation

3.2.1.1 Performance Data

This section shows the efficiency, power factor, iTHD, and load regulation results at 115-V and 230-V AC input conditions.

表 4 shows the data for VIN = 115-V AC.

表 4. Efficiency and Regulation at 115-V AC

VINAC (V)	IINAC (A)	PINAC (W)	PF	iTHD (%)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFF (%)
115.03	0.55	57.4	0.902	13.00	53.52	0.895	47.897	83.44
114.95	1.03	113.5	0.962	8.29	53.51	1.894	101.348	89.29
114.89	1.45	163.2	0.979	6.76	53.51	2.780	148.749	91.15
114.86	1.93	219.3	0.987	5.75	53.50	3.780	202.245	92.22
114.74	2.37	269.4	0.991	5.23	53.50	4.680	250.389	92.94
114.79	2.85	325.5	0.994	4.89	53.50	5.679	303.827	93.34
114.74	3.29	375.5	0.995	4.67	53.50	6.566	351.261	93.54
114.68	3.73	426.3	0.996	4.53	53.50	7.467	399.455	93.70
114.64	4.23	483.1	0.997	4.36	53.49	8.466	452.872	93.74
114.62	4.67	533.9	0.997	4.18	53.49	9.352	500.201	93.69

表 5 shows the data for VIN = 230-V AC.

表 5. Efficiency and Regulation at 230-V AC

VINAC (V)	IINAC (A)	PINAC (W)	PF	iTHD (%)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFF (%)
230.15	0.62	112.3	0.79	12.08	53.48	1.900	101.610	90.48
230.11	1.02	215.8	0.90	10.54	53.48	3.785	202.410	93.80
230.04	1.46	320.0	0.95	9.04	53.48	5.684	303.952	94.98
229.98	1.90	423.9	0.97	7.15	53.48	7.569	404.767	95.49
229.89	2.35	528.0	0.98	6.21	53.48	9.468	506.311	95.89
229.86	2.80	633.0	0.98	5.73	53.48	11.354	607.178	95.92
229.88	3.25	738.0	0.99	5.41	53.48	13.239	707.969	95.93
229.82	3.71	844.0	0.99	5.25	53.48	15.138	809.535	95.92
229.78	4.15	945.0	0.99	5.16	53.48	16.926	905.152	95.78
229.76	4.57	1040.0	0.99	5.1	53.48	18.616	995.528	95.72

3.2.1.2 Performance Curves

The following figures show the graphs for efficiency, power factor, and iTHD, respectively.

図 5. Efficiency at 230-V AC

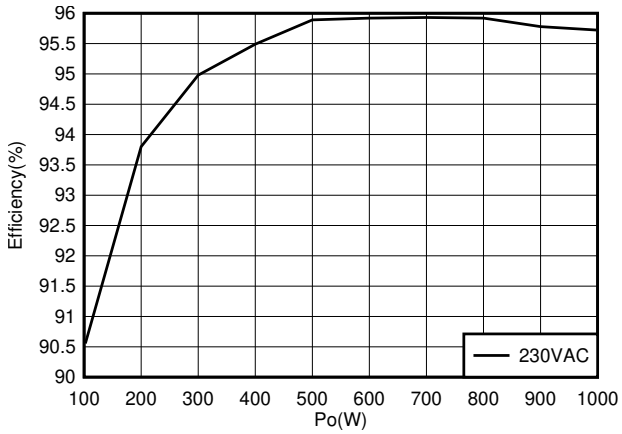


図 6. Efficiency at 115-V AC

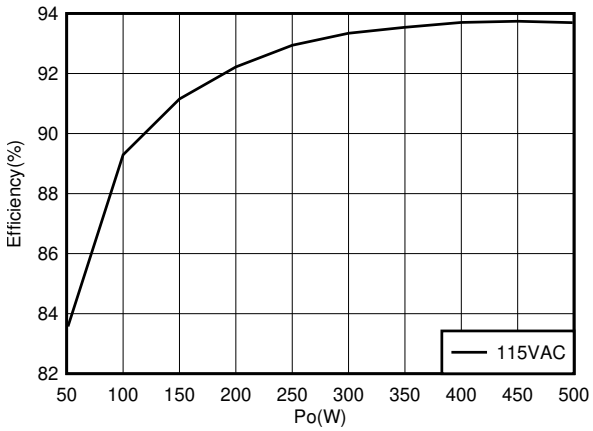


図 7. Power Factor at 230-V AC

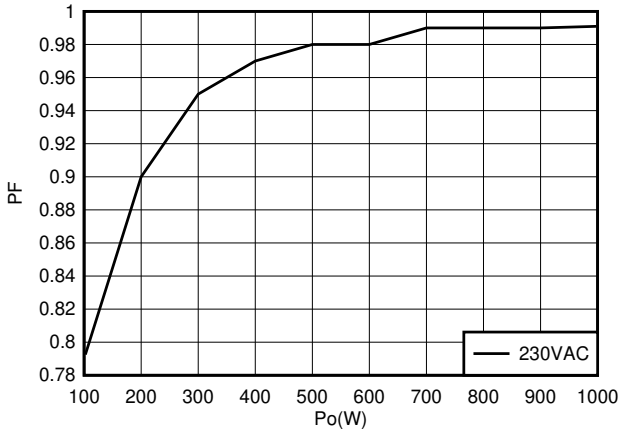


図 8. Power Factor at 115-V AC

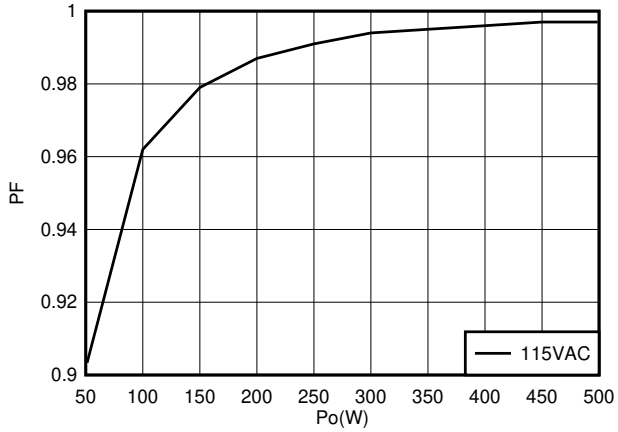


図 9. iTHD at 230-V AC

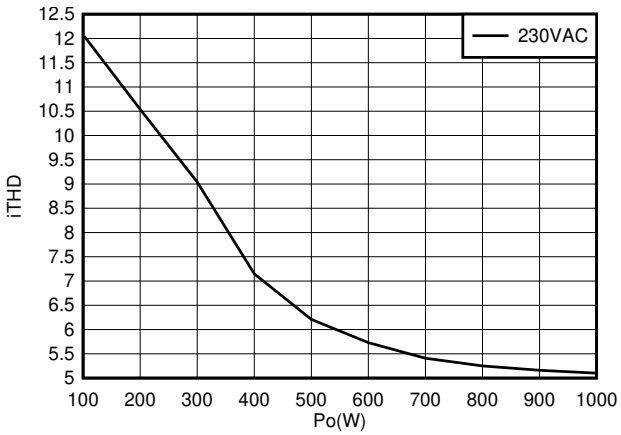
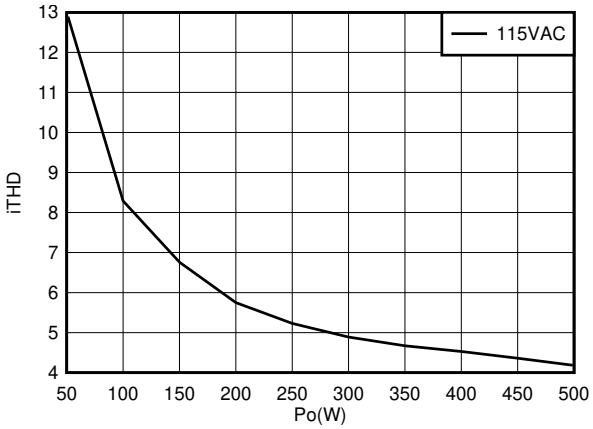


図 10. iTHD at 115-V AC



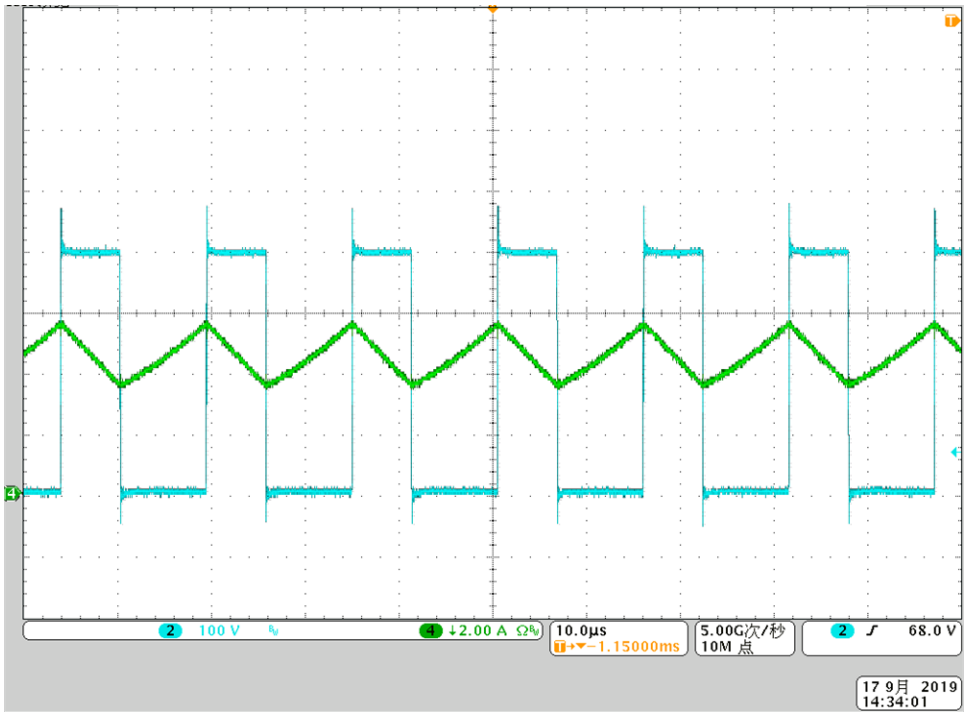
3.2.2 Switching Waveforms

3.2.2.1 PFC Stage Switching Waveforms

This section shows the PFC stage switching waveforms at an input voltage of 115-V AC and 230-V AC at different load conditions.

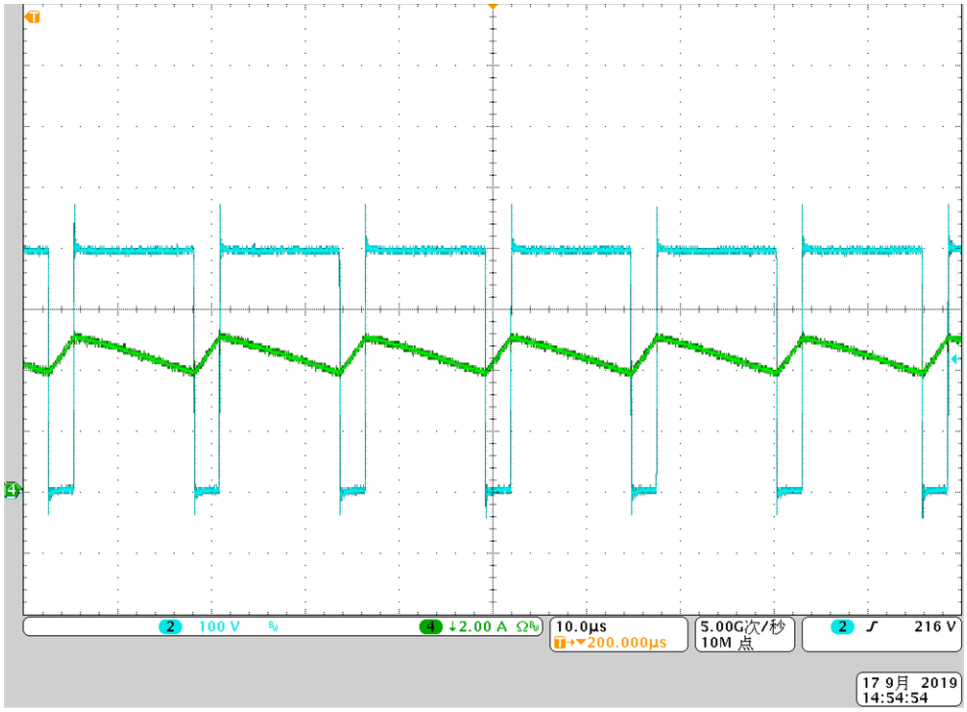
注: CH2: PFC switch node voltage (100 V/div, bandwidth: 20 MHz);
CH4: PFC inductor current (2 A/div, bandwidth: 20 MHz);
Test condition: VIN = 230-V AC/50 Hz; I_{OUT} = 100% load

図 11. PFC Inductor Current and Switching Node Waveform at 230-V AC, 1000 W



注: CH2: PFC switch node voltage (100 V/div, bandwidth: 20 MHz);
CH4: PFC inductor current (2 A/div, bandwidth: 20 MHz);
Test condition: VIN = 115-V AC/60 Hz; I_{OUT} = 100% load (derating)

図 12. PFC Inductor Current and Switching Node Waveform at 115-V AC, 500 W



3.2.2.2 LLC Stage Switching Waveforms

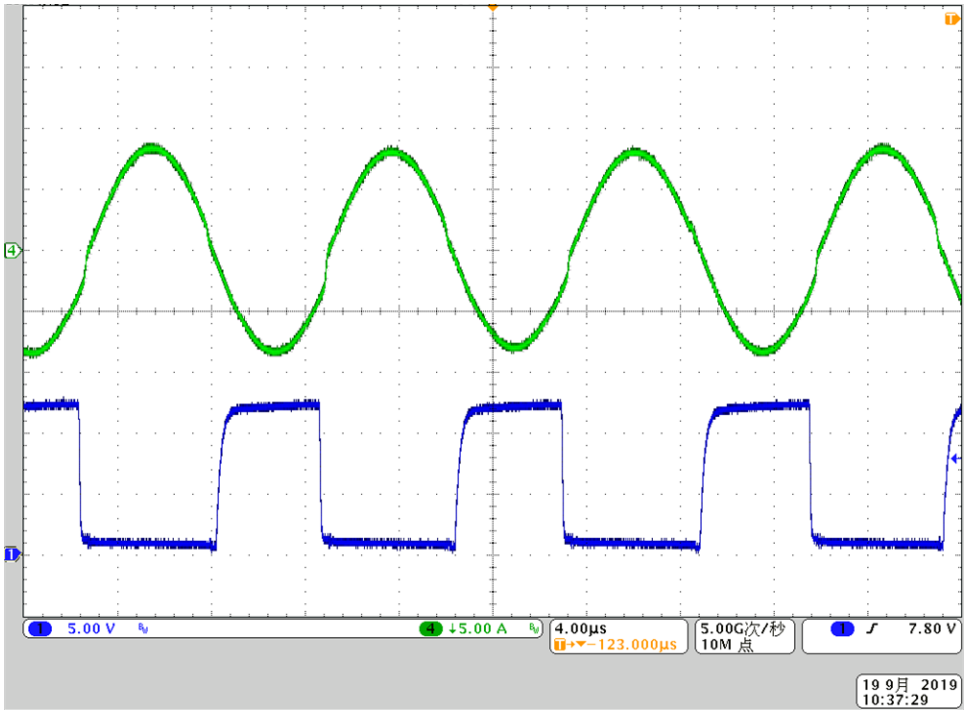
This section shows the LLC-stage, primary-side switching waveforms at an output voltage of 24-V AC at different load conditions.

注: CH2: Low side PWM (5 V/div, bandwidth: 20 MHz);

CH4: LLC resonant current (5 A/div, bandwidth: 20 MHz);

Test condition: VIN = 230-V AC/50 Hz; I_{OUT} = 100% load

図 13. Low-Side PWM and Resonant Current at Full Load



3.2.2.3 LLC Secondary Side Synchronous Drive Waveform

The synchronous drive output waveforms and the resonant current are shown in the following figures.

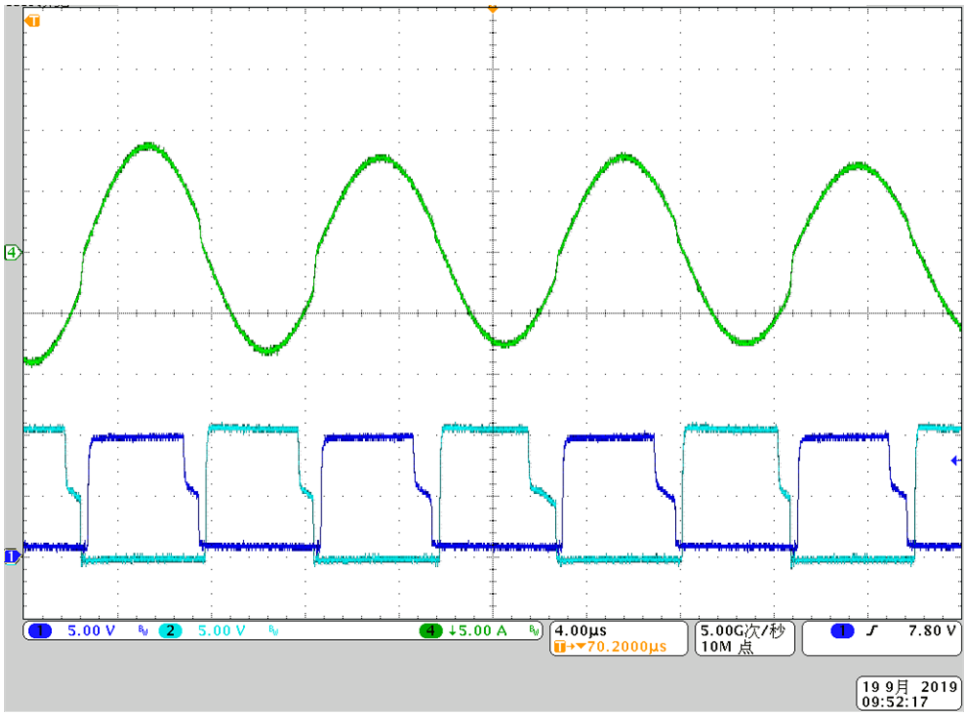
注: CH1: Gate driver of SR1 (5 V/div, bandwidth: 20 MHz);

CH2: Gate driver of SR2 (5 V/div, bandwidth: 20 MHz);

CH4: LLC resonant current (5 A/div, bandwidth: 20 MHz);

Test condition: VIN = 230-V AC/50 Hz; I_{OUT} = 100% load

図 14. SR Rectifier Gate Driver



3.2.3 Input Waveforms

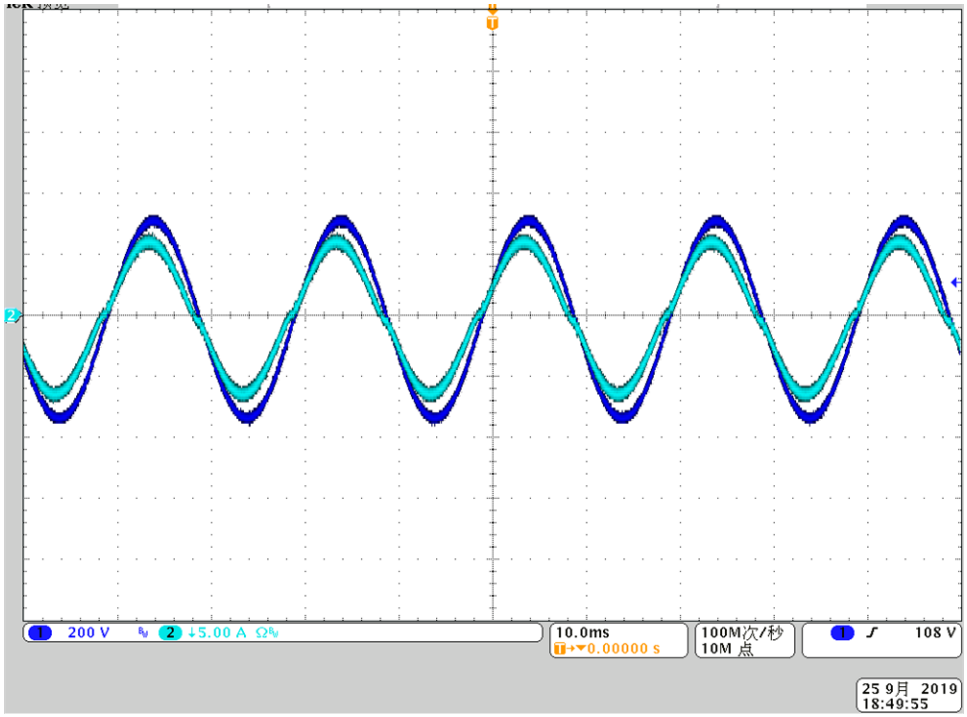
図 15 and 図 16 show the input current waveform at 230-V AC and 115-V AC at full load conditions, respectively.

注: CH1: Input voltage (200 V/div, bandwidth: 20 MHz);

CH2: Input current (5 A/div, bandwidth: 20 MHz);

Test condition: VIN = 230-V AC/50 Hz; I_{OUT} = 100% load

図 15. Input Voltage and Current at 230-V AC, 1000 W

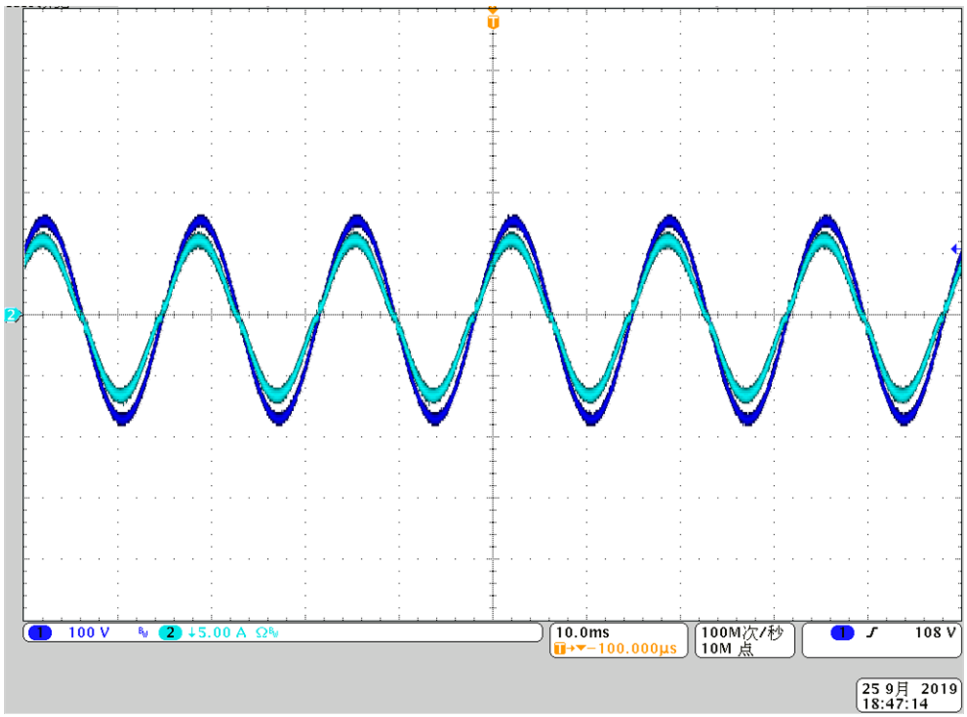


注: CH1: Input voltage (100 V/div, bandwidth: 20 MHz);

CH2: Input current (5 A/div, bandwidth: 20 MHz);

Test condition: VIN = 115-V AC/60 Hz; I_{OUT} = 100% load (derating)

図 16. Input Voltage and Current at 115-V AC, 500 W



3.2.4 Start-up Waveforms

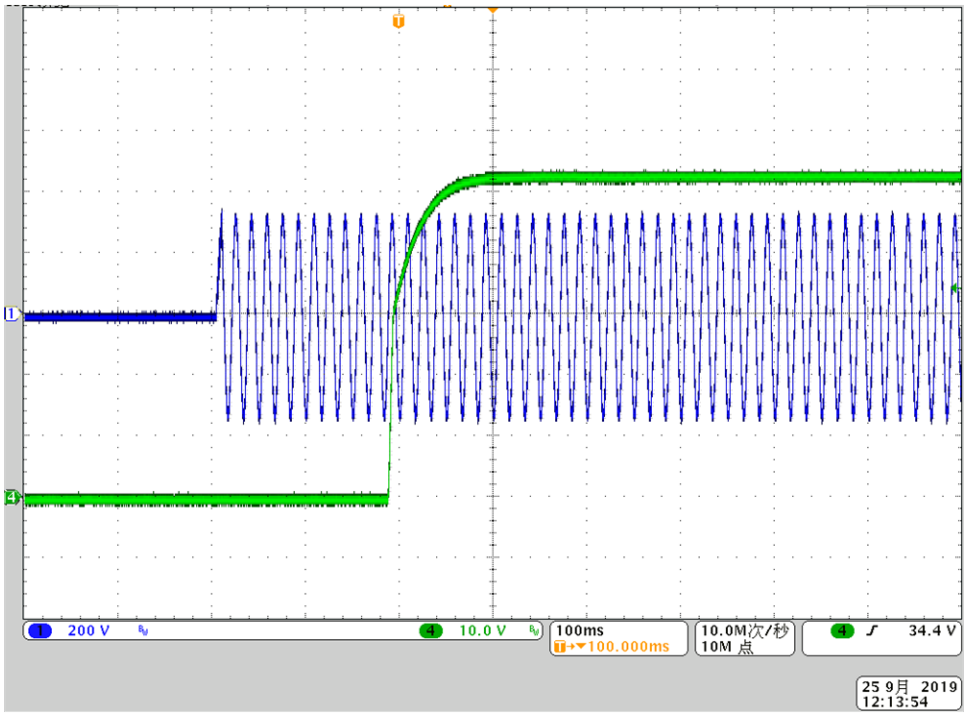
The startup waveform showing the 54-V output voltage and the input AC voltage .

注: CH4: Output voltage (10 V/div, bandwidth: 20 MHz);

CH1: Input voltage (200 V/div, bandwidth: 20 MHz);

Test condition: VIN = 230-V AC/50 Hz; I_{OUT} = 100% load.

図 17. Startup Waveform at VINAC = 230-V AC and 1000 W

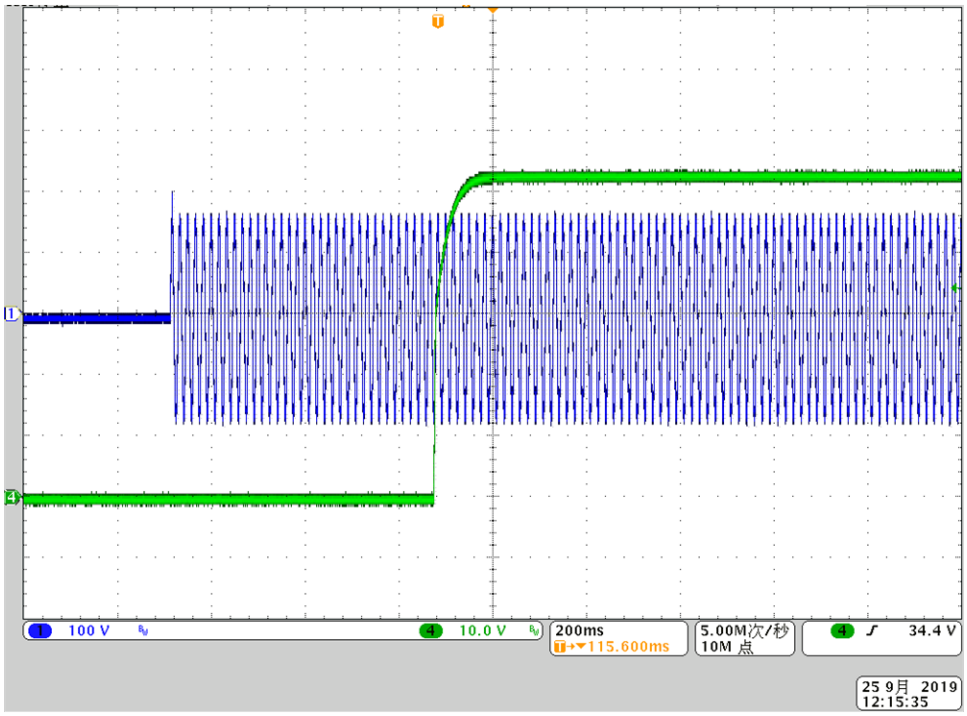


注: CH4: Output voltage (10 V/div, bandwidth: 20 MHz);

CH1: Input voltage (100 V/div, bandwidth: 20 MHz);

Test condition: VIN = 115-V AC/60 Hz; I_{OUT} = 100% load (derating)

図 18. Startup Waveform at VINAC = 115-V AC and 500 W



3.2.5 Dynamic Load Characteristics

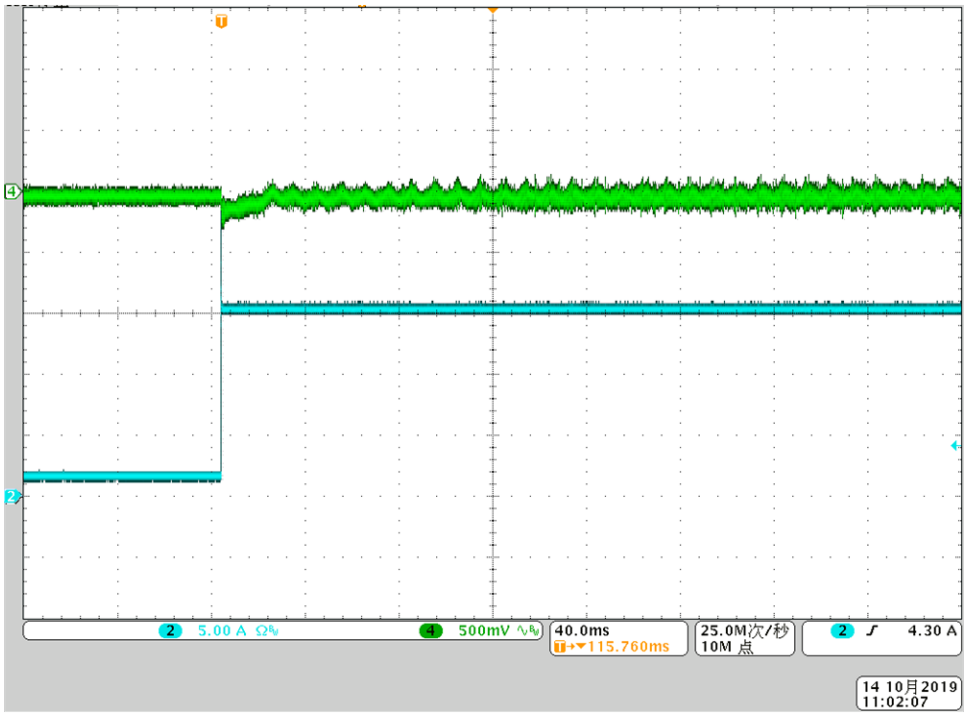
Load transient performance is observed using an electronic load. The converter is operating at an input voltage of 230-V AC and an output voltage of 54-V DC.

注: CH4: Output voltage in AC level (500 mV/div, bandwidth: 20 MHz);

CH2: Output current (5 A/div, bandwidth: 20 MHz);

Test condition: VIN = 230-V AC/50 Hz; I_{OUT} = from 10% to 90% load, 2 A/us

図 19. Transient Response From 10% to 90% Load

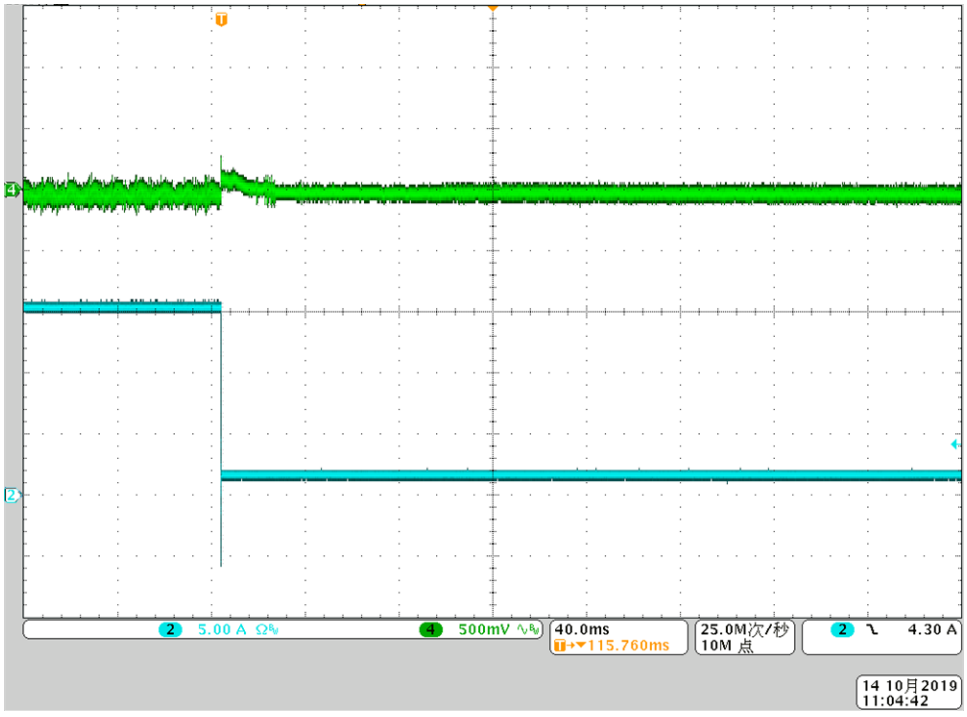


注: CH4: Output voltage in AC level (500 mV/div, bandwidth: 20 MHz);

CH2: Output current (5 A/div, bandwidth: 20 MHz);

Test condition: VIN = 230-V AC/50 Hz; I_{OUT} = from 90% to 10% load, 2 A/us

図 20. Transient Response From 90% to 10% Load

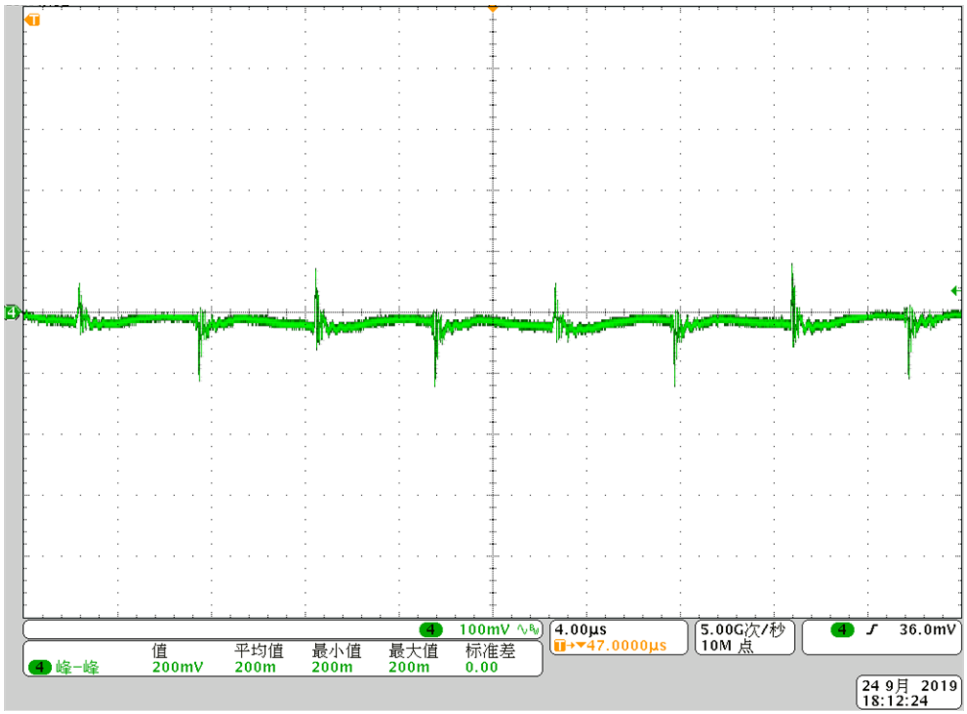


3.2.6 Output Ripple

図 21 shows the output voltage ripple at full load conditions at a 230-V AC input.

注: CH4: Output ripple (100 mV/div, bandwidth: 20 MHz);
Test condition: VIN = 230-V AC/50 Hz; I_{OUT} = 100% load

図 21. Output Ripple With 1000 W at VINAC = 230-V AC



3.2.7 Input Power Metering Test

表 6 and 表 7 show the input power accuracy at room temperature. The results are tested with TIDM-SERVER-PWR-MON reference board.

表 6. Input Power Metering Test Result at 230-V AC

Vin	Vin_read	VOLTAGE ERROR	VOLTAGE (%)	Iin	Iin_read	CURRENT ERROR	CURRENT (%)	Pin	Pin_mcu	POWER ERROR	POWER (%)
230.28	230.322	-0.042	-0.018	0.5356	0.532	0.0036	0.672	110.2	111.257	-1.057	-0.959
230.21	230.251	-0.041	-0.018	0.9571	0.953	0.0041	0.428	213.0	214.621	-1.621	-0.761
230.16	230.204	-0.044	-0.019	1.3818	1.379	0.0028	0.203	311.6	313.492	-1.892	-0.607
230.1	230.157	-0.057	-0.025	1.829	1.825	0.004	0.219	415.5	417.304	-1.804	-0.434
230.03	230.087	-0.057	-0.025	2.277	2.275	0.002	0.088	519	521.531	-2.531	-0.488
229.98	230.039	-0.059	-0.026	2.733	2.731	0.002	0.073	624	627.163	-3.163	-0.507
229.94	229.992	-0.052	-0.023	3.189	3.187	0.002	0.063	729	732.263	-3.263	-0.448
229.85	229.922	-0.072	-0.031	3.65	3.648	0.002	0.055	835	838.574	-3.574	-0.428
229.78	229.875	-0.095	-0.041	4.112	4.11	0.002	0.049	941	944.051	-3.051	-0.324
229.89	229.922	-0.032	-0.014	4.479	4.477	0.002	0.045	1025	1029.53	-4.53	-0.442

表 7. Input Power Metering Test Result at 115-V AC

Vin	Vin_read	VOLTAGE ERROR	VOLTAGE (%)	Iin	Iin_read	CURRENT ERROR	CURRENT (%)	Pin	Pin_read	POWER ERROR	POWER (%)
115.13	115.039	0.091	0.079	0.5626	0.559	0.0036	0.640	61.9	61.929	-0.029	-0.047
115.04	114.992	0.048	0.042	1.0364	1.033	0.0034	0.328	117.3	117.344	-0.044	-0.038
114.99	114.922	0.068	0.059	1.5135	1.510	0.0035	0.231	172.8	172.961	-0.161	-0.093
114.93	114.851	0.079	0.069	1.9888	1.985	0.0038	0.191	227.8	227.876	-0.076	-0.033
114.87	114.804	0.066	0.057	2.474	2.472	0.002	0.081	283.6	283.541	0.059	0.021
114.80	114.733	0.067	0.058	2.963	2.960	0.003	0.101	339.4	339.514	-0.114	-0.034
114.76	114.663	0.097	0.085	3.454	3.452	0.002	0.058	395.8	395.903	-0.103	-0.026
114.67	114.592	0.078	0.068	3.944	3.941	0.003	0.076	451.6	451.802	-0.202	-0.045
114.59	114.545	0.045	0.039	4.442	4.441	0.001	0.023	509	508.821	0.179	0.035

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010081.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010081.

4.3 PCB Layout Recommendations

Key guidelines for routing power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high-frequency switching currents, on both the primary and secondary sides of the converter. This helps reduce EMI and improve converter overall performance.
- Keep traces with high dV/dt potential and high dI/dt capability away from or shielded from sensitive signal.
- Keep power ground and control ground separated for each power supply stage. If they are electrically connected, tie them together at one point near the DC input return or output return of the given stage correspondingly.
- When multiple capacitors are used in parallel for current sharing, the layout must be symmetrical across both leads of the capacitors. If the layout is not identical, the capacitor with the lower series trace impedance will see higher currents and become hotter.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device. The devices are intended for protection and hence must be routed with short traces to reduce inductance.
- Choose the width of PCB traces based on acceptable temperature rise at the rated current per IPC2152 as well as acceptable DC and AC impedances. Also, the traces must withstand the fault currents (such as short-circuit current) before the activation of electronic protection such as a fuse or circuit breaker.
- Determine the distances between various circuits according to the requirements of applicable standards such as the UL60950.
- Adapt thermal management to fit the end-equipment requirements.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010081.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010081.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010081.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010081.

5 Related Documentation

1. Texas Instruments, *UCC25640x LLC Resonant Controller With Ultra-Low Audible Noise and Standby Power Data Sheet*
2. Texas Instruments, *UCC24624 Dual-Channel Synchronous Rectifier Controller for LLC Resonant Converters Data Sheet*
3. Texas Instruments, *UCC2751x Single-Channel, High-Speed, Low-Side Gate Driver (With 4-A Peak Source and 4-A Peak Sink) Data Sheet*
4. Texas Instruments, *TLV900x Low-Power, RRIO, 1-MHz Operational Amplifier for Cost-Sensitive Systems Data Sheet*
5. Texas Instruments, *MSP430i204x, MSP430i203x, MSP430i202x Mixed-Signal Microcontrollers Data Manual*

5.1 商標

5.2 Third-Party Products Disclaimer

6 About the Author

HUIXIN WANG is a systems engineer at Texas Instruments, where she is responsible for developing reference design solutions for the power delivery, industrial segment. Huixin earned her master of technology degree in power electronics from Zhejiang University.

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2019年11月発行のものから更新 **Page**

- the TIDA-010081 block diagram 変更 4

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265