参考資料

Design Guide: TIDA-010210

6.6kW、3 相、3 レベル ANPC インバータ / PFC 双方向電力段のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインは、SiC/GaN (シリコン・カーバイド / 窒化ガリウム) をベースとする 3 レベルの 3 相 ANPC (Advanced Neutral Point Clamped、高度な中性点クランプ) インバータ電力段を実装するための設計テンプレートを提示します。高速スイッチング・パワー・デバイスを使用すると、100kHz を上回る高周波数でパワー・デバイスのスイッチングを実施できます。この場合、フィルタで使用する磁気素子のサイズを小型化し、電力段の電力密度を高めることができます。マルチレベル・トポロジー採用により、600V 定格のパワー・デバイスを、最大 1,000V というそれより高い DC バス電圧で使用できるようになります。スイッチング電圧ストレスが低いことでスイッチング損失の低減につながり、その結果、98.5% というピーク効率を達成しています。このデザインはモジュール型の構造を採用しており、同じフィルタ段を使用して、SiC または GaN のパワー・デバイスとの組み合わせで動作するように構成することが可能です。

リソース

TIDA-010210	デザイン・フォルダ
LMG3410R050	プロダクト・フォルダ
UCC21530、UCC21541	プロダクト・フォルダ
TMDSCNCD280049C	ツール・フォルダ
TMS320F280049C	プロダクト・フォルダ
AMC3302、OPA4376	プロダクト・フォルダ
ISO7721、SN6501	プロダクト・フォルダ
TPS563200、LP5907	プロダクト・フォルダ
TLV9004、LMT87	プロダクト・フォルダ

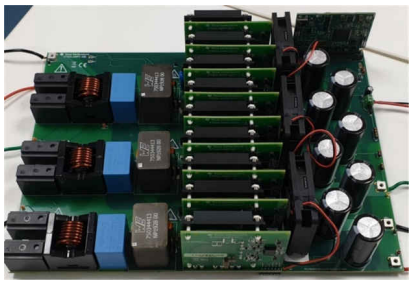
Ask our TI E2E™ support experts

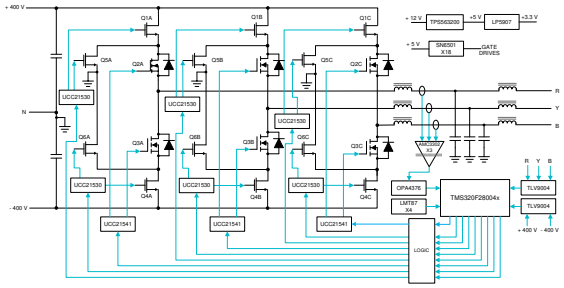
特長

- SiC / GaN スイッチを使用した 3 相インバータ / PFC の電力段
- 650V 定格のスイッチを 800V システムに使用可能 (3 レベルのため)
- C2000 の CLB を使用して実装された新しいオンボード保護機能
- 絶縁型デュアル・チャネル・ドライバによる高周波動作 (100kHz) のサポート
- シャントを使った電流検出 (温度範囲全体にわたる優れた精度と直線性)
- 最大 10A の電流 (AC 側) に対応するパワー・モジュール
- 高いスイッチング周波数 (100kHz) と高い効率 (98% 超、全負荷時) による高い電力密度
- 1ms 未満で方向を切り替えることができる双方向動作
- システムの信頼性の向上に役立つ小さな部品ストレス
- 最適化済みの制御方式を採用した結果、標準的な実装で 9 個の PWM を使用するのに対し、必要なのは 6 個の PWM のみ
- 低コスト - アームごとに (6 つに対して) 4 つの高周波スイッチ
- 追加のコストを掛けないでリアルタイムの安全動作を実現

アプリケーション

- 太陽光ストリング・インバータ
- 太陽光セントラル・インバータ
- エネルギー・ストレージ電力変換システム (PCS)





1 System Description

Modern commercial scale solar inverters are seeing innovation on multiple fronts, which lead to smaller, higher efficiency products in the market:

- The move to higher voltage solar arrays
- Reducing the size of onboard magnetics
- Inclusion of localized power storage requiring bidirectional power stages

By increasing the voltage to 1000-V or 1500-V DC from the array, the current can be reduced to maintain the same power levels. The reduction in current reduces conduction losses and hence results in higher efficiency. The reduction in di/dt also reduces the stress on electrical components. However, high DC bus voltages can limit the choice of power components that can be used as devices with higher voltage withstand capability is needed.

To compensate for the voltage stresses generated by high-voltage solar arrays, new topologies of solar inverters have been designed. Traditional half bridges block the full input voltage on each switching device. By adding additional power components, the overall stress on the device can be significantly reduced. This reference design shows how to implement a three-level ANPC converter that limits the voltage stress on all the power components to only half the DC bus voltage, allowing use of more abundant and faster power components. This design also demonstrates the use GaN devices in solar inverters which was not possible with other topologies due to their limitation of voltage withstand capability.

Additional power density is also being enabled by moving to higher switching speeds in power converters. As this design shows, a higher switching speed reduces the overall size requirement of the output filter stage—a primary contributor to the design size.

Though multilevel topologies enable the use of lower voltage switching devices, they come with certain limitations – the need to drive more switches and need to avoid overvoltage even during abnormal operation. This design tries to demonstrate how to address all 18 power devices in the power stage with the limited number of PWMs available from a common MCU and also how to implement hardware based interlocking protections needed to avoid device overvoltage under all operating conditions without the use of additional components.

Another requirement that is becoming more prevalent for inverter power stages is the need for bidirectional power transfer. This is important in storage ready inverters where there can be a need for the power from the grid to be stored in local power storage like a battery. The power conversion stage in an electronic energy storage system also has the same requirement. The ANPC power stage demonstrated in this design is inherently capable of bidirectional operation – only software is required for it to operate either as inverter or power factor controller (PFC). Currently the design is tested in inverter mode operation and the testing in PFC mode is in progress.

1.1 Key System Specifications

表 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Output power	6.6 kW	At 400-V AC output
Output voltage	Three-phase 400-V AC	
Output frequency	50 or 60 Hz	

表 1-1. Key System Specifications (continued)

PARAMETER	SPECIFICATIONS	DETAILS
Output current	10 A	
Nominal input voltage	800-V DC	
	600-V to 1000-V DC	
Inverter switching frequency	100 kHz	
Efficiency	98.5%	At 400-V AC output, 60% load
Power density	1.54 kW/L	

2 System Overview

2.1 Block Diagram

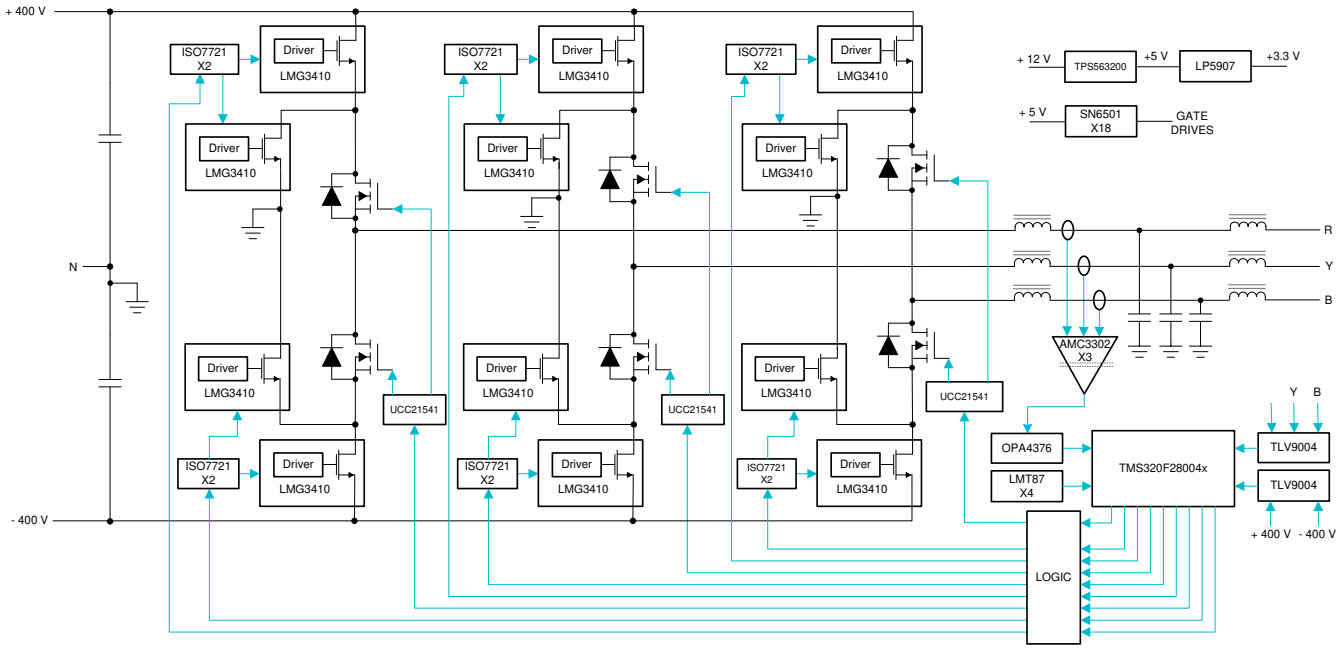


図 2-1. Block Diagram

This reference design is built in a modular construction to allow easy replacement of power switching devices to allow easy comparison between them. The following boards combine to form this three-phase inverter reference design:

- A mother board, comprising of the LCL filter, sensing electronics, bias power, switching relays and cooling fans.
- A TMDSCNCD280049C Control Card to support the DSP.
- Six power cards switching at 100kHz containing power switching devices, gate drivers and isolated bias power supplies. These can be SiC or GaN based.
- Three power cards switching at 100/120Hz containing power switching devices, gate drivers and isolated bias power supplies. These can be Si or SiC based.

Though the board can accept 12 V bias power from an external power supply, it has provision to add an auxiliary power supply that can run from the high voltage DC bus.

2.2 Design Considerations

2.2.1 Three-Phase ANPC Inverter Architecture Overview

The basic architecture of the ANPC topology is shown in 図 2-2.

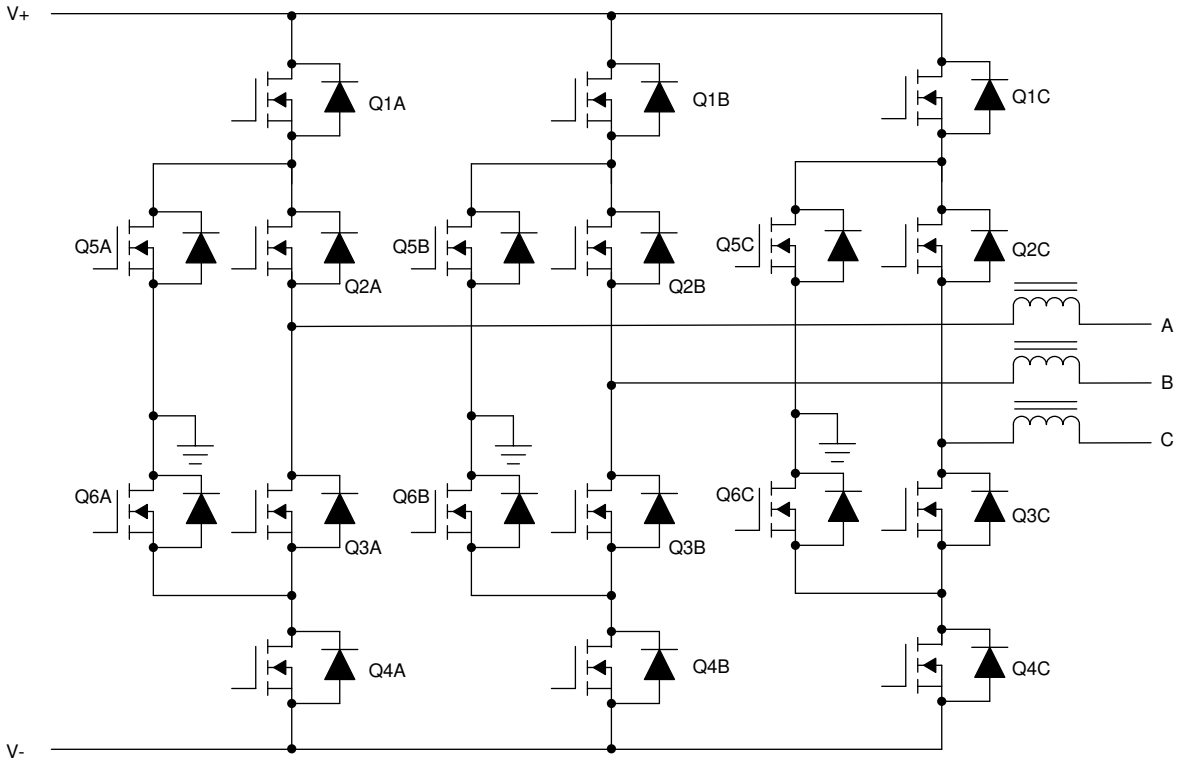


図 2-2. ANPC Three-Phase Inverter Architecture

To simplify the analysis, a single leg can be separated out as shown in 図 2-3.

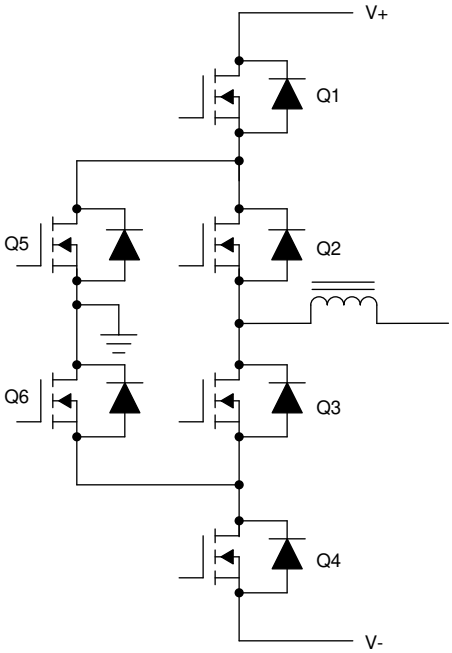


図 2-3. ANPC Single-Phase Inverter Leg

As can be seen, there are six switches in each phase. Though there can be various switching schemes to control this power stage, we selected a relatively simpler scheme to reduce complexity. The upper half of the circuit consisting of Q1, Q5 and Q2 is active during the positive half cycle and the lower half consisting of Q4, Q6 and Q3 is active during the negative half cycle. Q2 and Q3 are slow switches that connect the inductor to either the upper high frequency switching pair of Q1 & Q5 or Q4 & Q6 during positive and negative half cycles respectively. Each of the high frequency switching pairs is operated as a synchronous buck converter during their corresponding half cycles. The switching scheme is explained in detail in 図 2-4 and 図 2-5.

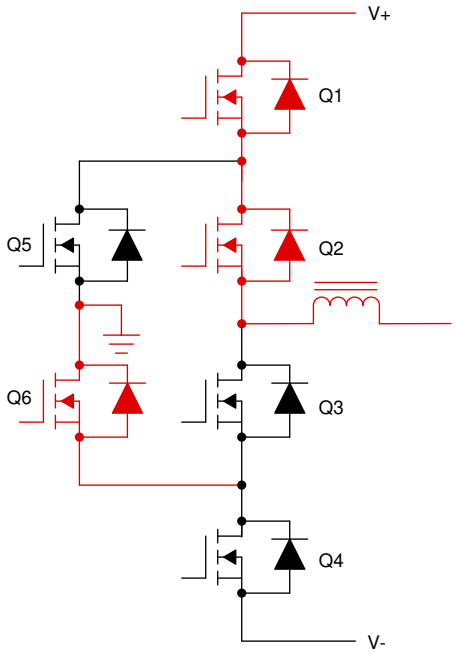


図 2-4. Inductor connected to V+

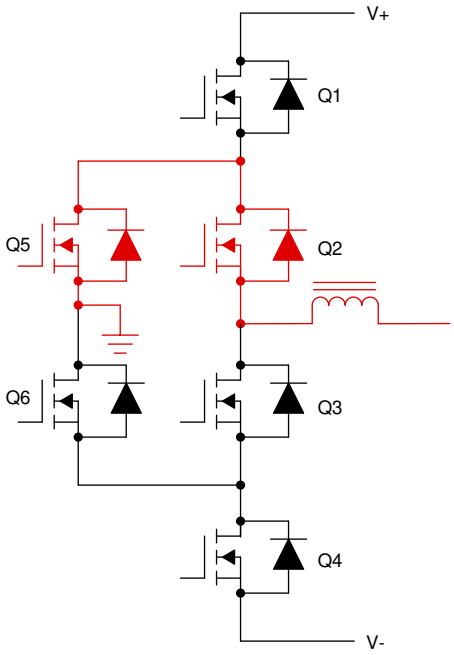


図 2-5. Inductor connected to N (+ve)

図 2-4 and 図 2-5 show the operation of the circuit during the positive half cycle of this phase. The components in red are the ones that are conducting and those in black are the ones that are off. As can be seen Q2 remains on for the entire half cycle. When Q1 is on, the circuit is in active mode, establishing current flow from V+ to the inductor as in 図 2-4. Since both Q1 and Q2 are on, the switching node of the inductor is connected to V+. Now, the switches Q3 and Q4 together have to withstand the full bus voltage. To avoid unequal distribution of the bus voltage among these devices (due to unequal device parasitics), Q6 also is kept on so that the central node gets connected to neutral, dividing the voltage equally between Q3 and Q4. When Q1 and Q6 are turned off together during the dead-time between the states shown in 図 2-4 and 図 2-5, the inductor current can only flow through the body diode of Q5 and Q2 (which stays on). During the freewheeling mode shown in 図 2-5, Q5 acts as a synchronous diode, connecting the switching node of the inductor to neutral. Since the switches Q3 and Q4 have only half the bus voltage across them, it is not necessary to keep Q6 on for voltage balancing.

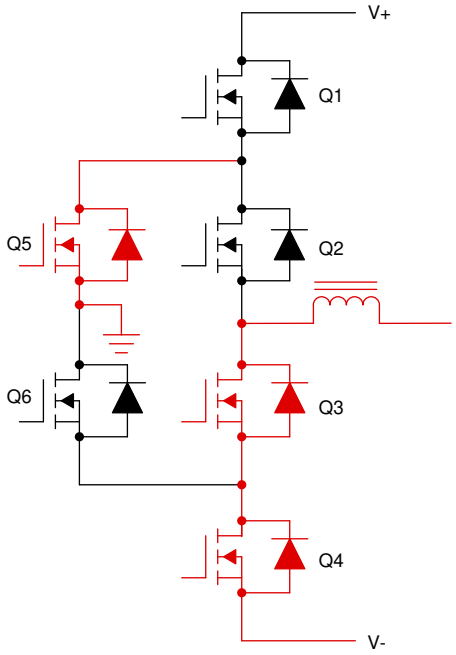


図 2-6. Inductor connected to V-

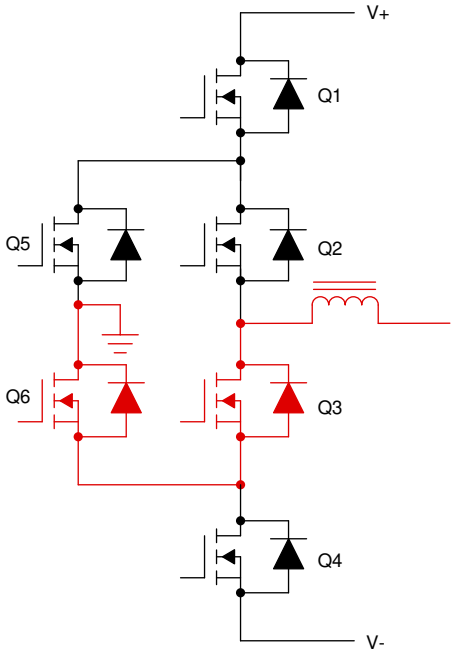


図 2-7. Inductor connected to N (-ve)

Similar to the operation during the positive half cycle, 図 2-6 and 図 2-7 illustrate the operation of the ANPC power stage during the negative half cycle. Q3 remains on for the entire duration of the negative half cycle.

図 2-6 shows the active mode operation in which the inductor gets connected to V- through Q4 and Q3. Similar to the operation during positive half cycle, Q5 also is kept on in this active mode operation to balance the voltage stress between Q1 and Q2. In freewheeling mode shown in 図 2-7, the inductor current is maintained through Q6 and Q3, connecting the inductor switch node to neutral.

2.2.2 LCL Filter Design

Any system of power transfer with the grid is required to meet certain output specifications for harmonic content. In many rectifiers, a high-order LCL filter typically provides sufficient harmonic attenuation, along with reducing the overall design size versus a simpler filter design. However, due to the higher order nature, take some care in its design to control resonance. 図 2-8 shows a typical LCL filter.

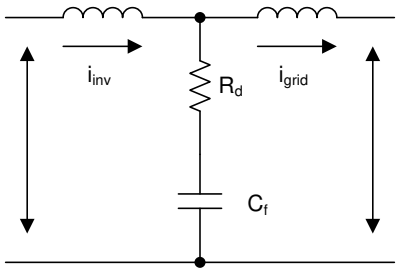


図 2-8. LCL Filter Architecture

One of the key benefits of using SiC or GaN switching devices (as this reference design does) is the ability to increase the switching frequency of the power stage significantly versus traditional Si-based switching devices. This increased switching frequency has a direct impact on the filter resonant design of the converter, which needs to be accounted for. To ensure that the filter is designed correctly around this switching frequency, the known mathematical model of this type of filter is used in this design.

The primary component is the switch side inductor, or L_{inv}, which can be derived using 式 1:

$$L_{inv} = \frac{V_{DC}}{8 \times f_{SW} \times I_{grid\_rated} \times \%ripple} \quad (1)$$

Using the system specifications, the primary inductor value can be calculated:

$$L_{inv} = \frac{1000\ V}{8 \times 100\ kHz \times 10\ A \times 30\%} = 417\ \mu H \quad (2)$$

An inductor from Wurth Elektronik (750344413) with rated current of 15A having zero bias inductance of 480mH is used. With the high current bias during the operation, the inductance can reduce by 25% as per the data sheet. This results in an effective inductance of 360mH at 15 A, which is sufficient to ensure ripple current below 40%.

The sizing of the primary filter capacitor is handled in a similar fashion using 式 3:

$$C_f = \frac{\%\chi \times Q_{rated}}{2 \times \pi \times F_{grid} \times V_{grid}^2} \quad (3)$$

Make some design assumptions to finalize the value of C_f , limiting the total reactive power absorbed by the capacitor to 3.5%. Scaling the total system power by the per phase power results in a primary capacitor value of:

$$C_f = \frac{3.5\% \times \frac{6.6\ kW}{3}}{2 \times \pi \times 50\ Hz \times \left(\frac{400\ V}{\sqrt{3}}\right)^2} = 4.59\ \mu F \quad (4)$$

A standard value capacitor of 4.7uF was selected.

For the remainder of the filter design, determine the values by defining the attenuation factor between the allowable ripple in grid inductor and the inverter inductor. This factor needs to be minimized while still maintaining a stable and cost effective total filter. By assuming an attenuation factor, an r value, which defines the ratio between the two inductors, is determined using 式 5:

$$I_{att} = \frac{1}{\left|1 + r \times \left[1 - L_{inv} \times C_b \times \left(2 \times \pi \times f_{SW}\right)^2 \times \chi\right]\right|} \times 100 \quad (5)$$

Where C_b is given by:

$$C_b = \frac{C_f}{\chi\%} = \frac{4.7\ \mu F}{3.5\%} = 134\ \mu F \quad (6)$$

To obtain an attenuation factor of 5%, and using the earlier derived values, the value of r can be evaluated by rewriting this 式 5 to be:

$$r = \left| \frac{\frac{1}{5\%} - 1}{1 - 360\ \mu H \times 134\ \mu F \times \left(2 \times \pi \times 100\ kHz\right)^2 \times 3.5\%} \right| = 2.85\% \quad (7)$$

The resultant value for L_{grid} is then:

$$L_{grid} = r \times L_{inv} = 2.85\% \times 360\ \mu H = 10.3\ \mu H \quad (8)$$

A higher standard value of 15µH was selected to ensure good attenuation.

The filter design can be validated by determining its resonant frequency (F_{res}). A good criteria for ensuring a stable F_{res} is that it is an order of magnitude above the line frequency and less than half the switching frequency. This criteria avoids issues in the upper and lower harmonic spectrums. The resonant frequency of the filter is given by 式 9:

$$F_{res} = \frac{1}{2 \times \pi \times \sqrt{\frac{L_{grid} \times L_{inv}}{L_{grid} + L_{inv}} \times C_f}} \quad (9)$$

Using the derived filter values, the resonant frequency is:

$$F_{res} = \frac{1}{2 \times \pi \times \sqrt{\frac{15\ \mu H \times 360\ \mu H}{15\ \mu H + 360\ \mu H} \times 4.7\ \mu F}} = 19.35\ kHz \quad (10)$$

This value for F_{res} meets the criteria listed earlier and validates the filter design.

The remaining value to determine is the passive damping that must be added to avoid oscillation. Generally, a damping resistor at the same relative order of magnitude as the C_f impedance at resonance is suitable. This impedance can be derived using 式 11:

$$R_d = \frac{1}{6 \times \pi \times F_{res} \times C_f} \quad (11)$$

$$R_d = \frac{1}{6 \times \pi \times 19.35\ kHz \times 4.7 \mu F} = 0.58\ \Omega \quad (12)$$

For the final implementation in hardware, use real values for all of these components based on product availability and must be chosen to be appropriately close (±10% typically). When final values are determined, recalculate the resonant frequency to ensure the filter is still stable.

2.2.3 Power switching devices Selection

As shown in the architecture overview, the main switching device needs to support only half the full switching voltage. To support the 1000-V DC link voltage of this design, we can use 600-V rated devices. The switches Q1, Q5, Q4 & Q6 are high frequency switching and hence will need to be either GaN or SiC devices. However, the switches Q2 & Q3 are only switching at 100/120Hz and hence can use Si MOSFETs.

Conduction loss is mainly determined by the R_{DS_on} of the SiC/GaN MOSFET and the R_{DS_on} of the Si MOSFET. At any instance, there are two devices conducting at the same time (one each of the SiC/GaN device and the Si device). So the R_{DS_on} of these should be selected based on the conduction loss that can be allowed on them.

Switching loss is a function of the switching frequency and switching energy of each switching element; the switching energy being related to the device current and voltage at the switching transient. Using the switching energy curve in the data sheet, the total switching loss can be estimated. Note that in inverter configuration, only Q1 or Q4 experience switching loss, as Q5 & Q6 work as synchronous switches only and hence experience zero voltage switching. However, since Q5 and Q6 body diodes conduct during dead-time, they can have forward drop loss and reverse recovery loss. However, TI's GaN devices do not have reverse recovery loss at all and

SiC devices have only negligible reverse recovery. Q2 & Q3 switch only at a very low frequency and hence their switching loss can be neglected.

The conduction loss and switching loss can be estimated for all the devices and efficiency can be estimated as explained. With the thermal impedance information of the thermal system design, the proper device rating can be selected. 650-V/50-mΩ GaN/SiC MOSFET and 650-V/40-mΩ Si MOSFET are good tradeoffs among thermal, efficiency and cost.

2.2.4 GaN Power Stage

Unlike the SiC and Si power boards which are driven by isolated gate drivers as explained in セクション 2.2.8, the TI GaN device LMG3410R050 has inbuilt gate drive. So the power stage needs signal isolation to interface it with the MCU. The GaN power stage is shown in 図 2-9. The ISO7721 isolator used to isolate the PWM input has another channel in reverse direction that can transmit the fault signal back to the MCU side. As this is a negative logic one, an AND gate is used to combine these signals to give a negative logic fault signal back to the MCU if either of these GaN devices generate a fault.

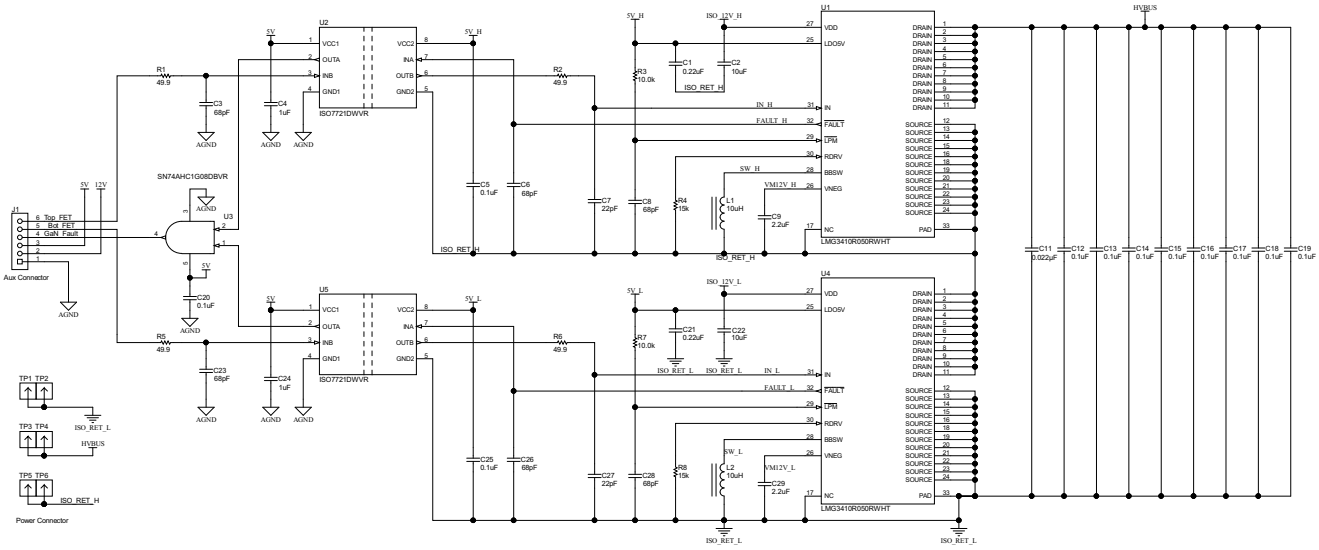


図 2-9. GaN Power Stage

2.2.5 Voltage Sensing

Voltage sensing happens at three points in the inverter signal path to aid in control: before and after the primary output relay and at the positive and negative bus voltages. By enabling measurement on both sides of the relay, the control system can lock into the grid voltage and frequency before connecting, thus preventing any mismatch issues. Similarly, sensing of the positive and negative bus voltages help in fine adjusting the duty cycle separately during the positive and negative half cycle to prevent any bus voltage mismatch.

All three sensing topologies are similar. First, PGND is used as a virtual neutral using a resistor network. The high voltage signal is attenuated using a series of large value resistances. An offset of 1.65 V is added to the attenuated neutral point to center the voltage signal in the middle of the input range of the TLV9004, and the attenuated value from the phase voltage is measured using the ADC within the C2000™ MCU. 図 2-10 shows this sensing arrangement.

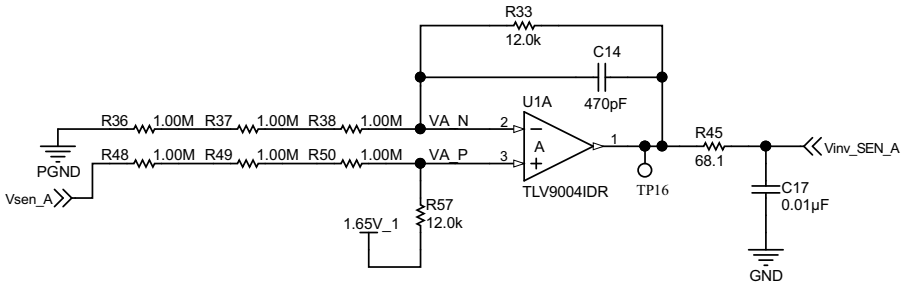


図 2-10. High-Voltage Sensing Signal Path

2.2.6 Current Sensing

Critical to getting a closed loop control system is accurate current measurement of the inverter. In this design, current measurement is done to sense the current through the inductor. Because the output is high voltage and the controller needs to remain isolated, the AMC3302 reinforced isolated current sensor is used to measure the resistor voltage drop. To keep system losses low, the AMC3302 has a ±50-mV input range. When compared to other devices with a typical input range of ±250 mV, the total power loss across the shunt is significantly reduced.

Sizing the shunt resistor for this design is a trade-off between sensing accuracy and power dissipation. A 2 mΩ shunt provides a ±30-mV output signal at the inverters approximate ±15-A output but also only generates 0.2 W of heat at full load. When choosing an actual device, select a high accuracy one to eliminate the need to calibrate each sensor path.

The voltage across the shunt resistor is fed into the AMC3302 isolated current sensor with integrated isolated bias power supply, which generates a differential output. This differential output is converted to a single ended output with a 1.65 V offset using an OPA4376 amplifier for measurement using the ADC present on the C2000™ MCU. The current sensing circuit is given in 図 2-11.

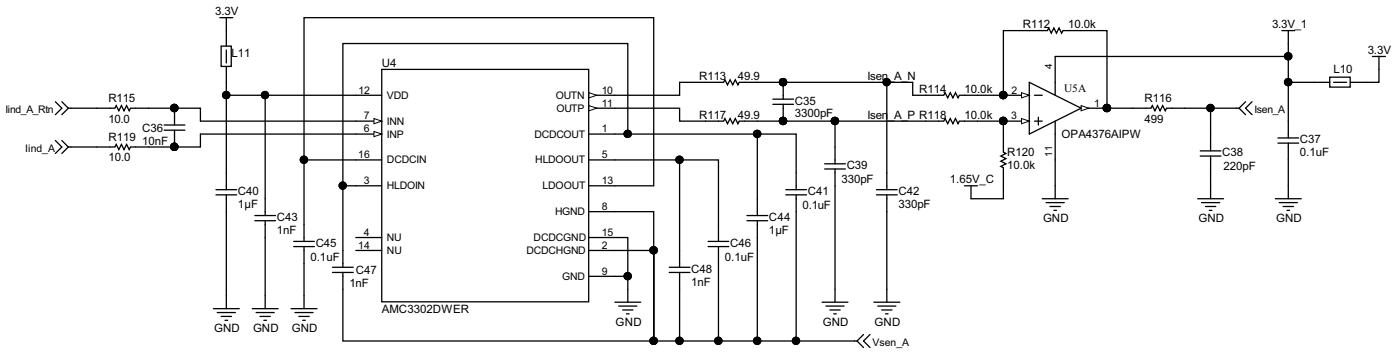


図 2-11. Isolated Current Sensing With AMC3302

2.2.7 System Power Supplies

This reference design uses multiple voltage domains across the system:

- A primary bias power input to power the entire design (regulated 12 V). This is used to directly power relays and fans used on the board. There is a connector provision on the main board to generate this 12 V supply directly from the high voltage DC bus.
- A TPS563200 synchronous buck converter generates 5 V to power the control card and power cards from the 1 V main power. Each of the power cards generate its own isolated power supply for gate driving from this 5 V power supply.
- The 3.3 V supply for analog sensing and logic is generated by an LDO LP5907 from the 5 V.

図 2-12 shows the power tree for all of these domains.

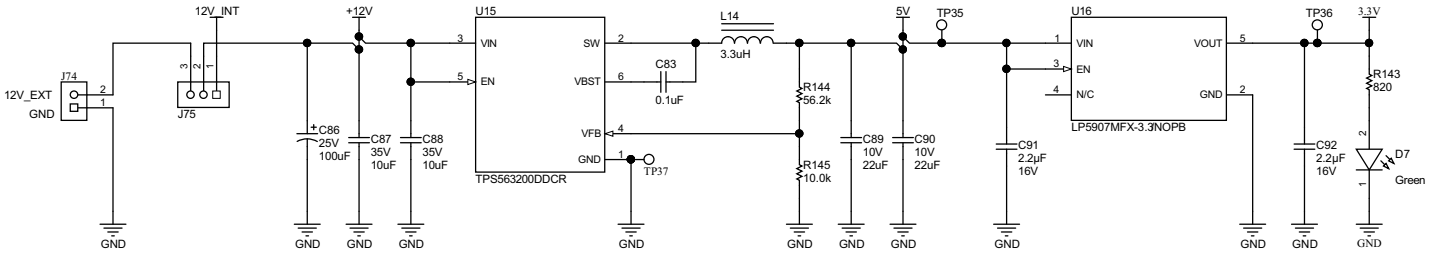


図 2-12. Power Tree

2.2.7.1 Isolated Bias Supplies

To generate the isolated bias supplies for each of the power cards, the SN6501 transformer driver is used to drive transformers suited for the power rails required to drive the specific power switching devices used in each type of board As each of the boards have two switching devices, there are two isolated bias power supplies per board.

As the SCT3060AL SiC device from Rohm needs a +15 V and -4 V drive, the SN6501 transformer driver along with Würth Elektronik 750343725 transformer in a push-pull configuration is used to generate a 19 V supply. A TL431 based level shifting circuit converts this to +15 V, -4 V supply. The circuit is shown in 図 2-13.

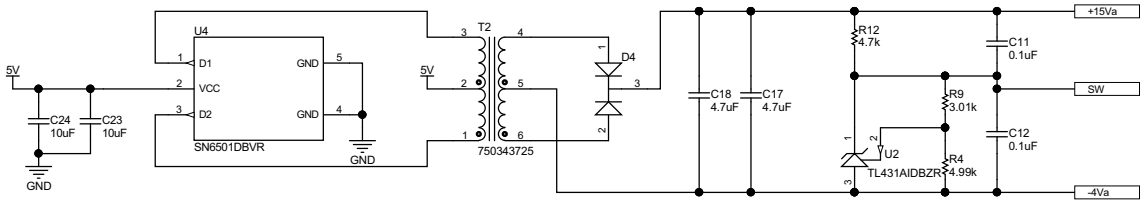


図 2-13. SN6501 Bias Voltage Supply for SiC power board

For the TI GaN device LMG3410R050, a 12 V output is needed. This is generated using the SN6501 transformer driver along with Würth Elektronik 750313638 transformer in a voltage doubler configuration as shown in 図 2-14.

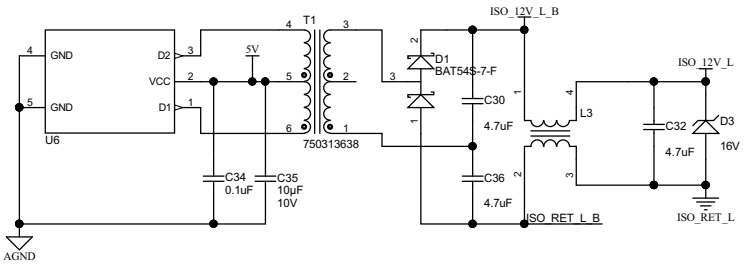


図 2-14. SN6501 Bias Voltage Supply for GaN power board

For the slow switching Si power board, a +12 V, -5 V drive is used to drive the FCH040N65S3 Si MOSFET. The SN6501 transformer driver along with Würth Elektronik 750342879 transformer in a push-pull configuration is used to generate a 17 V supply. A TL431 based level shifting circuit converts this to +12 V, -5 V supply. The circuit is shown in 図 2-15.

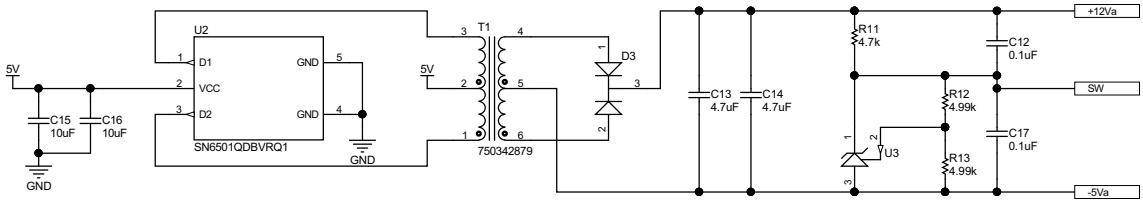


図 2-15. SN6501 Bias Voltage Supply for Si power board

2.2.8 Gate Drivers

図 2-16 shows the schematic of the isolated SiC MOSFET gate driver. As the UCC21530 gate driver used has two isolated gate drive outputs, it can drive both the devices in the half-bridge power stage of the power board. The drive current is controlled separately for turn-on and turn-off with diode controlled separate drive paths. A ferrite bead is used in the gate drive path to suppress ringing.

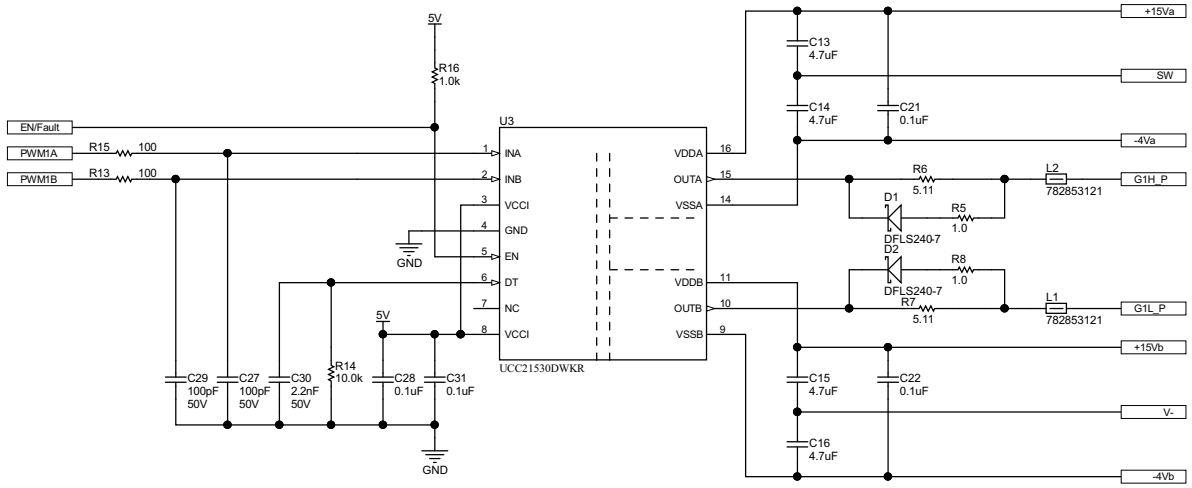


図 2-16. UCC21530 Gate Drive Circuit

図 2-17 shows the schematic of the isolated Si MOSFET gate driver. As the UCC21541 gate driver used has two isolated gate drive outputs, it can drive both the devices in the half-bridge power stage of the power board. The drive current is controlled separately for turn-on and turn-off with diode controlled separate drive paths. A ferrite bead is used in the gate drive path to suppress ringing.

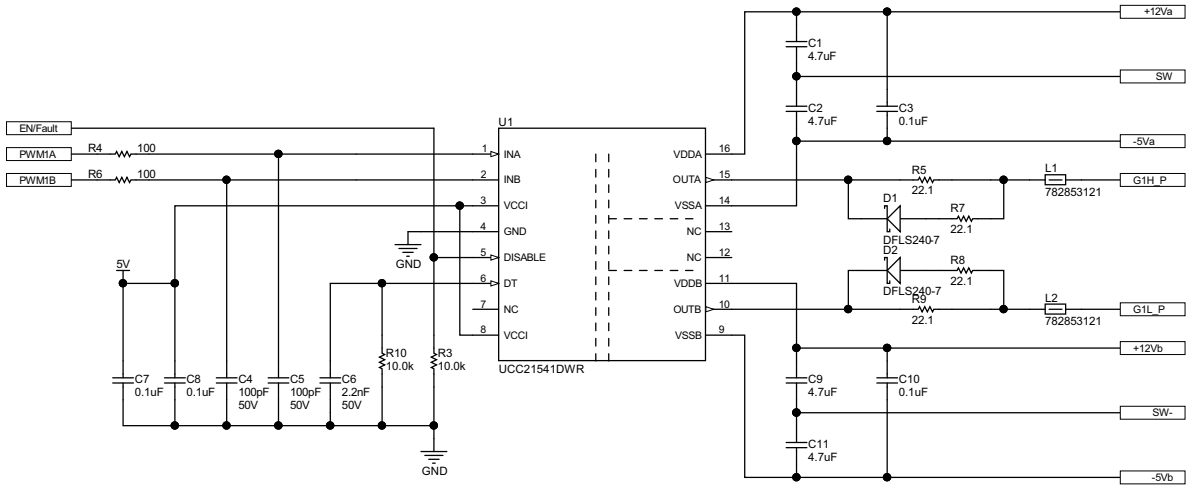


図 2-17. UCC21541 Gate Drive Circuit

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware and Software Requirements

3.1.1 Hardware

The DUT in this design is set up and operated in several pieces:

- One TIDA-010210 mother board
- Six TIDA-010210 High frequency power cards, with either GaN or SiC switching devices
- Three TIDA-010210 low frequency power cards with Si MOSFETs

- TMDSCNCD280049C Control Card:

  S2 Switch : Should be changed from DOWN to UP position
  S3 Switch : Should be changed from UP to DOWN position
- Mini USB cable
- Laptop or other computer

The test equipment required to power and evaluate the design is as follows:

- 15-V/2-A bench style supply for primary board power
- >1000-V/10-A power supply for DC link input
- >6.6-kW resistive load

Four-channel, power quality analyzer

3.1.2 Software

- Code Composer Studio™ 9.3 or later versions with TI C2000 powerSUITE

3.2 Testing and Results

3.2.1 Test Setup

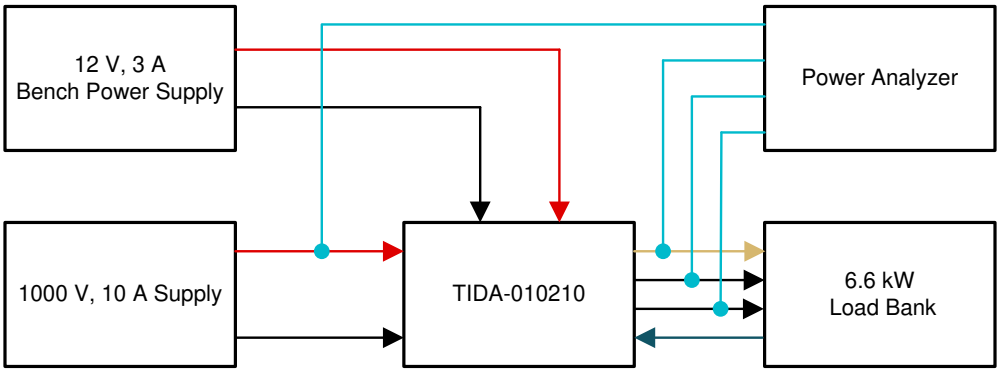


図 3-1. Test Setup for Efficiency

To test the efficiency of this reference design, use the following equipment:

- One Magna-Power 1000-V, 10-A power supply to provide CV/CC adjustable input to the DUT.
- A 6.6-kW KWE load bank is used as a configurable load to test the design at various set points.
- An AC power analyzer is connected to the DUT input and output to perform efficiency measurements.
- An external bench power supply is used to provide a 12-V input to power the DUT.

The system is configured to operate in an open loop control mode, generating a static 400-V, 50-Hz output. The power demand is then modulated by the Simplex load bank to test the system at multiple load points.

3.2.2 Test Results

表 3-1 and 表 3-2 lists the system efficiency results with SiC device SCT3060AL and GaN device LMG3410R050 respectively. The results demonstrate the inverter power stage peak efficiency of 98.5%.

表 3-1. System Efficiency Results with SiC device SCT3060AL

INPUT VOLTAGE	INPUT CURRENT	INPUT POWER	OUTPUT POWER	EFFICIENCY
798.2	0.0235	18.7577	0	0
798.2	0.281	224.2942	203.2	90.5953
798.2	0.793	632.9726	599.6	94.72764
798	2.03	1619.94	1574	97.16409
797.8	3.254	2596.0412	2539.8	97.83358
797.7	4.475	3569.7075	3499.5	98.03324

表 3-1. System Efficiency Results with SiC device SCT3060AL (continued)

INPUT VOLTAGE	INPUT CURRENT	INPUT POWER	OUTPUT POWER	EFFICIENCY
797.7	4.955	3952.6035	3875.6	98.05183
799.1	5.812	4644.3692	4554.9	98.0736
799	7.394	5907.806	5794.8	98.08717
798.9	8.123	6489.4647	6365.4	98.08821

表 3-2. System Efficiency Results with GaN device LMG3410R050

INPUT VOLTAGE	INPUT CURRENT	INPUT POWER	OUTPUT POWER	EFFICIENCY
799.3	0.0164	13.10852	0	0
799.3	0.274	219.0082	205.14	93.66773
799.3	0.784	626.6512	606.9	96.84813
799.1	2.028	1620.5748	1591.5	98.2059
799	3.259	2603.941	2563.9	98.46229
798.8	4.481	3579.4228	3526	98.5075
798.7	4.961	3962.3507	3903	98.50213
799.1	5.885	4702.7035	4630.8	98.47102
799	7.197	5750.403	5660.5	98.43658
799	7.46	5960.54	5866.7	98.42565

The efficiency graph shown in 図 3-2 shows a clear efficiency advantage with the GaN device. TI GaN gives about 0.5% efficiency improvement at high loads; 2 – 3% at light loads.

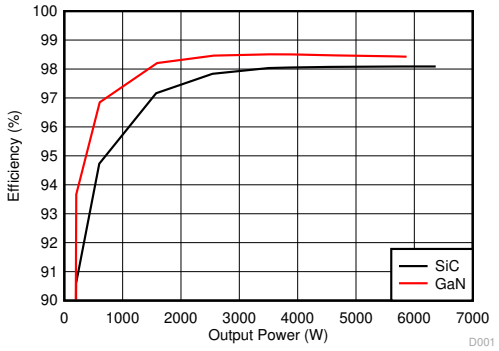


図 3-2. Inverter Efficiency

The open loop test output waveforms in 図 3-3show clean sinusoidal waveforms with the new PWM scheme. There is very little distortion even at zero crossing with CLB based protection active.

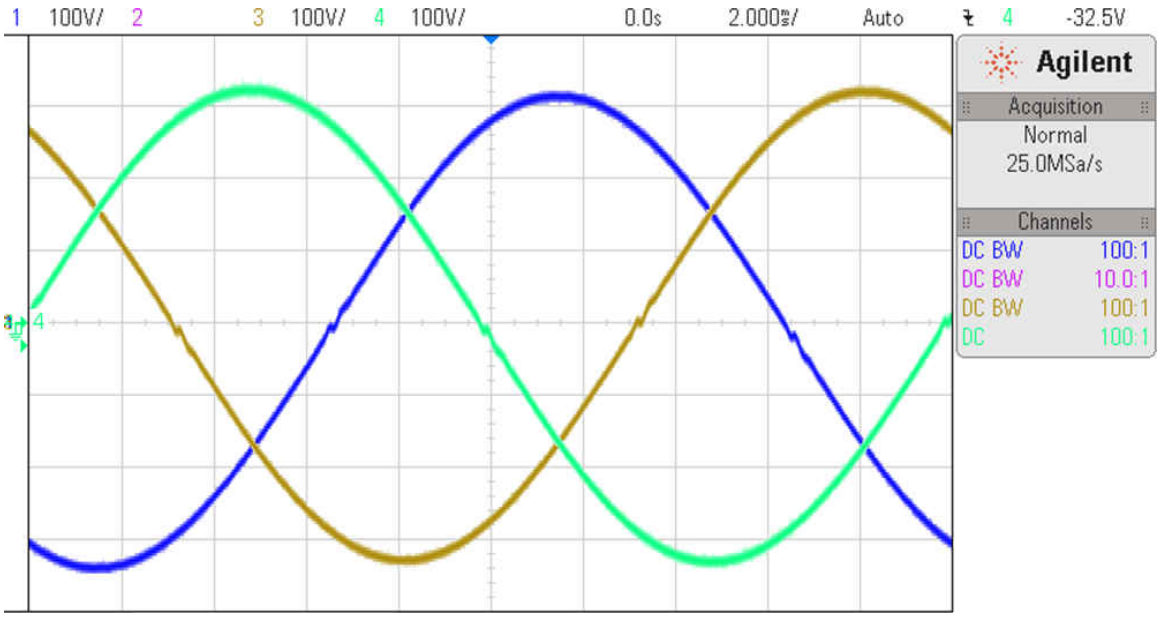


図 3-3. Open Loop Output Waveforms

The current loop stability of the circuit is demonstrated by the smooth transition in the current transient response. 図 3-4 shows the response when current is changed from 1 A to 6 A and 図 3-5 shows the response when current is changed from 6 A to 1 A.

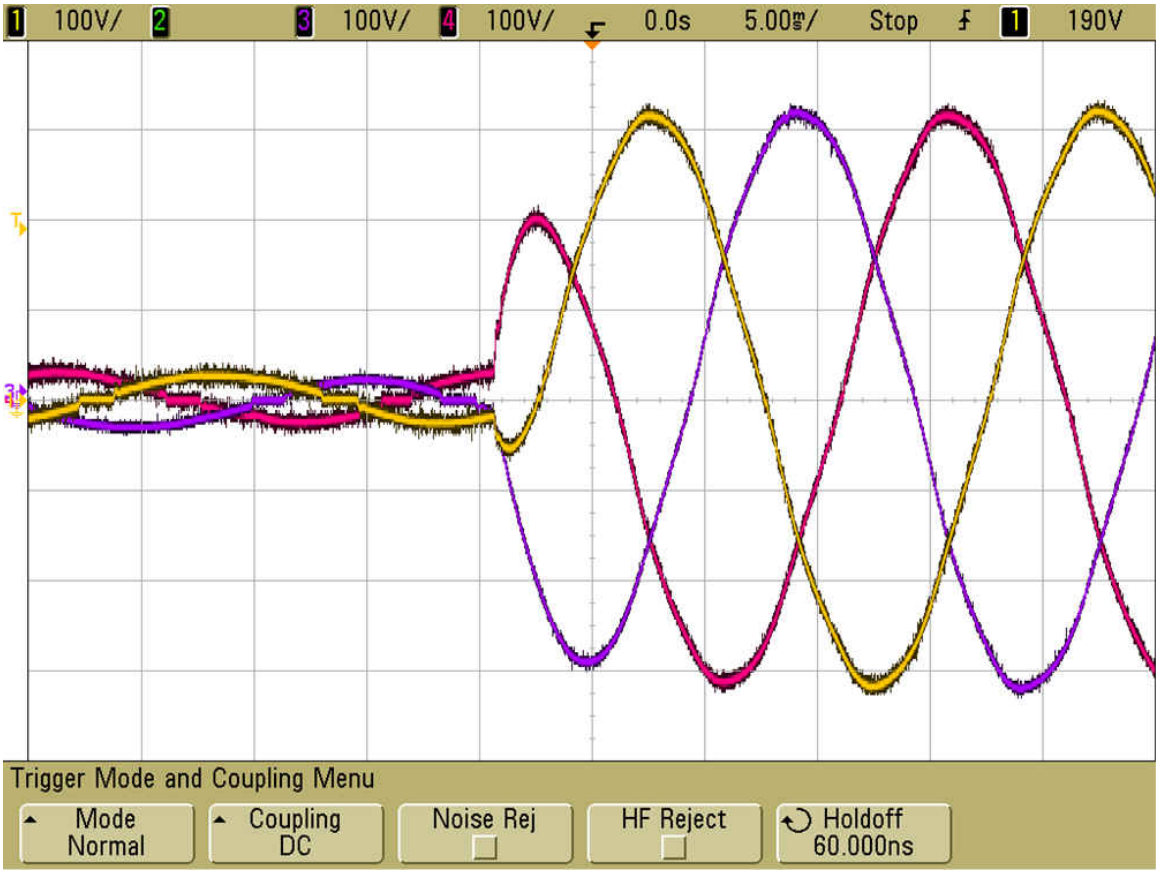


図 3-4. Positive going transient response

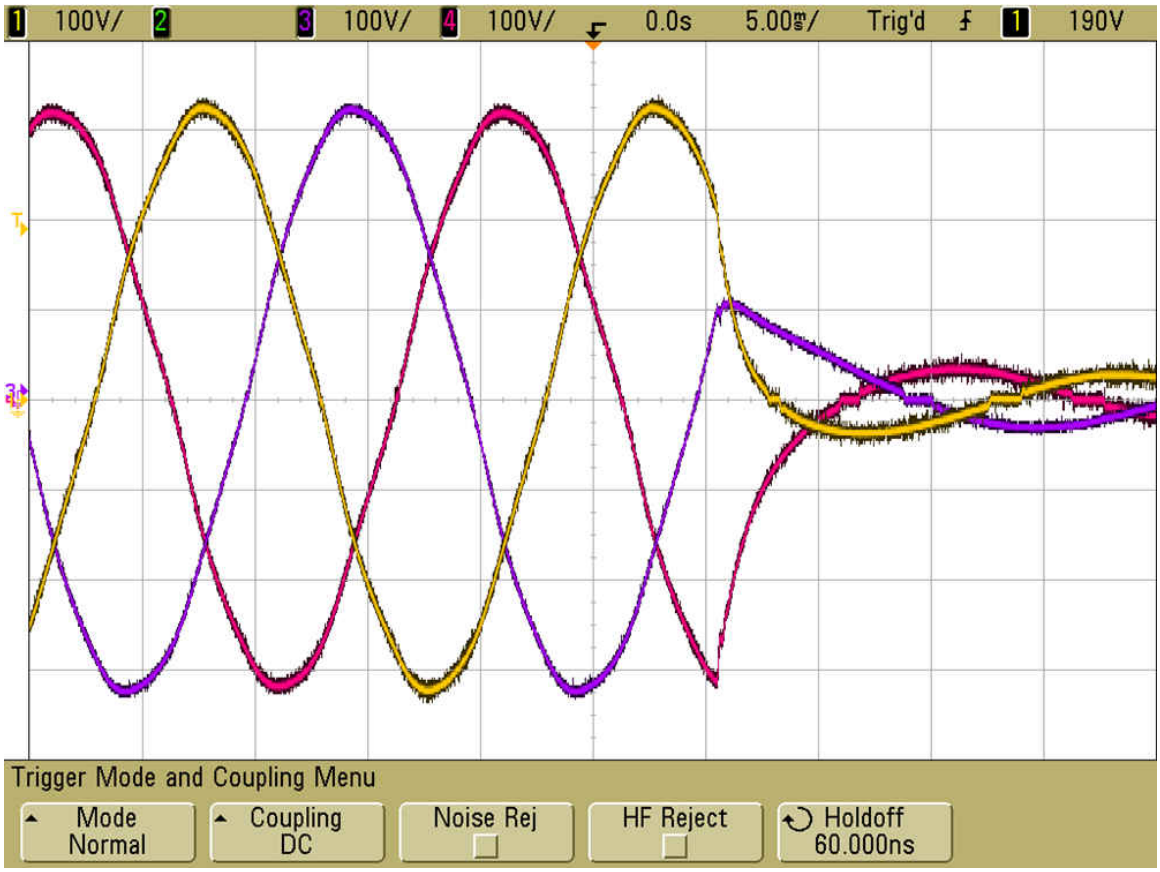


図 3-5. Negative going transient response

表 3-3. System Dimensions

AXIS	DIMENSION
X	300 mm
Y	220 mm
Z	65 mm
Volume	4.29 liters

The final design dimensions are outlined in 表 3-3and show a total volume of 4.3 L. With a power rating of 6.6 kW, this results in a power density of 1.54 kW/L.

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010210.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010210.

4.1.3 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010210.

4.1.4 Gerber Files

To download the Gerber files, see the design files at TIDA-010210.

4.1.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010210.

4.2 Tools and Software

Tools

Concise Description	TMDSCNCD280049C is an HSEC180 controlCARD based evaluation and development tool for the C2000™ *F28004x series* of microcontroller products. controlCARDs are ideal to use for initial evaluation and system prototyping. controlCARDs are complete board-level modules that utilize one of two standard form factors (100-pin DIMM or 180-pin HSEC) to provide a low-profile single-board controller solution. For first evaluation controlCARDs are typically purchased bundled with the *TMDSHSECDOCK* baseboard or bundled in an application kit.

Software

Concise Description	To download the software, see the software files at TIDA-010210.

4.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

4.4 Trademarks

TI E2E™ and C2000™, and are trademarks of Texas Instruments.
Altium Designer® is a registered trademark of Altium LLC or its affiliated companies.
すべての商標は、それぞれの所有者に帰属します。

5 About the Authors

SALIL CHELLAPPAN is a Systems Engineer at Texas Instruments working on leveraging TI's product portfolio to solve system engineering problems related to Renewable Energy markets. After graduating from Kerala University in 1990, Salil started his career at Bharat Electronics. Subsequently, he worked for companies for example, Lucent Technologies, Power Integrations, and GE before joining Texas Instruments; where he has worked in various roles as Lead Engineer, Systems Manager, and Systems Engineer for the past 13 years.

HIMANSHU CHAUDHARY is a systems application engineer at Texas Instruments with the C2000 Microcontrollers Industrial applications team. Since his graduation from Indian Institute of Technology (IIT) Kharagpur in 2018, Himanshu has been with the C2000 software group.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売約款 (https://www.tij.co.jp/ja-jp/legal/terms-of-sale.html)、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

日本語版 日本テキサス・インスツルメンツ合同会社