参考資料

Design Guide: TIDA-010230

*マルチチャネル **RF** トランシーバ、低ノイズ・クロックのレーダーと **EW** アプリケーション向けリファレンス・デザイン*

TEXAS INSTRUMENTS

概要

最新のレーダーおよび電子戦システムでは、アクティブ電子スキャン・アレイ（AESA）アンテナ・システムは、高速マルチチャネル RF トランシーバとともに多く使用されます。このようなシステムには、チャネル間スキューを正確に調整して、信号対雑音比 (SNR)、スプリアス・フリー・ダイナミック・レンジ (SFDR)、IMD3、有効ビット数 (ENOB) などのシステム性能を最適化できる、超低ノイズなクロック・ソリューションが必要です。このリファレンス・デザインは、LMX2820 および LMK04832 ベースの低ノイズ JESD204B 準拠クロックを提供し、最大 X バンド動作で複数の AFE7950 デバイスを 10ps 未満で同期させます。この結果、9GSPS、3GSPS の DAC または ADC クロックでシステム性能を向上できます。すべての主要な設計理論が記載され、部品選択プロセスや設計の最適化が説明されます。また、回路図、基板レイアウト、ハードウェア・テスト、結果も公開しています。

リソース

TIDA-010230	デザイン・フォルダ
AFE7950EVM、TSW14J56EVM	評価基板フォルダ
AFE7950、LMX2820	プロダクト・フォルダ
LMX04832、LMK1C1104	プロダクト・フォルダ

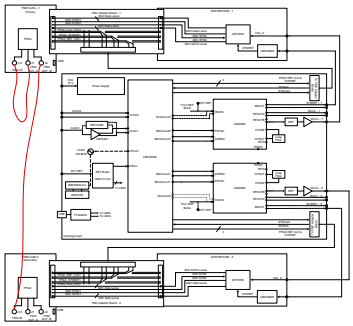
テキサス・インスツルメンツの TI E2E™ サポート・エキスパートにお問い合わせください。

特長

- JESD204B 準拠のマルチチャネル・クロック・ソリューション
- RF サンプリング AFE 向けの低位相ノイズ・クロッキング
- 8T8R RF サンプリング・アナログ・フロント・エンド
- 構成可能な位相同期により、複数チャネル・システムで低スキューを実現
- テキサス・インスツルメンツの高速コンバータ・カードとキャプチャ・カード (AFE7950EVM、TSW14J56EVM) をサポート
- 低ノイズと低リップルの DC / DC (TPS62913) は、小型サイズ、低消費電力、良好な放熱特性を、LDO なしでサンプル性能を達成

アプリケーション

- フェーズド・アレイ・レーダー
- 電子戦
- 追尾フロント・エンド



1 System Overview

1.1 Key System Level Specifications

The objective of this reference design is to demonstrate the high-speed clocking solution for multichannel RF sampling transceiver signal chains. This design focuses on measuring the synchronization performance of the two AFE7950EVM devices along with their SNR, SFDR, and IMD3 performance. The data generation and data capture are done by the TSW14J56EVM, which is interfaced with AFE7950EVM using an FMC adapter card. 表 1-1 lists the key system level specifications for the multichannel signal chains from the clocking solution perspective.

表 1-1. Key Specifications

Parameter	Specification	Condition	Unit
SFDR		AFE79xx sampling freq - 8847.36 M with 18 × interpolation, Spur free dynamic range 0-f_{DAC}/2, –0.5 dBFS;	
850	50.8		dBc
1800	51.9		dBc
2600	42		dBc
3500	44		dBc
4900	46.1		dBc
8100	46.1		dBc
SFDR		AFE79xx sampling freq - 8847.36 M with 18x interpolation, Spur free dynamic range within 500 MHz f_{OUT} ±250 MHz, –0.5 dBFS;	
850	68.5		dBc
1800	79.4		dBc
2600	77		dBc
3500	75		dBc
4900	76		dBc
8100	75		dBc
IMD3		AFE79xx sampling freq - 8847.36M with 18x interpolation, 2 tones at ±10 MHz –13 dBFS each tone	
850 MHz ±10 MHz	–66		dBc
1800 MHz ±10 MHz	–63		dBc
2600 MHz ±10 MHz	–62		dBc
3500 MHz ±10 MHz	–61		dBc
4900 MHz ±10 MHz	–57		dBc
Channel-to-Channel Skew		AFE79xx sampling freq - 8847.36M with 18x interpolation, **Using TSW14J56 EVMs in primary & secondary mode**	ps
850	5		ps
1800	5		ps
2600	5		ps
SNR		AFE79xx sampling freq - 2949.12M with Decimation by 6, specs from SNR plots in the data sheet; Signal to noise ratio, –3 dBFs input signal;	
840	63.2		dBFs
1750	60.9		dBFs
2610	62.5		dBFs
3700	62.2		dBFs
4910	60		dBFs
Channel-to-Channel Skew			
SFDR		AFE79xx sampling freq - 2949.12M with Decimation by 6, specs from data sheet; SFDR, –3 dBFs input signal;	
840	88.2		dBFs
1750	80.6		dBFs
2610	88		dBFs
3700	84		dBFs
4910	78.9		dBFs

表 1-1. Key Specifications (continued)

Parameter	Specification	Condition	Unit
Channel-to-Channel Skew		AFE79xx sampling freq - 2949.12 M with Decimation by 12, Signal to noise ratio, –3 dBFs input signal; **Using TSW14J56 EVMs in primary and secondary mode**	
840	5		ps
1750	5		ps
2610	5		ps
3700	5		ps
4910	5		ps

1.2 System Description

Multichannel high-speed end equipment such as RADAR and electronic warfare systems have a critical clocking requirement to achieve better performance (high SNR, SFDR, IMD3, and so forth) of analog front end and low analog channel-to-channel skew.

Phased array radar contains high channel count transceiver systems, which need high dynamic range, wide transmitter and receiver bandwidth, low latency, and good synchronization between the transceiver channels. The signal chain solution based on the AFE7950 RF sampling transceiver, LMX2820, and LMK04832 devices are able to achieve optimum performance for phased array radar applications.

Electronic warfare equipment used as electronic protection, security, and attack also require a multichannel transceiver system with wide dynamic range and higher instantaneous bandwidth for higher range and speed. The AFE7950 device is a good fit for the multichannel transceiver requirements of the EW application, and this design shows the synchronization of multiple devices.

In this solution, two LMX2820 devices receive in-phase OSCin reference input signals from an external source or onboard LMK61E2 through the LMK1C1104 reference buffer and generate the two in-phase device clocks at 8847.36 MHz and SYSREFs at 1.92 MHz for the AFE7950EVM devices. LMK04832 is responsible to generate the two pair of in-phase FPGA reference clock and SYSREF for TSW14J56EVM capture cards. The LMK04832 device also provides the SYNC signal to two LMX2820 devices for synchronization to each other.

To meet the SYSREF setup and hold time for both AFE7950 devices, very low skew and phase-adjustable SYSREFs and device clocks are provided through the LMX2820 devices, which are responsible for low channel-to-channel skew between two AFEs.

This reference design demonstrates the multichannel low-noise JESD204B-compliant clock generation for two AFE7950 devices to synchronize them and make an 8T8R (8-transmit and 8-receive) system that is a good fit for phased-array RADAR, and electronic warfare applications.

1.3 Block Diagram

図 1-1 shows the block diagram of the proposed multichannel phase-synchronized clock solution interface with multiple RF sampling transceivers. The AFE7950EVM interfaces with the TSW14J56 EVM data capture board through the FMC adapter card. A device clock and SYSREF to the AFE7950EVMs are provided by the LMX2820 using the length-matched cables and FPGA reference clocks and SYSREF provided through the LMK04832.

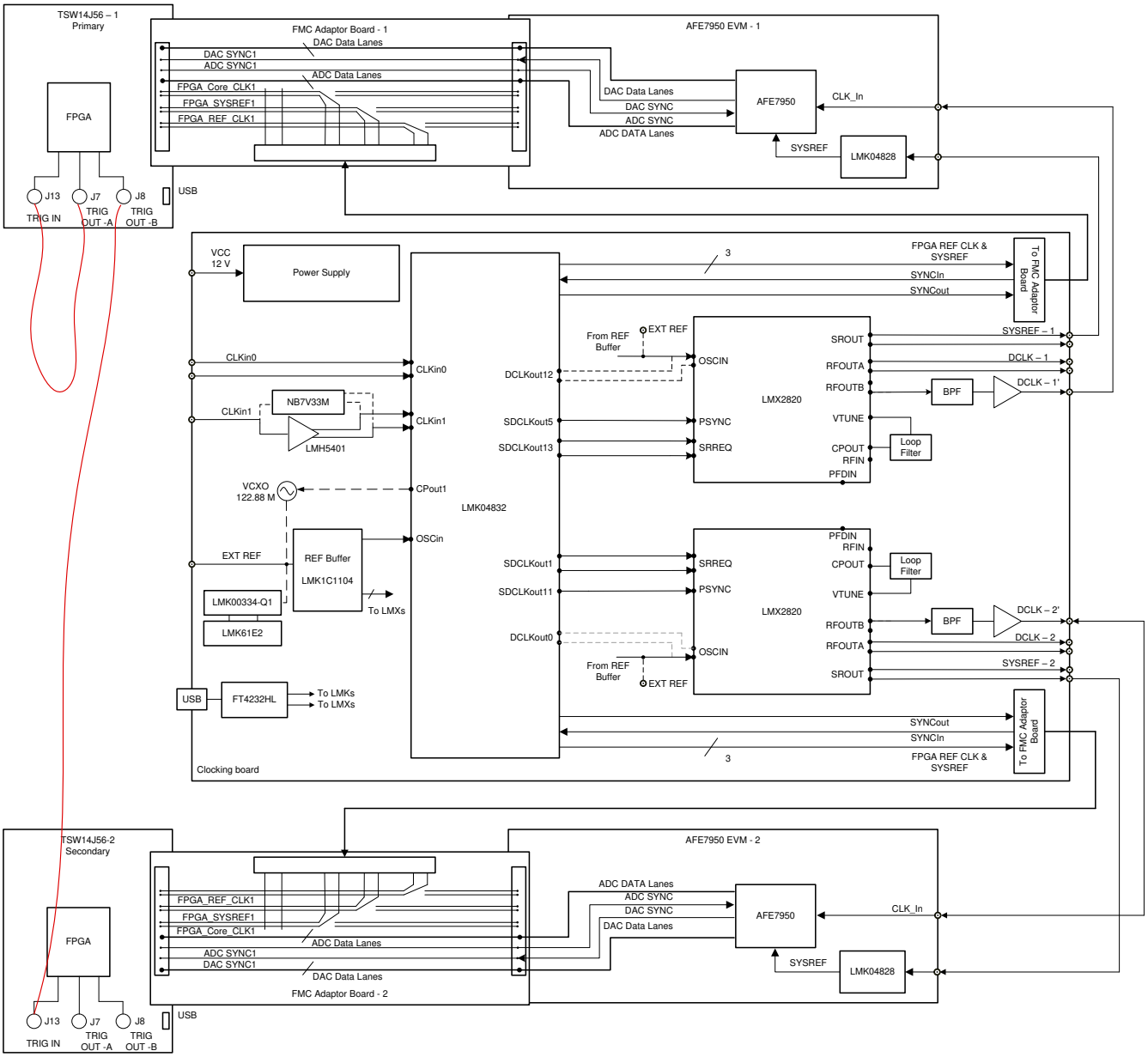


図 1-1. Block Diagram of Interface Between Clocking Board, AFE7950 EVM, FMC Adapter Board, and TSW14J56 Board

1.4 Design Considerations

Radar and EW systems typically operate in X, C, S, and L frequency bands. Radar and EW are typically based on a multiple wideband frequency conversion super-heterodyne architecture followed by a data converter. The multiple wideband frequency conversion stages use large, complex switched microwave filter banks. The number of wideband frequency conversion stages and the filter banks in the super-heterodyne architecture could be reduced in size and complexity with a wideband high sample rate data converter.

The AFE7950 device allows direct sampling from lower frequency band to X-band and could eliminate multiple components compared to conventional front-end architectures.

1.4.1 Frequency Band and Applications

S-band radars operate on a wavelength of 8–15 cm and a frequency of 2–4 GHz which is less attenuated in propagation compared to other higher frequency bands. Lesser attenuation makes them useful for near- and far-range radars. The drawback to this band of radar is that it requires a large antenna and antenna array will be challenging.

C- and X-band radars operate at frequencies of 4–12 GHz which is more easily attenuated in propagation. Lesser attenuation makes them useful for near-range radars. The antenna size for C and X bands are small that helps to realize antenna arrays. The smaller dimensions also allow applications like turbulence and weather radar in the aerospace segment. Higher frequency bands like C and X allow higher bandwidth radar signals resulting in finer range resolution.

1.4.1.1 RF Transceiver Synchronization Challenges

In a JESD204B system environment, data transfer from the JESD204B RX block to the TX block happens in multi-frames. These multi-frames are aligned to the edges of the local multi-frame clock (LMFC), which is internal to the JESD204B RX and TX block. The concept of the LMFC and the associated alignment requirements are critical in applications that require deterministic latency and multiple device synchronization. To achieve deterministic latency, multiple device synchronization, or both is to ensure that the LMFC of each JESD204B device in the JESD204B system environment are aligned. The LMFC of each JESD204B device is aligned through the SYSREF signal, which is globally generated from the common source throughout the JESD204B system. Once the LMFCs of all devices in the system are aligned, the devices are synchronized and data transfer happens at the same rate and at the same instant.

High-speed applications like RADAR and electronic warfare, where multiple channels are needed to achieve higher data rates or multiple input and multiple outputs (MIMO), require a multichannel device to reduce system size, complexity, and cost. The AFE7950, a JESD204B-compliant device, supports 4-transmit and 4-receive signal chains and is a good fit for these multichannel systems with the provided clock solution. A large number of AFE7950 devices can be used in such systems requiring multiple device synchronization.

The key clocking challenges in multi-RF transceiver systems to minimize channel-to-channel skew include:

1. Synchronization of device clocks for RF transceivers
2. Synchronization of digital functions across RF transceivers

図 1-2 shows the typical setup for multiple JESD204B TX and RX device synchronization. For synchronization, the clock source requires:

1. Phase-align device clocks and sampling clocks (DCLK) at each AFE7950 device
2. In-phase SYSREF to each DCLK to meet SYSREF setup and hold time of the AFE7950
3. In-phase FPGA CLK and FPGA SYSREF, if using multiple FPGAs in a system

AFE7950 internal clocks, such as ADC sampling clock, frame clock, or LMFC, are generated from the common DCLK. Hence the DCLK phase is critical to each data converter for multiple synchronized systems.

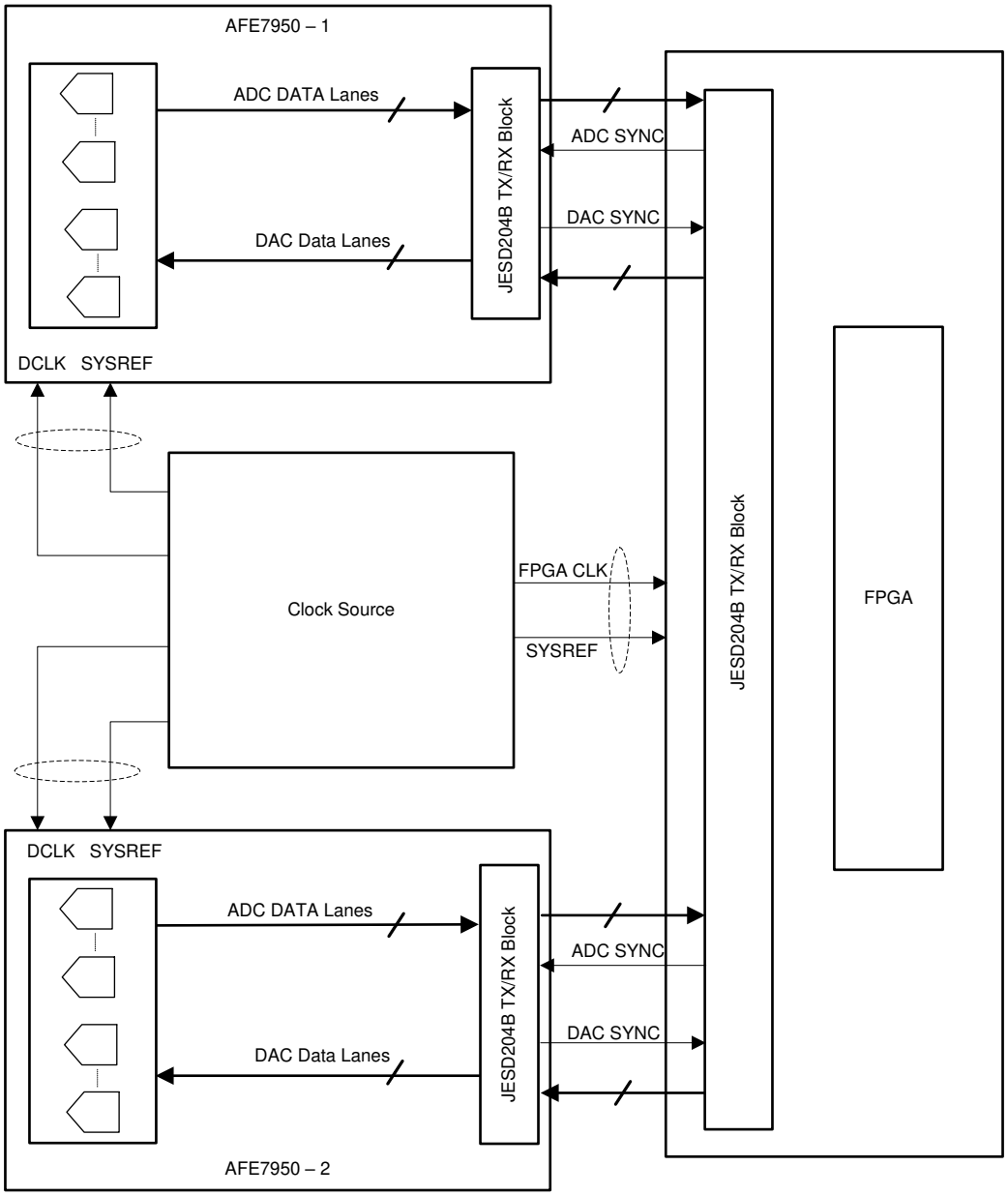


図 1-2. Synchronization Block Diagram

1.4.1.2 JESD204B-Compliant Multichannel Phase Synchronized Clocks Generation

The latest RF sampling data converter supports a JESD204B-compliant interface, which needs a high-frequency sampling clock and system reference signal called SYSREF. When clocking multiple RF transceivers, channel-to-channel skew becomes an important design consideration. Clock jitter and phase mismatch leads to deviation from the ideal sampling instant of a channel and thereby, results in channel-to-channel skew. To achieve the excellent phase noise performance at high frequencies, LMX2820 synthesizers used in this reference design, which brings down the clock jitter to around 45 fs.

図 1-3 shows the block diagram of a multichannel JESD204B-compliant clocking board. A common reference frequency can be fed externally, or generated by onboard VCXO or LMK61E2 and is provided to the LMK04832 at the OSCin input through the reference buffer LMK1C1104. The LMK04832 on this design is used to provide an FPGA reference clock and SYSREF to the TSW14J56EVM capture card through the FMC adapter board and SYSREF to AFE7950EVMs through LMX2820 in repeater mode. The LMK04832 is configured in PLL mode to phase synchronize OSCin and the remaining generated clocks.

To generate the phase-synchronized device clocks to AFE7950EVMs, a common reference frequency is input to the OSCin of the two LMX2820 synthesizers using LMK1C1104 and the SYNC signals from LMK04832. As 図 1-3 shows, SYSREF and the device clock to the AFE7950EVMs are provided through LMX2820, where SYSREF is distributed in repeater mode. For multi-device JESD204B synchronization, device clocks should be phase aligned and meet the SYSREF setup and hold time of the AFE7950 device.

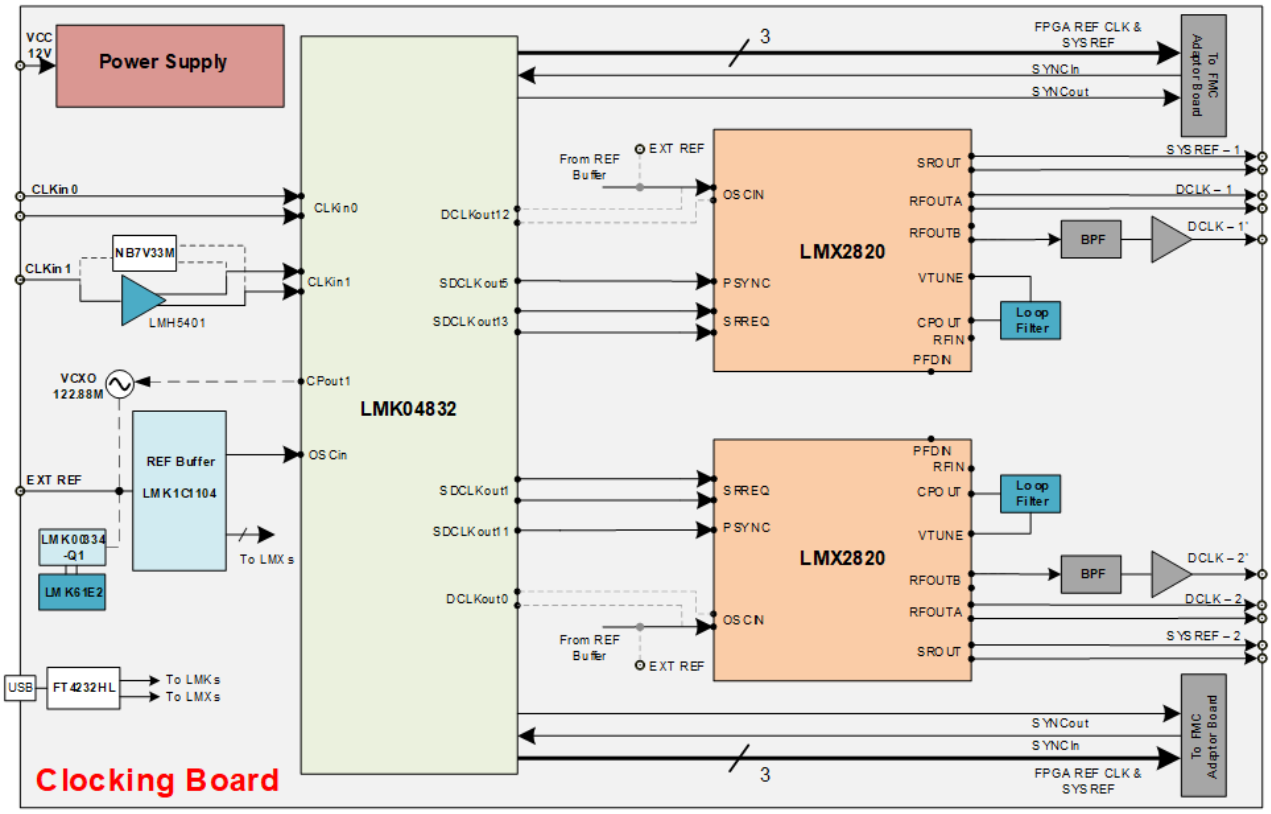


図 1-3. Clocking Board Block Diagram

図 1-4 shows the waveform of the device clocks and SYSREF to both AFE7950EVMs. In this design, the device clock of the AFE7950 is 8847.36 MHz and SYSREF setup and hold time of the AFE7950 are 50 ps each. With this, the valid window for meeting the setup and hold time is approximately 13 ps, which is less than the step size (25 ps) of SYSREF from the LMK04832. Hence, phase delay must be provided in device clocks, which is done by the MASH_SEED value in the LMX2820 as well as SYSREF phase delay in the steps of 9 ps from LMX2820. Each LMX2820 device may require tuning for the MASH_SEED delays to achieve in-phase generated clocks and meet the setup and hold time of the SYSREFs.

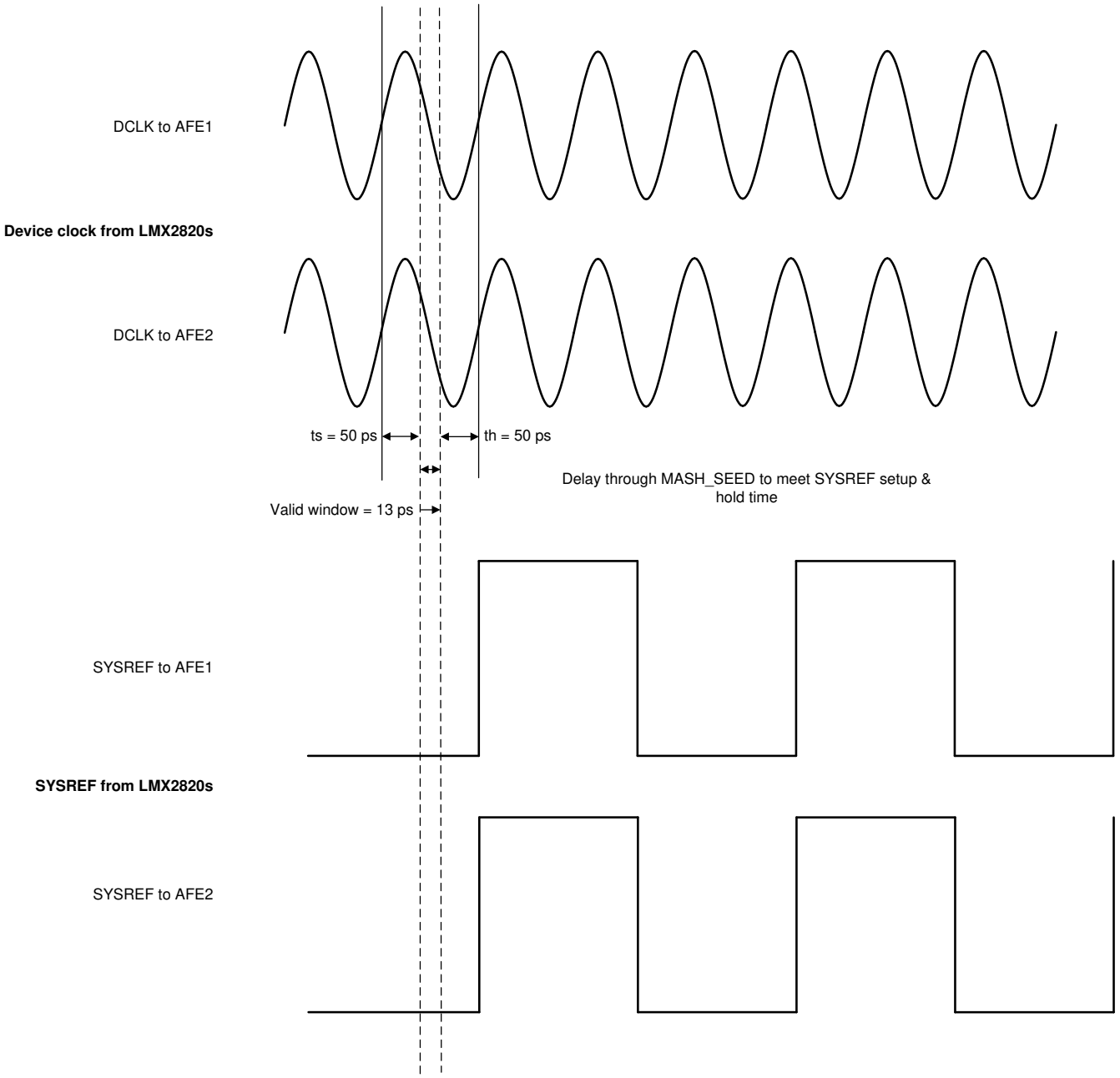


図 1-4. Clock Timing Waveforms

Reference frequency to the clocking board can be any standard frequency such as 10 MHz, 100 MHz, and so forth as per the operating clock frequency. In this design, the AFE7950 performance and synchronization test performed at 8847.36 MHz on the device clock is done to show the comparison with the internal PLL clock mode. To generate the synchronized device clock, the LMX2820 operates in integer PLL mode along with SYNC enable. The LMX2820 can operate at higher reference frequency along with phase detector frequency for better phase noise performance. In this design, an external input reference frequency of 184.32 MHz is provided to the LMX2820 devices by the sig gen through reference buffer LMK1C1104. The phase-detector frequency also changes to 184.32 MHz, and the loop filter configuration is the same as the LMX2820EVM.

表 1-2 details the loop filter component values.

表 1-2. Loop Filter Configuration

Parameter	Value
C1_LF	470 pF
C2_LF	68 nF
C3_L3	2.2 nF
R2_LF	68.1 Ω
R3_LF	18.2 Ω

1.4.2 Clock Jitter and System SNR

The ADC SNR degrades due to external clock jitter and internal ADC aperture jitter. SNR of the ADC, limited by the total jitter, is calculated as in 式 1:

$$(SNR)_{jitter} = -20\log\left(2\pi f_{in} T_{jitter}\right)\left[in\ dBc\right] \quad (1)$$

SNR of the ADC is also affected by the quantization noise of the ADC, thermal noise, and jitter. The effective SNR of ADC that includes all of these artifacts can be represented using 式 2:

$$(SNR)_{ADC} = -20\log\sqrt{\left(10^{-\frac{\mathrm{SNR}_{quantization\_noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{thermal\_noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{jitter}}{20}}\right)^2}\left[in\ dBc\right] \quad (2)$$

図 1-5 shows the effective SNR of a 14-bit ADC from Texas Instruments. The external clock jitter depends on the clock generator section and should be designed in such a way that it is not limiting the ADC SNR performance.

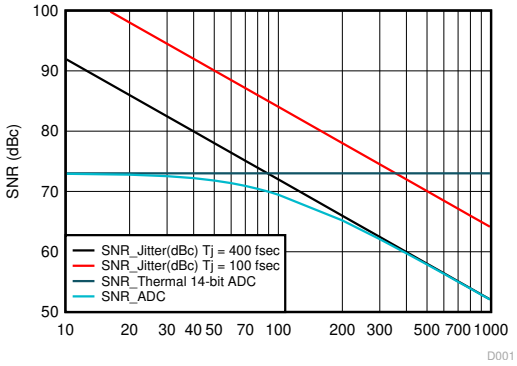


図 1-5. SNR Performance vs Input Frequency

1.4.3 Power-Supply Selection

In this design, RF PLL LMX2820 is used as a frequency synthesizer for clocking the data converter. The LMX2820 requires lower clock jitter and therefore lower phase noise to generate the required higher sampling clocks. Phase noise is directly impacted by the power supply noise and ripple.

This design has included both the 3.3-V supply options from high efficiency, low noise and low-ripple synchronous buck converter (TPS62913) and high-accuracy low noise LDO (TPS7A5301). The LMX2820 phase-noise performance measured with both supply options and results shows very equivalent results. Hence, the LMX2820 is powered up with the TPS62913 in this design and all AFE7950 performance results are with the TPS62913 on clocking board.

図 1-6 and 図 1-7 show the phase noise and jitter performance of the LMX2820 at 9-GHz operating frequency with TPS62913 and TPS7A5301.

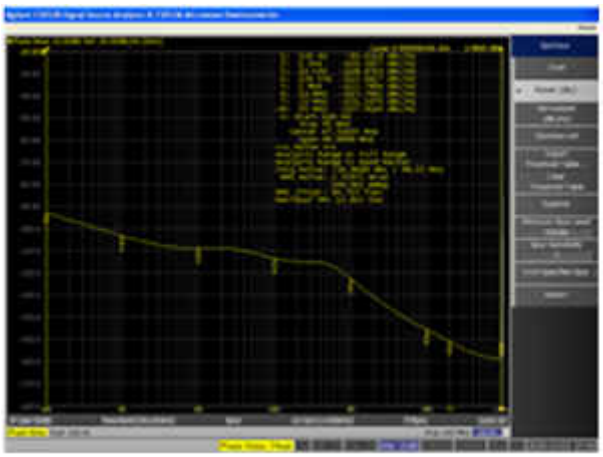


図 1-6. LMX2820 Phase Noise With TPS7A5A01

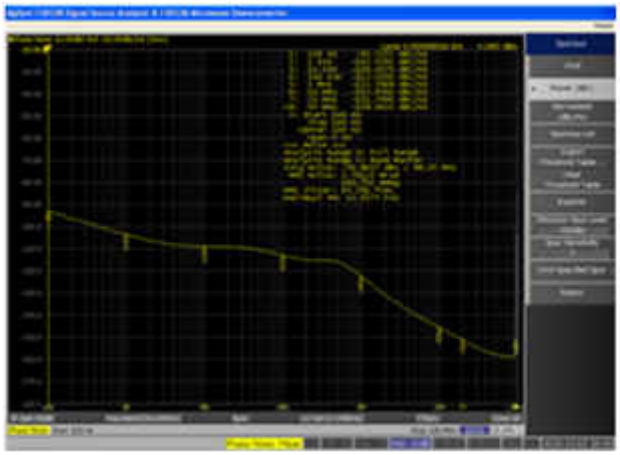


図 1-7. LMX2820 Phase Noise With TPS62913

1.4.4 Highlighted Products

1.4.4.1 AFE7950

The AFE7950 is a high-performance, quad-channel RF sampling transceiver based on 14 and 16-bit, 12-GSPS DACs and 14 and 16-bit, 3-GSPS ADCs. The AFE7950 operates up to X-band RF frequencies. The AFE7950 has 8 of JESD204B compatible SerDes transceivers running up to 15Gbps. The devices have up to two DUCs per TX channel and two DDCs per RX channel, with multiple interpolation and decimation rates and digital quadrature modulators and demodulators with independent, frequency flexible NCOs. Each ADC input path includes a DSA and RF and digital power detectors. Flexible decimation options provide optimization of data bandwidth and can support ADC BW up to 1200 MHz. The DAC signal paths support interpolation and digital up conversion options that deliver up to 2400 MHz of signal bandwidth. The differential output path includes a digital step attenuator (DSA), which provides tuning of output power.

1.4.4.2 LMX2820

The LMX2820 is a high-performance, wideband RF PLL with integrated VCO that supports a frequency range from 45 MHz to 22.6 GHz. The VCO operates from 5.65 GHz to 11.3 GHz, it uses the internal doubler to generate frequency up to 22.6 GHz. The device supports both fractional-N and integer-N modes, with a 32-bit fractional divider allowing fine frequency selection. The high performance PLL with figure of merit of –236 dBc/Hz and high phase detector frequency goes up to 300 MHz in fractional mode or 400 MHz in integer mode and can attain very low in-band noise and integrated jitter. Its integrated RMS jitter of 36-fs for a 6-GHz output makes the device an ideal low-noise source. The device accepts input reference frequency up to 1.4 GHz, which combined with frequency dividers and programmable low-noise multiplier allows flexible frequency planning. The

high speed N-divider has no pre-divider, thus significantly reducing the amplitude and number of spurs. The additional programmable low-noise multiplier lets users mitigate the impact of integer boundary spurs. In fractional-N mode, the device can adjust the output phase by a 32-bit resolution. For applications that need fast frequency changes, the device supports an ultra-fast VCO calibration option, which takes around 2.5 µs. The LMX2820 adds support for generating or repeating SYSREF (compliant to JESD204B standard) making it an ideal low-noise clock source for high-speed data converters. The LMX2820 SYSREF fine delay adjustment is provided in this configuration to account for delay differences of board traces. This device uses a single 3.3-V supply and it has integrated LDOs that eliminate the need for onboard low-noise LDOs.

1.4.4.3 LMK04832

The LMK04832 is a dual-PLL jitter cleaner and clock generator for JESD204B systems. The LMK04832 has 14 clock outputs from PLL2 which can be configured to drive seven JESD204B converters or other logic devices using device and SYSREF clocks. The LMK04832 supports two ranges of VCOs at 2440 to 2580 MHz, and 2945 to 3255 MHz. The LMK04832 also supports a distribution mode, where it accepts the high-frequency reference signal and distributes it to all 14 clock outputs without adding a PLL noise.

1.4.4.4 TPS62913 and TPS62912

The TPS62912 and TPS62913 devices are a family of high-efficiency, low-noise and low-ripple synchronous buck converters. The devices are ideal for noise-sensitive applications that would normally use an LDO for post regulation such as high-speed ADCs, clock and jitter cleaner, serializer, deserializer, and radar applications. The device operates at a fixed switching frequency of 2.2 MHz or 1 MHz, and can be synchronized to an external clock. To further reduce the output voltage ripple, the device integrates loop compensation to operate with an optional second-stage ferrite bead L-C filter. This allows an output voltage ripple below 10 μV_{RMS}. Low frequency noise levels, similar to a low-noise LDO, are achieved by filtering the internal voltage reference with a capacitor connected to the NR/SS pin. The optional spread spectrum modulation scheme spreads the DC/DC switching frequency over a wider span, which lowers the mixing spurs.

1.4.4.5 LMK1C1104

The LMK1C1104 is a low additive jitter and low-skew LVCMOS fan-out buffer solution. The low-noise floor enables the LMK1C1104 to exceed the phase noise requirements for a diverse array of applications, including but not limited to communications, enterprise computing, medical, and industrial.

2 Hardware, Software, Testing Requirements, and Test Results

2.1 Required Hardware and Software

2.1.1 Hardware

This reference design uses the following hardware:

- TIDA-010230 (LMX2820 clocking board)
- FMC adapter card
- AFE7950 EVM (AFE7950 evaluation board)
- TSW14J56EVM (JESD204B high-speed data capture and pattern generator card)

2.1.1.1 Clocking Board Setup

図 2-1 shows the multichannel LMX2820 clocking board.

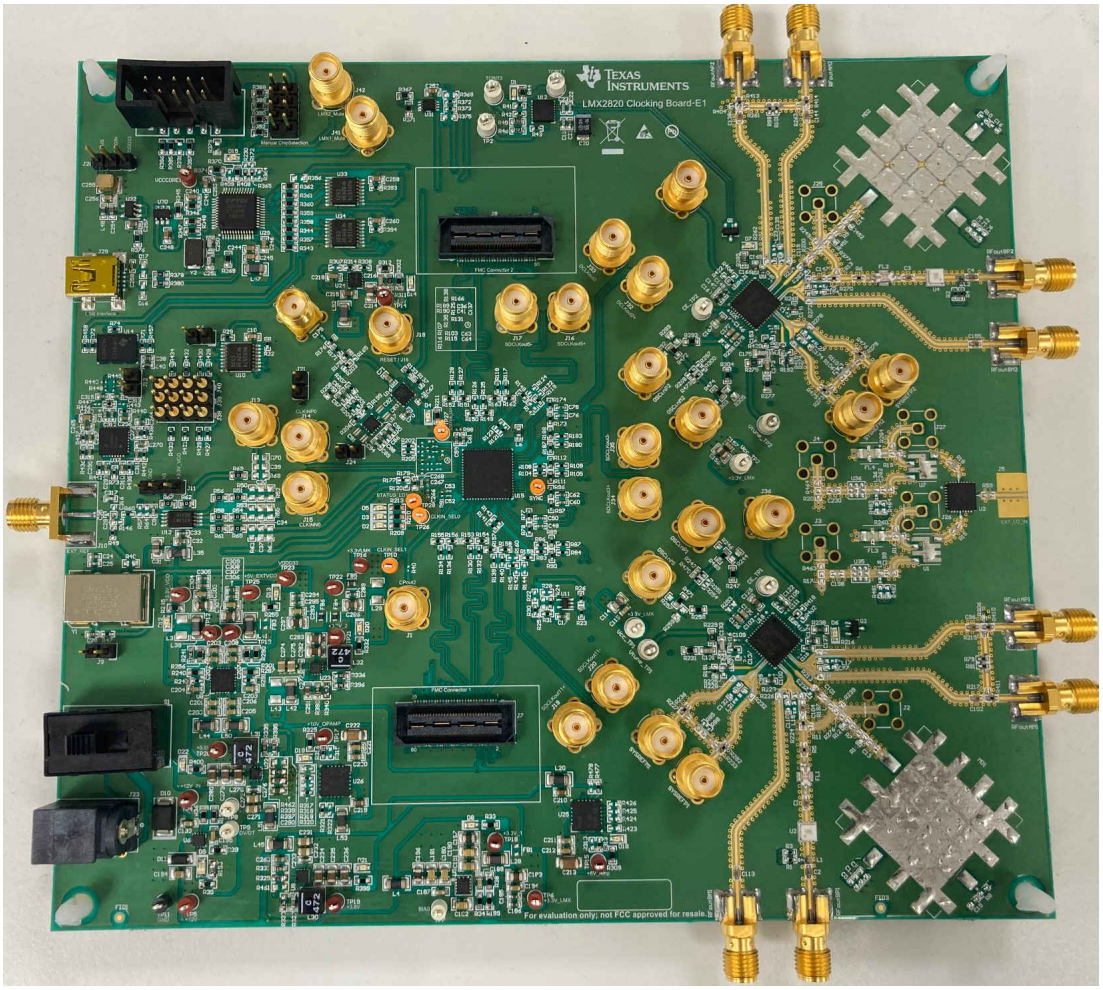


図 2-1. Multichannel Clocking Board

Reference the following for clocking board setup:

1. **Power Supply**

   Power supply connector J23: This connector is used to connect the power supply. Set the power supply to 12 V with a 3-A current limit.
2. **Input reference signals**
   - Option 1: Connect the external reference signal to EXT_REF connector (J10). While connecting the external reference, disconnect the Y1 and U14/U37 connection by removing C29 and C316, and place C35. Disconnect the power supply of Y1 and U14 by removing jumpers J9 and J12. For reference enable to the clocking devices from the reference buffer device U13, place the short jumper at pin 2-3 of jumper J11.
   - Option 2: The onboard reference LMK61E2 (U14) is powered up using the jumper J12 and factory programmed to generate a 156-MHz LVDS output. U14 can be programmed to generate different clock frequencies using the I2C interface. LVDS output is translated to LVCMOS format using U37 and output enabled by shorting pin 1 of the jumpers J39-J40. While using the onboard LMK61E2, disconnect the clock inputs from Y1 and external reference by removing C29 and C35, then place C316. Isolate the power supply to Y1 by removing J9. For reference enable to clocking devices from reference buffer device U13, place the short jumper at pin 2-3 of jumper J11.
   - Option 3: The onboard VCXO Y1 is powered on using the jumper J9 and outputs a 122.88-MHz signal to the LMK04832 OSCin_P pin input. In this option, LMX2820 devices receive the reference signals from

the LMK04832 DCLK ports. While using Y1, disconnect the clock inputs from LMK61E2 (U14) and external reference by removing C316, C35, C29, and R177, and place the R146 and R120. At the same time, isolate the power supply to U14 by removing the jumper J12.
- Option 4: Use one of the previous options, when LMK04832 works in PLL mode. When LMK04832 is operating in distribution mode, connect the external reference to external connector J18 or J22 based on operating input frequency. While operating in distribution mode, power down the Y1 and U14 by removing jumpers J9 and J12.

3. **Input sync signal**

   Connect the external sync signal at external J14 and J15 connectors to reset the LMK04832 dividers.
4. **Output signals**
   - LMX2820 amplified outputs are generated at RFoutBP1 and RFoutBP2 connectors as DCLK and are connected to AFE7950EVMs as an external sampling clock.
   - SYSREFM1 and SYSREFM2 connectors generate the low-frequency SYSREF signals for AFE7950EVM.
   - Connectors J7 and J8 generate the FPGA CLKs and SYSREFs for two TSW14J56 capture cards.
5. **Programming interface**

   Connect the USB mini cable to the onboard USB connector J29 and test the PC to program the LMX2820 clocking board devices using the clocking board software GUI.

2.1.1.2 FMC-to-FMC Adapter Board Setup

The FMC-to-FMC adapter board provides the FPGA clocks to the TSW14J56 capture card from the LMX2820 clocking board or AFE7950EVM along with the data lanes directly connected from the AFE7950EVM to the capture card. Follow the adapter board schematic to connect the FPGA clocks and SYSREFs from the clocking board.

2.1.1.3 AFE7950EVM Setup

See the AFE79xxEVM User's Guide for the AFE7950EVM hardware setup procedure.

The AFE7950EVM has both internal PLL as well as external options for clocking the AFE. In external clock mode, feed the external clock signal at the REF_CLK_HIGH (J12) connector and SYSREF at the LMK_CLK_IN (J14) connector of LMK04828 and use in distribution mode, from the clocking board. To enable the external clock signal from the clocking board, move R373, R372 to R370, R371; move R368, R369 to R366, R367; and add 0 Ω at L40, L41.

2.1.1.4 TSW14J56EVM Setup

This design requires two TSW14J56EVMs to establish a JESD204B link with two AFE7950EVMs and to synchronize both JESD204B links. Both TSW14J56EVMs are set up in primary and secondary mode to ensure the alignment of the JESD204B link and input and output data alignment individually. For more information, see the *TSW14J56 JESD204B High-Speed Data Capture and Pattern Generator Card User's Guide* and the *High Speed Data Converter Pro GUI User's Guide*.

2.1.1.5 Hardware Setup of Multiple Transceiver Synchronization

The proposed LMX2820 clocking solution is interfaced with two AFE7950EVMs and two TSW14J56EVM capture cards to show the synchronization between multiple AFE7950 devices. 図 2-2 shows the overall block diagram of the multiple transceiver synchronized system.

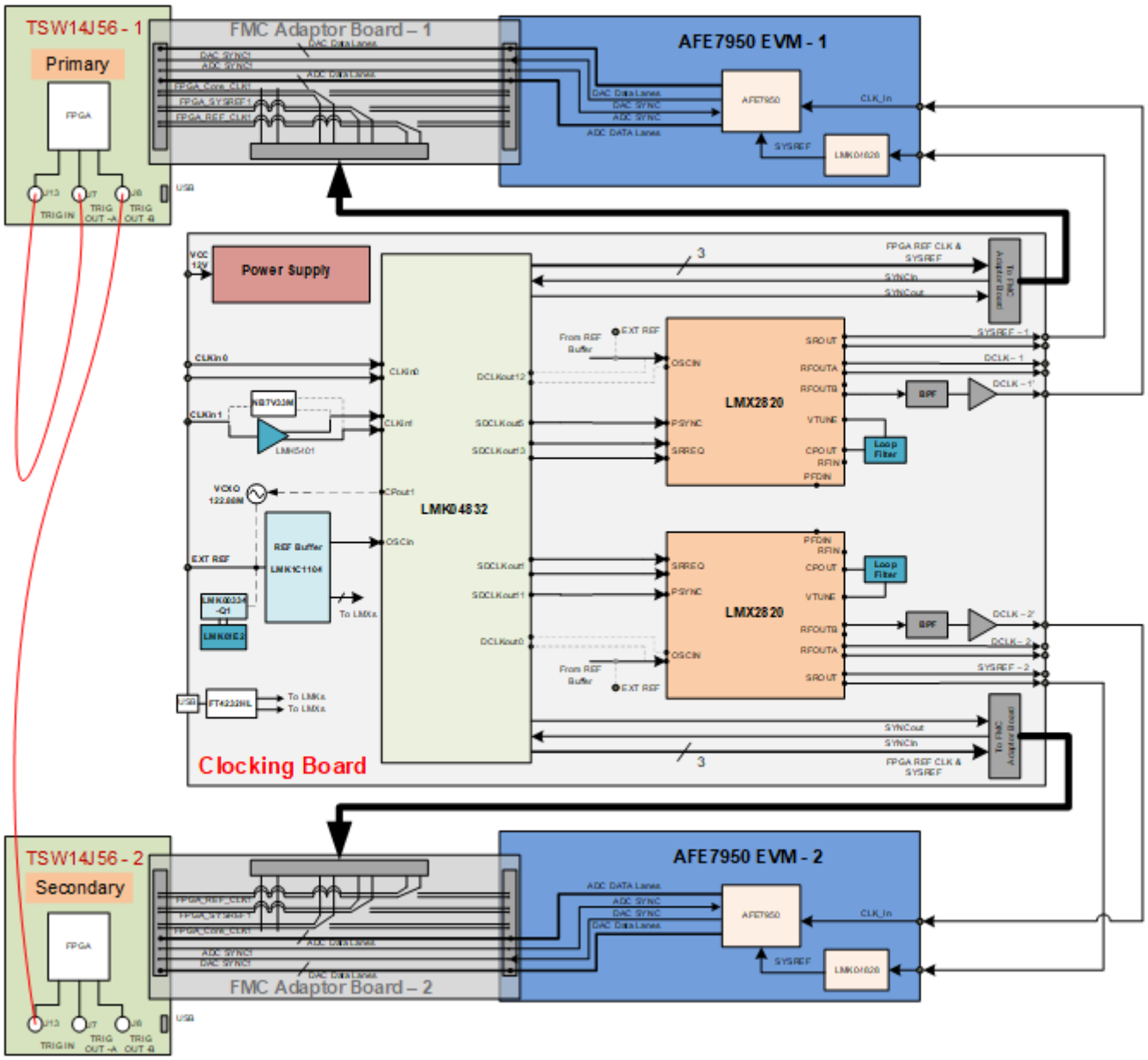


図 2-2. TIDA-010230 Device Synchronization Block Diagram

表 2-1 shows the AFE7950 operating modes and frequency requirements for various tests in this design.

表 2-1. AFE7950 Mode Setup

Parameters \ Test	TX Performance	RX Performance	Synchronization Test
Transmitter Mode	**44210**	**-**	**44210**
Interpolation	18	-	18
DAC Sampling Frequency (MHz)	8847.36	-	8847.36
Interpolated DAC clock rate (MHz)	491.52	-	491.52
K	16	-	16
F	2	-	2
Lane rate (Mbps)	9830.4	-	9830.4
Receiver Mode	**-**	**44210**	**24410**
Decimation	-	6	12

表 2-1. AFE7950 Mode Setup (continued)

Parameters \ Test	TX Performance	RX Performance	Synchronization Test
ADC Sampling Frequency (MHz)	-	2949.12	2949.12
Decimated output rate (MHz)	-	491.52	245.76
K	-	16	32
F	-	2	4
Lane rate (Mbps)	-	9830.4	9830.4
SYSREF Frequency (MHz)	1.92	1.92	1.92
FPGA Clock (MHz)	245.76	245.76	245.76

The AFE7950EVM was tested with the proposed LMX2820 clocking solution for various test cases and modes to see the transmitter and receiver performance and compare with the data sheet performance along with a synchronization test for common frequency settings.

2.1.2 Software

This reference design uses the following software:

- LMX2820 clocking GUI (used to program TIDA-010230 LMX2820 clocking board)
- Latte SW (AFE7950 EVM GUI)
- HSDC Pro (TSW14J56EVM GUI)

2.1.2.1 TIDA-010230 Clocking Board GUI

The TIDA-010230 clocking board includes the FTDI device, which needs to be programmed once to support the SW GUI. An FTDI utility, *FT Prog*, is installed from the web. 図 2-3 shows the product description is set to the TIDA010230.

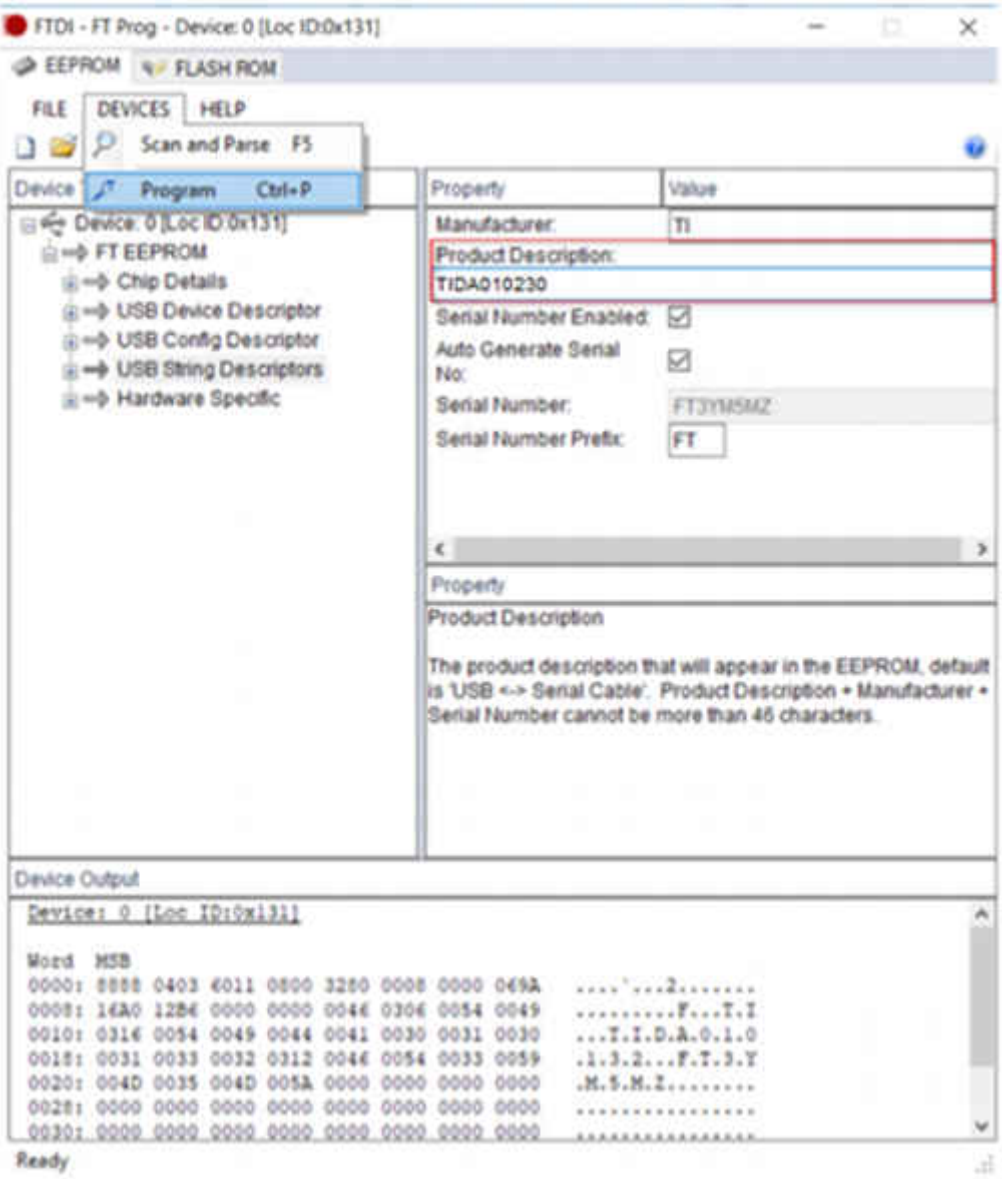


図 2-3. FTDI Software Setup

The TIDA-010230 GUI interfaces with the TIDA-010230 clocking hardware to configure all clocking devices on the board. Install this software from the Software section of the TIDA-010230 reference design folder.

2.1.2.2 AFE7950 EVM GUI

The AFE7950 EVM uses the Latte SW for programming purposes. Download the latest Latte SW from the TI secure folder and install it on the test PC.

2.1.2.3 High-Speed Data Converter (HSDC) Pro

The HSDC pro software interfaces with the TSW14J56EVM to support data transfer and capture to the AFE7950 EVM through a JESD204B link. Install the software from *DATACONVERTERPRO-SW*.

For more information, see the AFE7950EVM user guide and the *High-Speed Data Converter Pro GUI* user's guide.

2.1.2.4 Programming Steps

This section helps to provide the guidance to program each board in the TIDA-010230 reference design.

Use セクション 2.1.2.5 and セクション 2.1.2.6 to configure all boards in the synchronization test.

2.1.2.5 Clocking Board Programming Sequence

All devices in the clocking board are configured by loading the configuration files in the low-level view page.

1. Load the *LMK04832_2949.12M_184.32MREF_SYSREF_SYNC.cfg* file to program onboard LMK04832 to generate FPGA REF clock and SYSREFs
2. Load the *LMX2820_A_B_8847.36M_184.32MREF_SYSREF_REPT_SYNC.cfg* file to generate synchronized device clocks at 8847.36 MHz and SYSREF in repeater mode from LMX2820s
3. Once all other boards are programmed, turn off the SYSREF to AFE7950EVM by setting **Active/Logic Low** for SDCLK1 and SDCLK13 from the clocking board

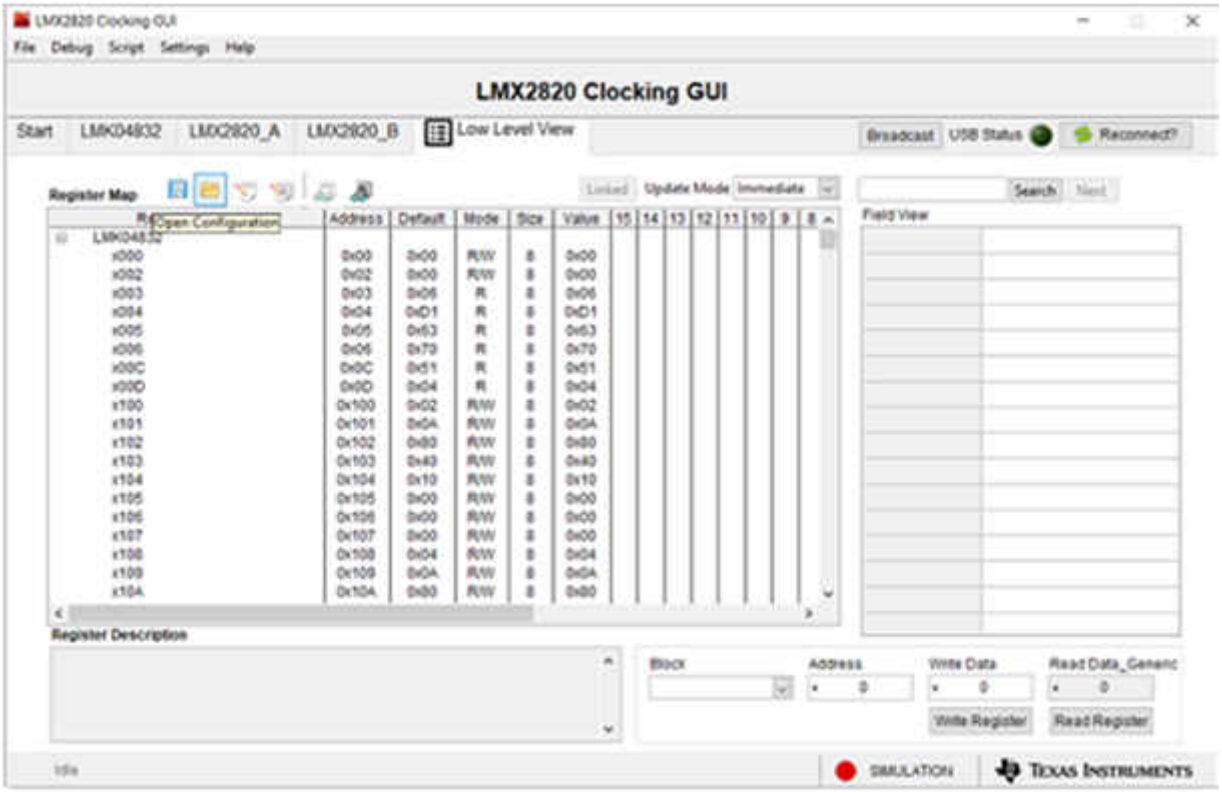


図 2-4. LMX2820 Clocking GUI

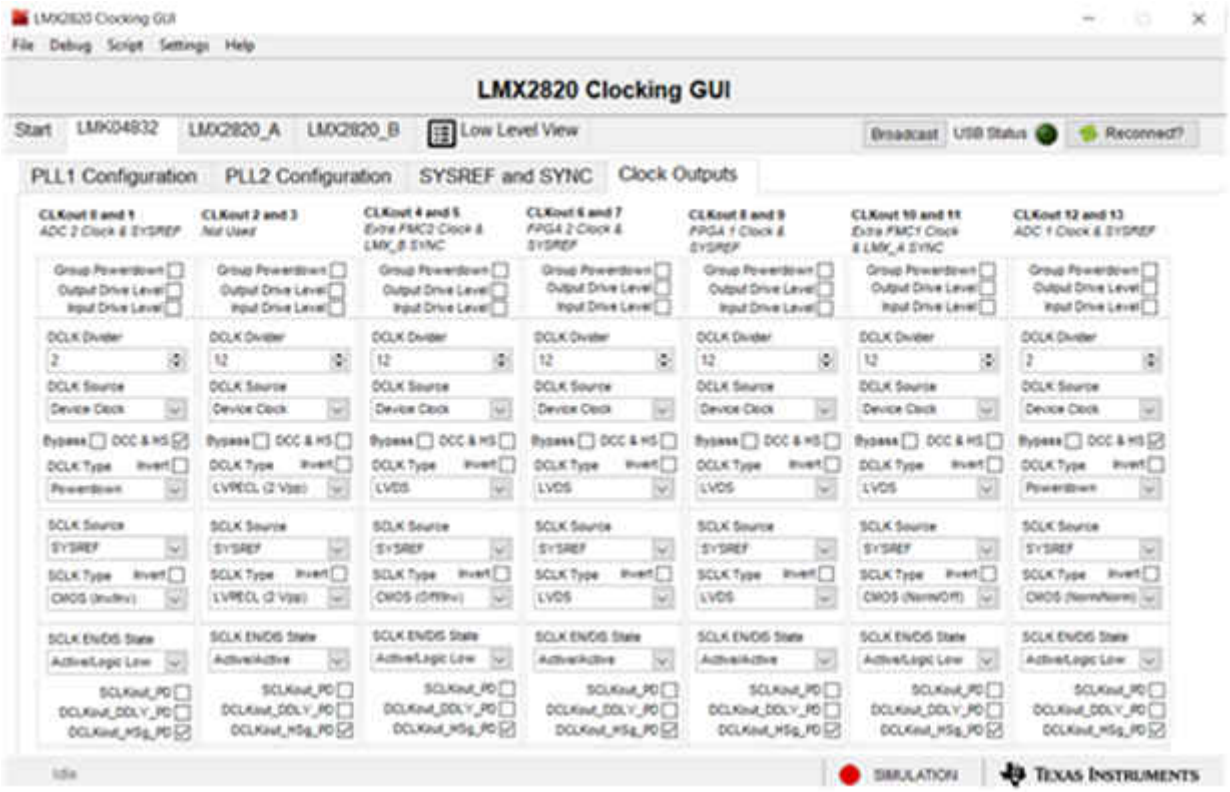


図 2-5. LMX2820 Clocking GUI With LMK04832 Tab

2.1.2.6 Latte SW and HSDC Pro Setup

Once the clocking board is programmed, open the Latte software and HSDC Pro software on the same test PC.

For a synchronization test, each AFE7950EVM and TSW14J56EVM pair must be connected to a separate PC running the Latte software and HSDC Pro software.

1. Select the *AFE79xx_TSW14J56_Mode1_Ext_SYSREF_1.py* automation script and run (press F5) in Latte SW. The script will bypass the external SYSREF through the onboard LMK04828, configure AFE7950 device and configure the TSW14J56EVM. Also synchronize the both AFE7950 devices in different EVMs.
2. After AFE EVM setup and HSDC Pro setup, run step 3 from セクション 2.1.2.5
3. For the synchronization test, use HSDC pro tools in trigger mode

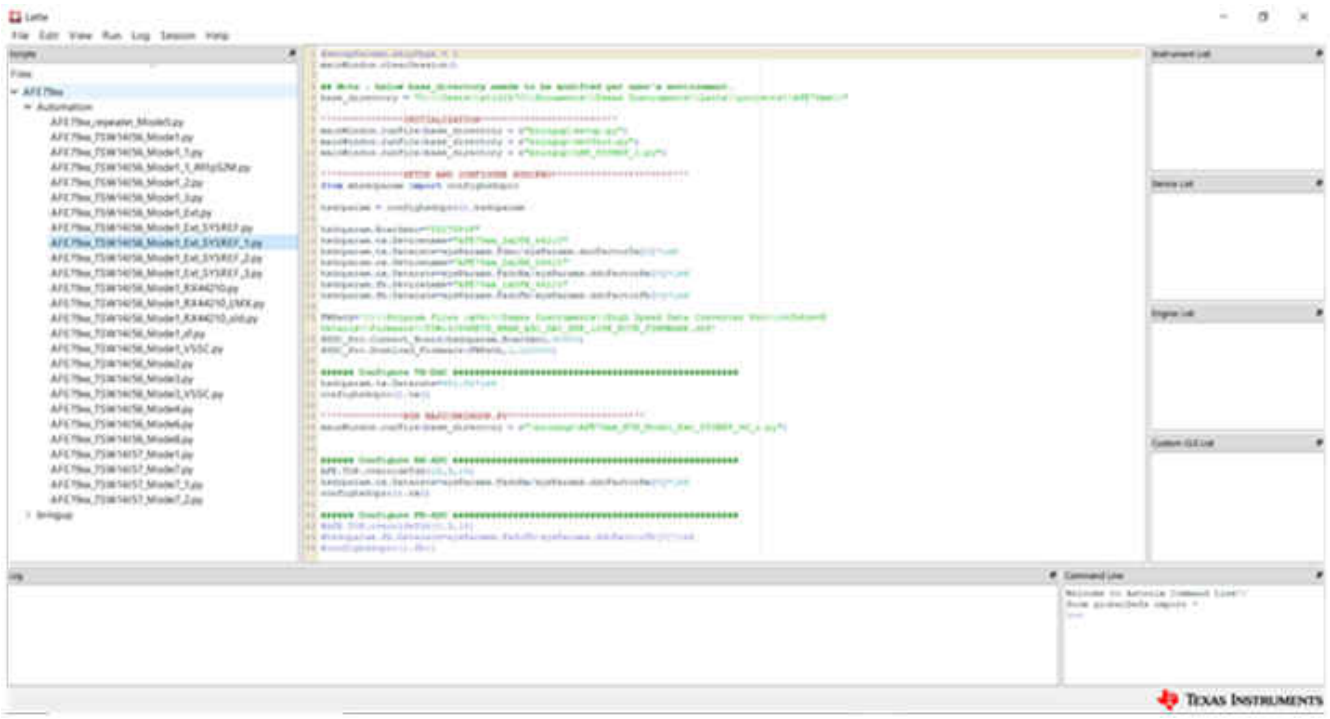


図 2-6. AFE7950 GUI

2.2 Test Setup

図 2-7, 図 2-8, 図 2-9, and 図 2-10 show the test setup for LMX2820 phase noise measurement, transmitter performance (SFDR, IMD3) measurement, receiver SNR measurement, and channel-to-channel skew measurement for multiple AFE7950s, respectively.

Use the following steps for each test setup:

1. Connect a 12-V/3-A power supply to the J23 connector of the clocking board.
2. Connect two separate 5-V/4-A power supplies to the J35 connector of both AFE7950EVMs.
3. Connect two separate 5-V/3-A power supplies to the J11 connector of each TSW14J56EVM.
4. Follow the programming sequence in Section 2.1.2 for each board based on the test setup.

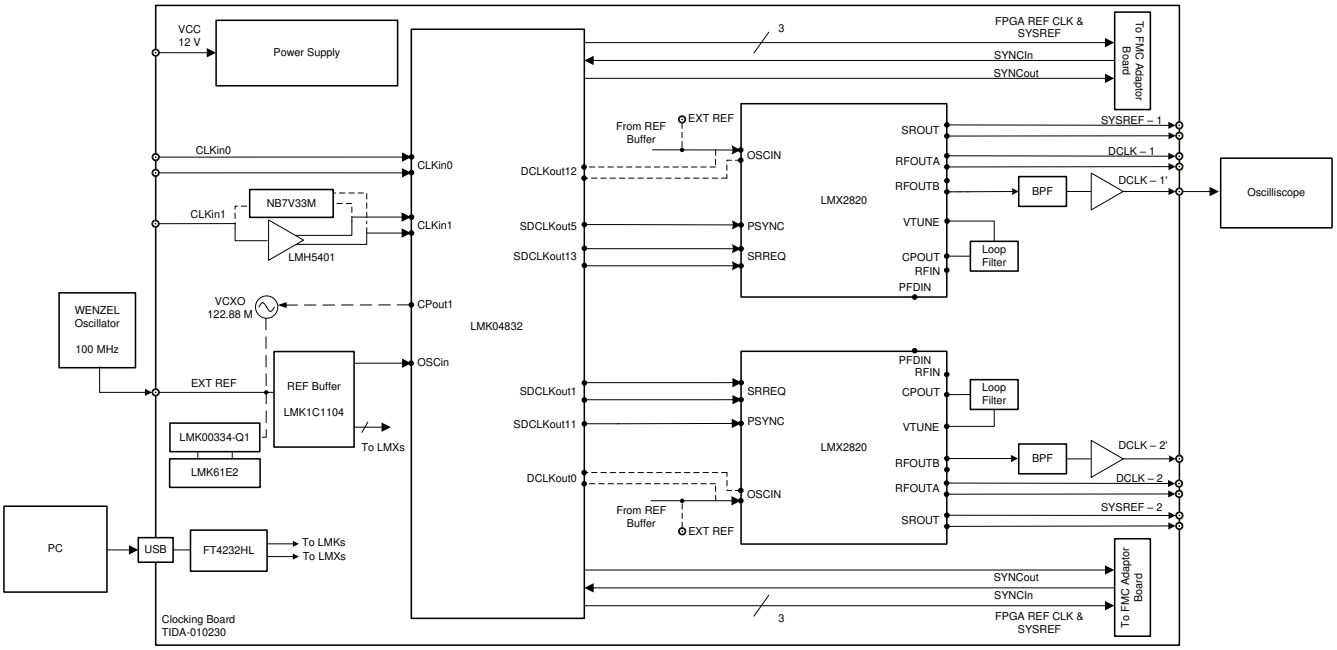


図 2-7. Test Setup for LMX2820 Phase-Noise Measurement

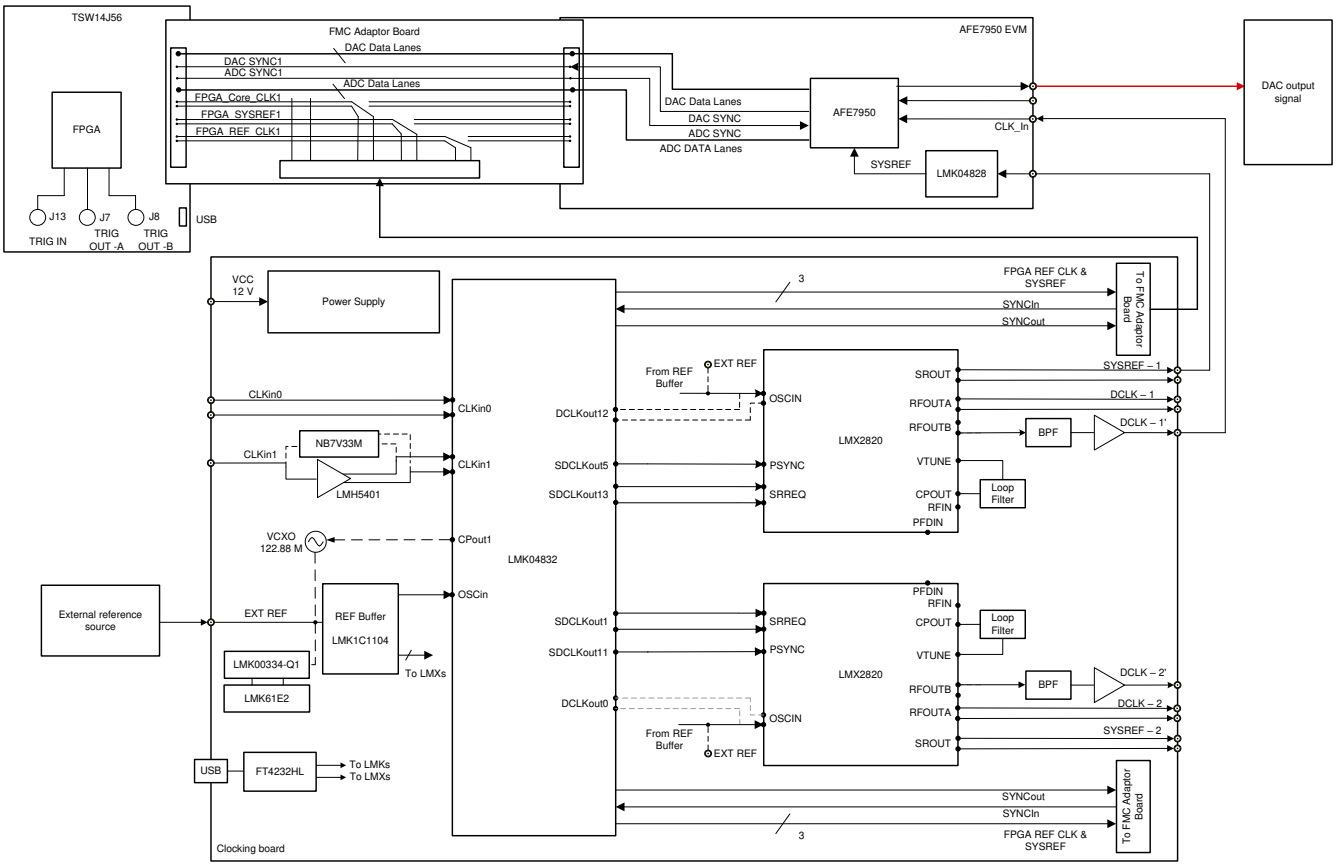


図 2-8. Test Setup for AFE7950 Transmitter SFDR and IMD3 Measurement

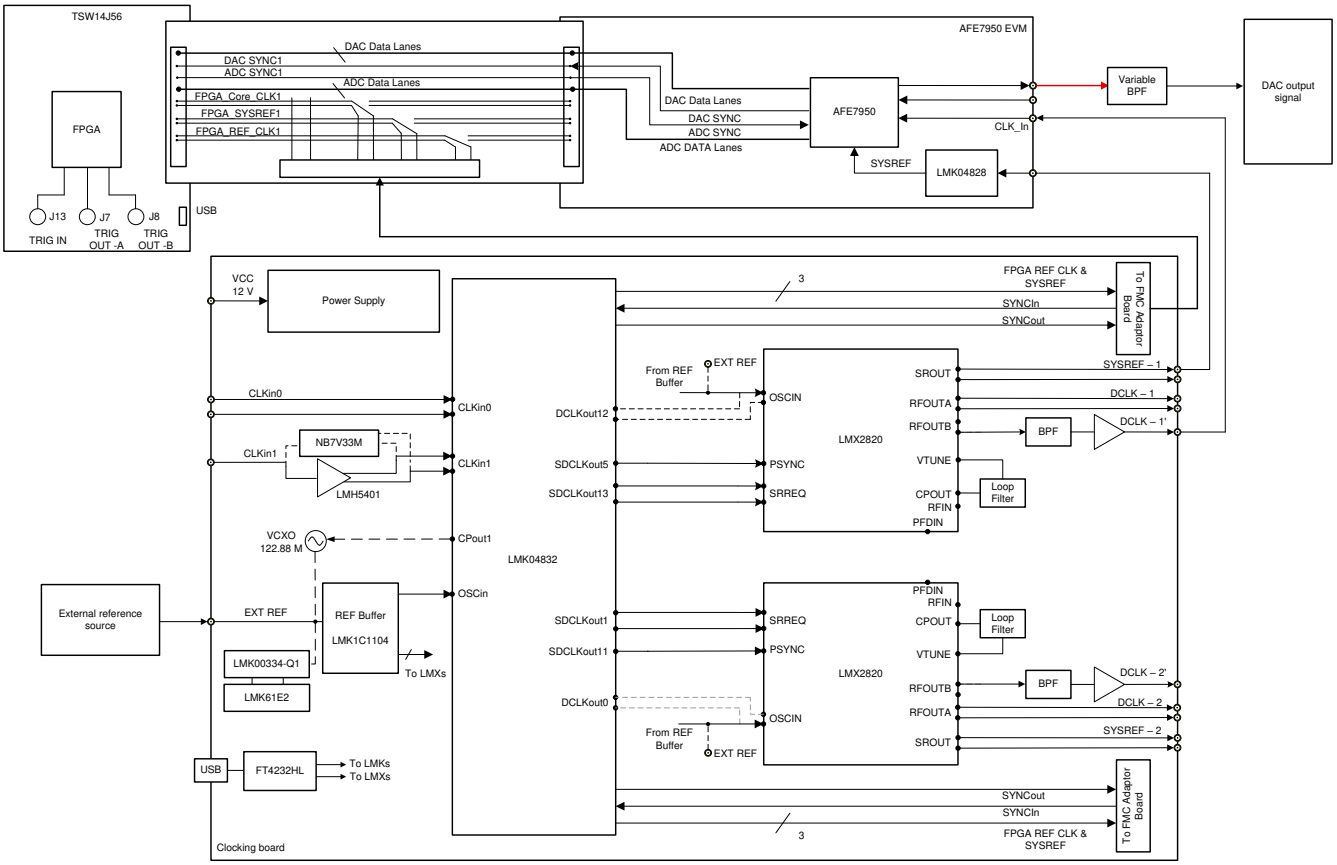


図 2-9. Test Setup for AFE7950 Receiver SNR Measurement

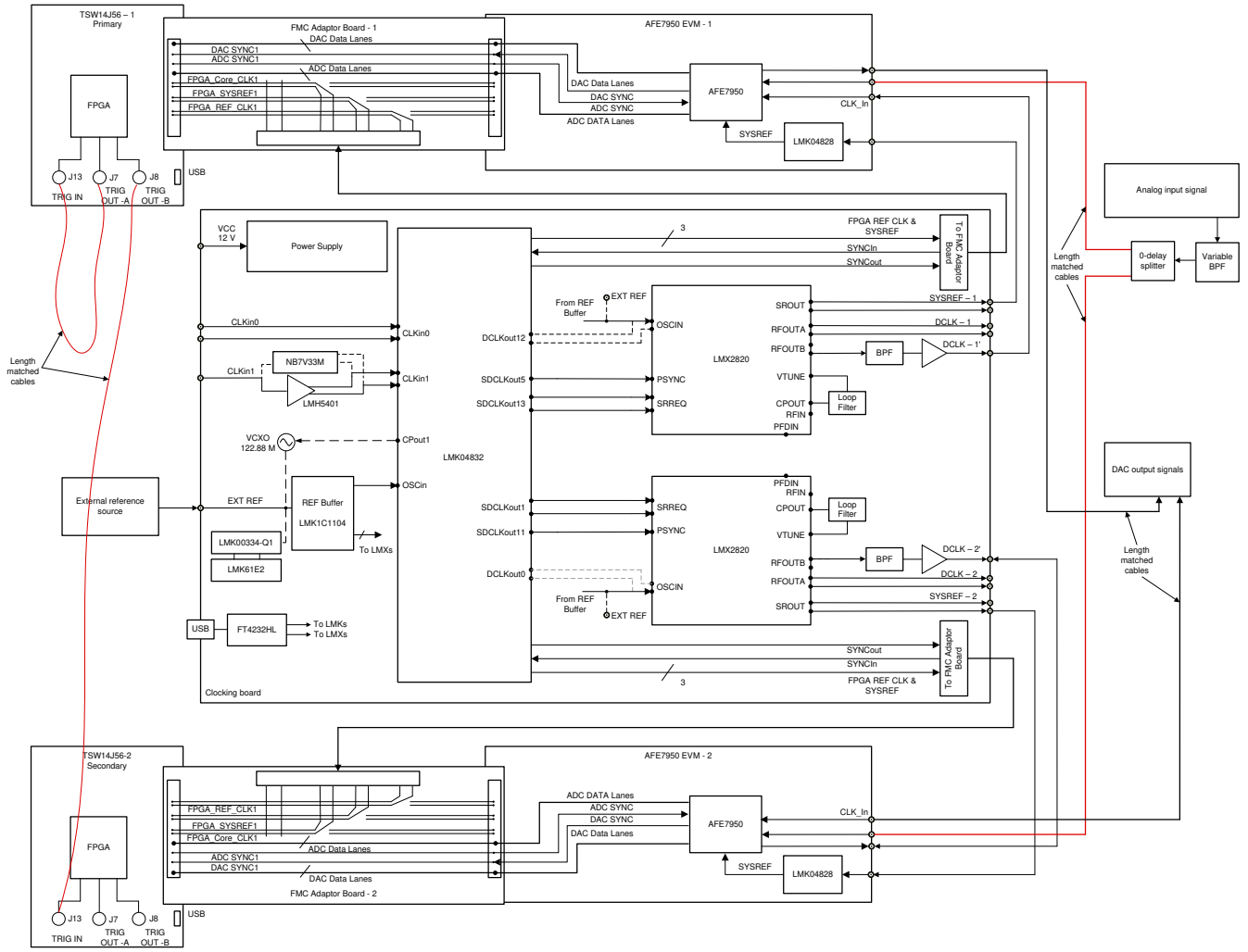


図 2-10. Test Setup for Two AFE7950 Analog Channel-to-Channel Skew Measurement

2.3 Test Results

2.3.1 LMX2820 Phase-Noise Performance

TIDA-010230 clocking board LMX2820 devices show almost the same results because both are identical on the board. 表 2-2 shows the measured phase noise performance of the LMX2820 on clocking board and comparing with LMX2820EVM results at various clock frequencies.

表 2-2. LMX2820 Phase-Noise Comparison

Output Frequency (GHz)	Condition	LMX2820 EVM Measured Phase Noise (dBc/Hz)	Clocking Board Measured Phase Noise (dBc/Hz)
6	10-kHz offset	–111.7	–111.9
	100-kHz offset	–117.5	–116.3
	1-MHz offset	–126.4	–125.9
	10-MHz offset	–149.9	–149.7
	95-MHz offset	–158.9	–159.5
11	10-kHz offset	–106.9	–107.3
	100-kHz offset	–111.2	–110.2
	1-MHz offset	–122.1	–122.5
	10-MHz offset	–144.5	–144.9
	95-MHz offset	–157.2	–156.3

表 2-2. LMX2820 Phase-Noise Comparison (continued)

Output Frequency (GHz)	Condition	LMX2820 EVM Measured Phase Noise (dBc/Hz)	Clocking Board Measured Phase Noise (dBc/Hz)
22	10-kHz offset	–100.3	–101.5
	100-kHz offset	–104.7	–104.1
	1-MHz offset	–116.3	–116.3
	10-MHz offset	–138.7	–139.1
	95-MHz offset	–149.9	–149.3

2.3.2 AFE7950 Transmitter Performance

表 2-3 shows the measured transmitter performance results in terms of SFDR and IMD3 for 2x2TX_44210 mode and an interpolation factor of 18. Measured SFDR and IMD3 of the AFE7950 with the proposed TIDA-010230 clocking solution are improved from the AFE7950EVM using the internal PLL clocks and is comparable with the external clock source from the signal generator.

表 2-3. Transmitter Performance

Parameters	Conditions	Unit	AFE7950 Data Sheet Specifications	TIDA-010230 Measured	AFE7950EVM Measured (INT CLK)	AFE7950EVM Measured (EXT CLK)
SFDR	For 0-FDAC/2 BW, DSA – 0 dB, –1 dBFS;					
850 MHz		dBc	50.8	34.35	33.98	34.1
1800 MHz		dBc	51.9	45.21	44.15	45.15
2600 MHz		dBc	42	45.17	40.3	45.48
3500 MHz		dBc	44	45.94	43.95	42.4
4900 MHz		dBc	46.1	39.62	39.3	39.12
8100 MHz		dBc	46.1	29.3	29	30.05
SFDR	For Fout ±250 MHz BW, DSA – 0 dB, –1 dBFS;					
850 MHz		dBc	68.5	72.64	72.09	72.92
1800 MHz		dBc	79.4	70.66	67.91	71.19
2600 MHz		dBc	77	71.3	68.3	68.96
3500 MHz		dBc	75	70.12	65.73	68.11
4900 MHz		dBc	76	67.44	62	62.67
8100 MHz		dBc	75	59.9	60.55	60.63
IMD3	IMD3 for ±10 MHz tone offset, DSA – 0dB, –13 dBFS each tone					
850 MHz ±10 MHz		dBc	–74.4	–70.65	–53.35	–55.43
1800 MHz ±10 MHz		dBc	–71.1	–75.7	–78.96	–79.01
2600 MHz ±10 MHz		dBc	–73	–72.28	–73.33	–72.42
3500 MHz ±10 MHz		dBc	–72	–71.95	–73.94	–72.35
4900 MHz ±10 MHz		dBc	–67.8	–65.32	–61.54	–62.94
8100 MHz ±10 MHz		dBc		–76.24	–73.94	–73.57

2.3.3 AFE7950 Receiver Performance

表 2-4 shows the measured SNR performance of the AFE7950 receiver for 2x2RX_44210 mode and decimation factor of 6 at various frequencies. Measured SNR of the receiver with the proposed TIDA-01230 clocking solution is improved compared to the AFE7950 internal PLL clocks and is comparable with the external clock source from the signal generator.

表 2-4. AFE7950 Receiver Performance

Parameters	Conditions	Unit	AFE7950 Data Sheet Specifications	TIDA-010230 Measured	AFE7950EVM Measured (INT CLK)	AFE7950EVM Measured (EXT CLK)
SNR	DSA – 4 dB, –3 dBFs input signal					
840		dBFs	63.2	67.29	67.29	67.36
1750		dBFs	60.9	66.15	66.2	66.68
2610		dBFs	62.5	64.6	64	64.5
3700		dBFs	62.2	62.19	60.4	62.57
4910		dBFs	60	60.44	59	60.87
9500		dBFs		44.4	44.21	44.33

2.3.4 Multiple AFE7950s TX and RX Alignment

Synchronized clocks are critical for multichannel systems. This section shows the multichannel synchronized clocking performance while measuring the channel-to-channel skew between the transmitter and receiver of the two AFE7950EVMs, respectively. The time-skew test is performed between the two channels of AFE7950EVMs at different frequencies operating in L and S band RADAR applications.

The skew of the transmitter channel is evaluated by measuring skew between the generated outputs of the DAC of each AFE in a high-speed oscilloscope. 表 2-5 shows the channel-to-channel skew at 8847.36-MHz DAC sampling frequency and the achieved skew was less than 5 ps for each output frequency.

表 2-5. Measured TX Channel-to-Channel Skew

Operating Frequency	Measured Time Skew (ps)
850 MHz	4.4
1800 MHz	5.3
2600 MHz	5.4

The skew of the receiver channel is evaluated by calculating the phase difference between signals captured from each ADC of the AFE. 表 2-6 shows the channel-to-channel skew at a 2949.12-MHz sampling frequency. The measured time skew was less than 10 ps for each input frequency.

表 2-6. Measured RX Channel-to-Channel Skew

Operating Frequency	Measured Time Skew (ps)
840 MHz	4.4
1750 MHz	0.31
2610 MHz	0.18
3700 MHz	3.56
4910 MHz	3.84

2.3.5 Summary and Conclusion

The TIDA-010230 is a low-noise JESD204B-compliant clocking reference design for a multichannel, RF-transceiver system, which is suitable for RADAR and electronic warfare applications. This design demonstrates a high-performance phase synchronized clock with multiple RF transceivers without affecting the performance of the data converter and shows the AFE7950 performance comparison with the proposed clocks, the external clock, and the internal PLL clocks. The system also shows deterministic latency behavior for every power on cycle with the analog channel-to-channel skew less than 10 ps.

3 Design and Documentation Support

3.1 Design Files

3.1.1 Schematics

To download the schematics, see the design files at TIDA-010230.

3.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010230.

3.2 Tools and Software

Software

To download the software files, see the design files at TIDA-010230.

3.3 Documentation Support

1. Texas Instruments, *AFE79xx Quad-Channel RF Transceiver With Feedback Path* data sheet

3.4 サポート・リソース

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4 About the Author

AJEET PAL is a systems engineer at Texas Instruments where he is responsible for developing reference design solutions for the Aerospace and Defense sector. Ajeet has ten years of experience in RF and wireless subsystem design for cellular and wireless systems. Ajeet earned his bachelor of engineering in electronics and communication engineering from the Institute of Technology & Management (ITM) University at Gwalior, India and his masters of technology in RF and microwave engineering from the Indian Institute of Technology (IIT) Kharagpur, India.

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