参考資料

Design Guide: TIDA-010241

*高性能 **Xilinx** および **Intel FPGA** 向けの柔軟な電源リファレンス・デザイン*

概要

FPGA (フィールド・プログラマブル・ゲート・アレイ) の処理能力の継続的な向上につれて、電源レール数の増加と同時に、レールあたりの要件もいっそう厳しくなっています。これらの要件を管理するには、すべてのレールに電力を供給し、シーケンシング機能を提供する、コンパクトな形態のパワー・マネージメント IC (PMIC) とコントローラが必要です。

リソース

TIDA-010241	デザイン・フォルダ
TPS650861	プロダクト・フォルダ
TPSM5D1806	プロダクト・フォルダ
TPS53688	プロダクト・フォルダ
CSD95410RRB	プロダクト・フォルダ

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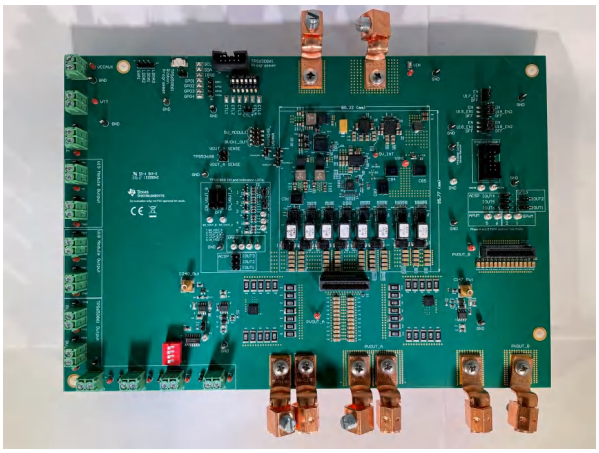
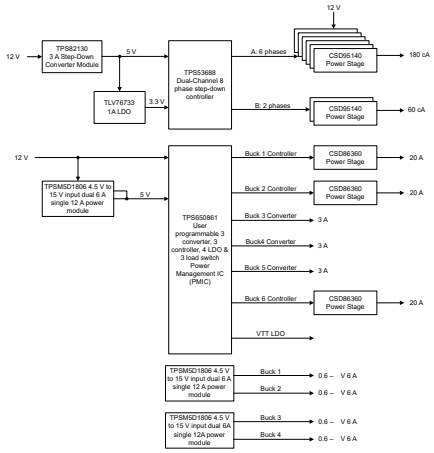
特長

- デュアル・チャネル DCAP+ コントローラ
  - コア・レールと 2 次レールの 6+2 相構成
  - PMBus と VR13.HC の SVID 機能により、動的な電圧スケーリングが可能
- 6 つの電源レールと PMIC からのシーケンシング
  - 3 つのコントローラが最大 20A を供給
  - 3 つのコンバータが最大 3A を供給
  - DDR 用の VTT レギュレータを内蔵
  - フレキシブルなプログラミングにより、カスタム シーケンシングと電源レールの割り当てが可能
- モジュール方式のコンパクトなコンバータ
  - デュアル 6A レールまたはシングル 12A レールに構成可能なモジュール

アプリケーション

- レーダー
- 電子兵器
- ソフトウェア無線
- MRI
- CT および PET スキャナ
- 超音波スキャナ
- X 線システム
- マルチパラメータ・メディカル・モニタ
- 半導体テスト
- オシロスコープおよびデジタイザ





1 System Description

図 1-1 shows that the TIDA-010241 reference design is comprised of various power components:

- The TPS53688 controller is configured in a 6 + 2 phase configuration. The six-phase output is used for the core rail of the FPGA, while the two-phase output is used for secondary core power.
- The TPS650861 PMIC has three controllers, three converters, and VTT LDO that are configurable and has flexible sequencing via software. The TPS650861 also has additional GPIOs that can be used to control external converters, or controllers for sequencing, or utilize both attributes.
- The TPSM5D1805 devices are used for any extra rails as well as providing an intermediate 5-V rail required by the three converters on the TPS650861

1.1 Key System Specification

The following tables show example or rail assignments and power trees with the Intel® Stratix® 10, Intel Agilex™, Xilinx® Versal®, and Xilinx Virtex-7® FPGAs.

1.1.1 Intel® Stratix® 10 Power Tree Example

表 1-1. Intel® Stratix® 10 Power Tree Example

PARAMETER			LOAD CAPABILITY	RAIL NAME (SEQUENCE)
Input Power Supply	Voltage	12 V	N/A	
TPS53688	Phase A (Six Phases)	0.85 V	136 A	VCC(1)
	Phase B (Two Phases)	1 V	50 A	VCCT, VCCR (2)
TPSM5D1806	Two-phase configuration	5 V	10 A	5-V Intermediate (1)
TPS650861	Buck Controller 1	0.9 V	15 A	VCCERAM, VCCPLLDIG (2)
	Buck Controller 2	1.8 V	20 A	VCCH (3)
	Buck Controller 6	1.2 V	20 A	DDR (4)
	VTT LDO	0.6 V	1.8A	DDR VTT (4)
	Buck Converter 3	1.8 V	3 A	VCCIO (4)
	Buck Converter 4	2.5 V	3 A	V2P5 (4)
	Buck Converter 5	1.2 V	3 A	V1P2(4)
	LDOA1	3 V	0.02 A	VCCIO3V(4)

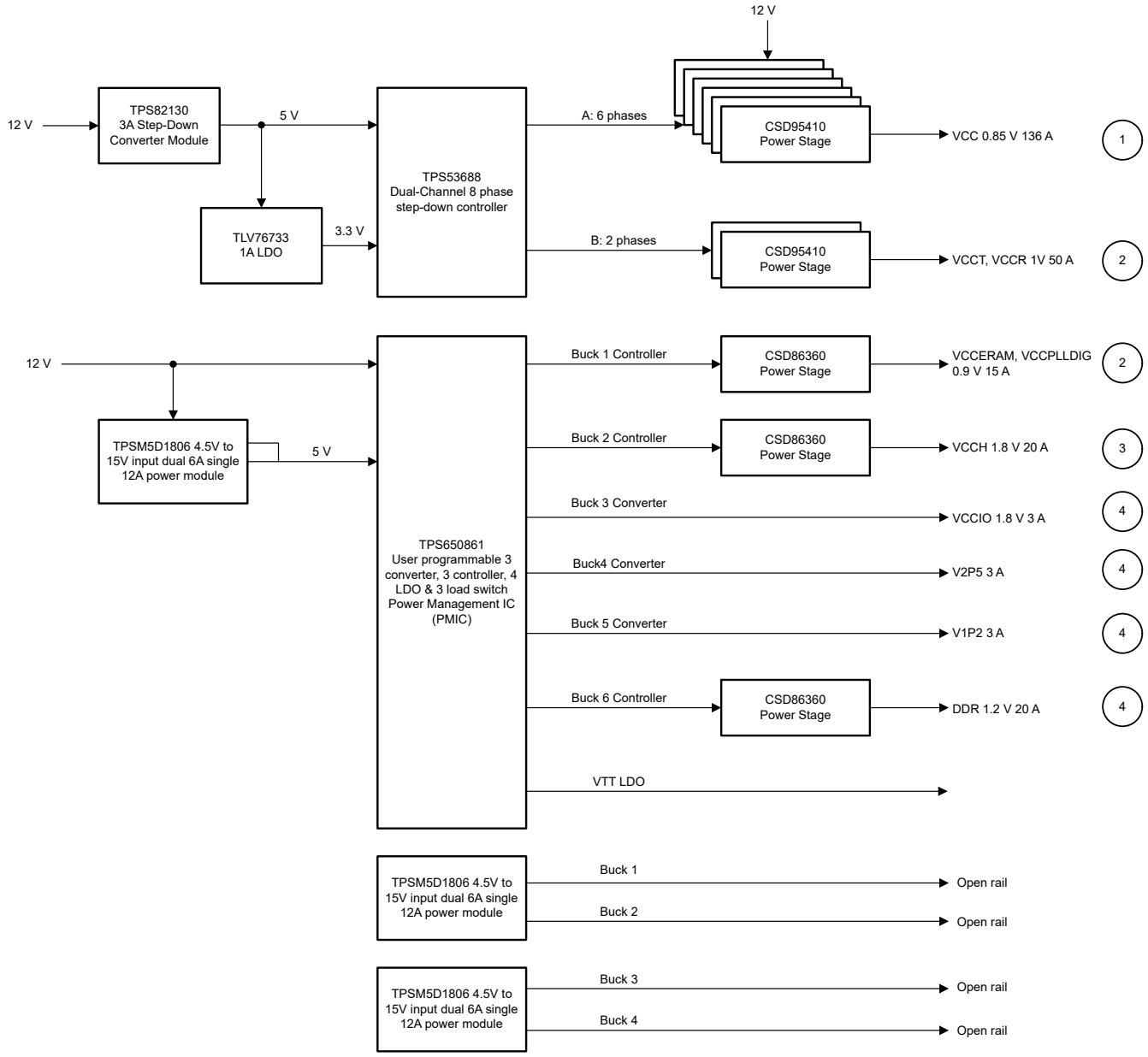


図 1-1. Intel® Stratix® 10 Power Tree Example 10 Power Tree and Rail Assignment

1.1.2 Intel® Agilex™ Power Tree Example

表 1-2. Intel® Agilex™ Power Tree Example

PARAMETER			LOAD CAPABILITY	RAIL NAME (SEQUENCE)
Input Power Supply	Voltage	12 V	N/A	
TPS53688	Phase A (Six Phases)	0.8 V	60–180 A	VCC(1)
	Phase B (Two Phases)	0.9 V	40 A	VCCT, VCCR (1)
TPSM5D1806	Buck 1	0.8 V	3 A	VCCL (1)
	Buck 2	1.1 V	4 A	VCCH (2)
TPSM5D1806	Buck 3	1.2 V	6 A	VCCIO (3)
	Buck 4	1.8 V	6 A	VCCIO (3)
TPSM5D1806	Multiphase output	Open	12 A	N/A

表 1-2. Intel® Agilex™ Power Tree Example (continued)

PARAMETER			LOAD CAPABILITY	RAIL NAME (SEQUENCE)
TPS650861	Buck Controller 1	5 V	20 A	Intermediate 5 V (1)
	Buck Controller 2	1.8 V	20 A	VCCERAM, VCCPLLDIG (2)
	Buck Controller 6	1.1–1.35 V	20 A	DDR (2)
	VTT LDO			DDR VTT (2)
	Buck Converter 3	2.5V	3 A	VCC_CLK (2)
	Buck Converter 4	2.5 V	3 A	VCCFUSE (3)
	Buck Converter 5	Open	3 A	N/A

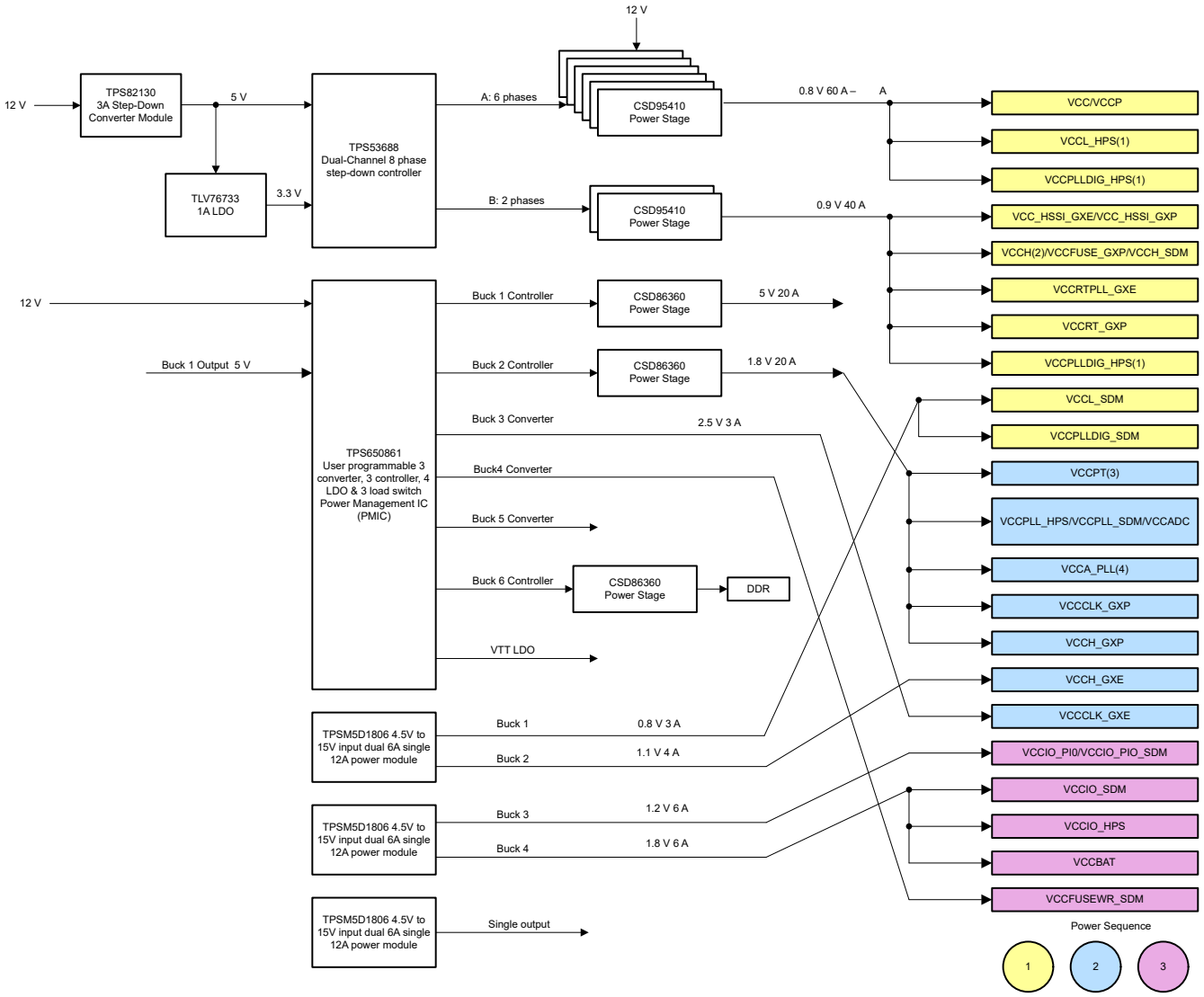


図 1-2. Intel® Agilex™ Power Tree and Rail Assignment

1.1.3 Xilinx Versal™ Power Tree Example

表 1-3. Xilinx Versal™ Power Tree Example for VM1402, 1502, 1802, 2702, VM2502-2902, VC1702-VC1902

PARAMETER			LOAD CAPABILITY	RAIL NAME (SEQUENCE)
Input Power Supply	Voltage	12 V	N/A	
TPS53688	Phase A (Six Phases)	0.8 V	+80 A	VCCINT, VCC_PSINTLP, VCC_PSINTFP, VCC_PMC (1)
	Phase B (Two Phases)	1.2 V	20 A	DDR Power(2)
TPSM5D1806	Two-phase configuration	5 V	10 A	5 V Intermediate (1)
TPSM5D1806	Buck 1	1.2 V	2 A	VCCO Option (3)
	Buck 2	1.5 V	2 A	VCCO Option (4)
TPSM5D1806	Buck 3	1.5 V	4 A	VCCAUX (10)
	Buck 4	1.1 to 3.3 V	< 3 A	VCCO(12)
TPS650861	Buck Controller 1	0.78 V	8 A	VCC_SOC, VCCBRAM, VCCINT_IO (5)
	Buck Controller 2	0.88 V	3–4 A	VMGTAVCC(9)
	Buck Controller 6	1.2 V	6 A	VMGTAVTT (7)
	Buck Converter 3	1.5 V	2 A	VMGTAVCCAUX (8)
	Buck Converter 4	3.3 V	3 A	3.3V System Rail (11)
	Buck Converter 5	Open	0.5 A	VCCO_PMIO (6)
	LDOA1	3 V	0.02 A	VCCIO3V(4)

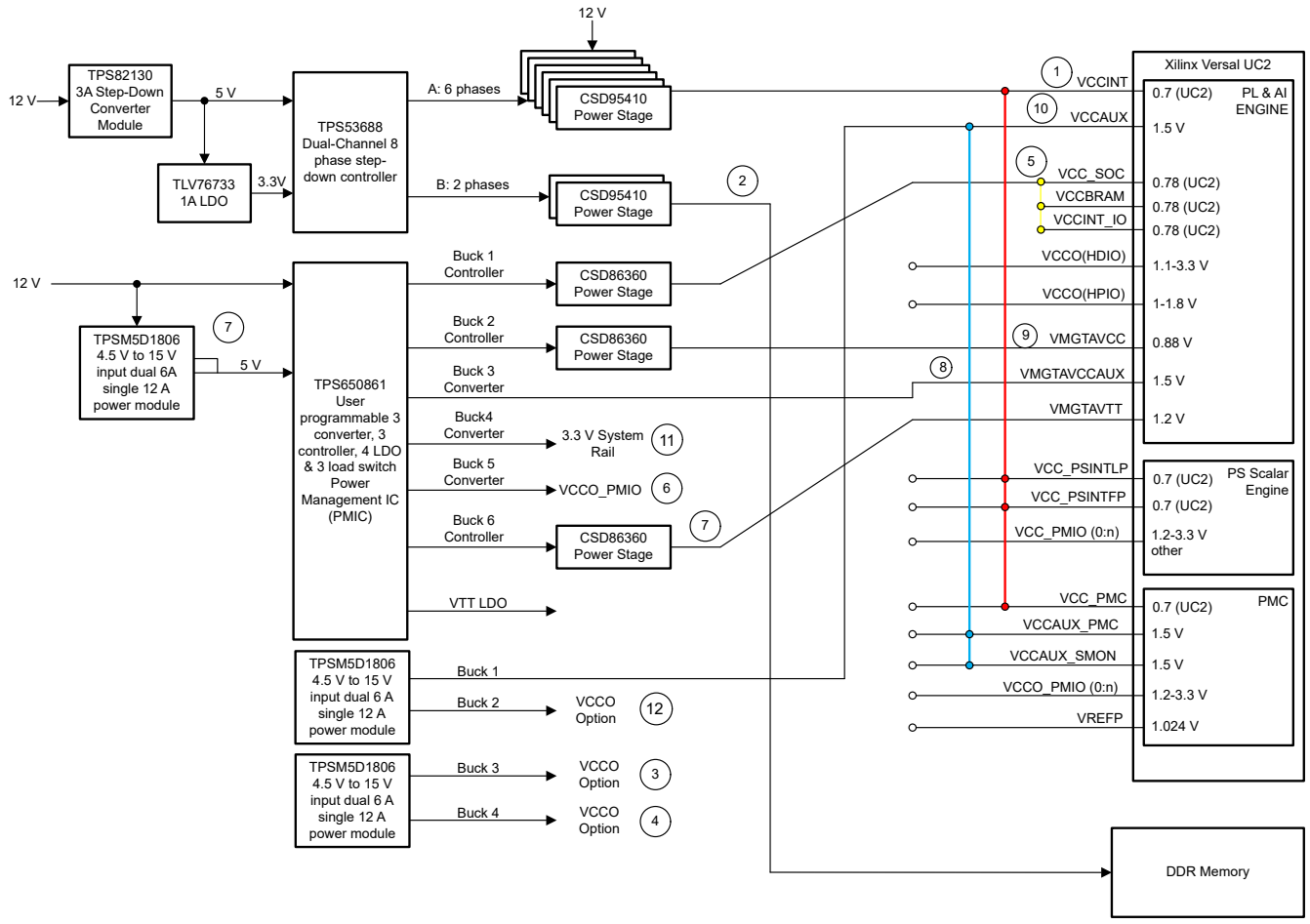


図 1-3. Xilinx Versal™ Power Tree and Rail Assignment

1.1.4 Xilinx Virtex-7® Power Tree Example

表 1-4. Xilinx Virtex-7® Power Tree Example

PARAMETER			LOAD CAPABILITY	RAIL NAME (SEQUENCE)
Input Power Supply	Voltage	12 V	N/A	
TPS53688	Phase A (Six Phases)	0.85 V	155 A	VCCINT, VCCBRAM, VCCINT_IO(1)
	Phase B (Two Phases)	1.2 V	25 A	VCCHMB(2)
TPSM5D1806	Two-phase configuration	5 V	10 A	5-V Intermediate (1)
TPSM5D1806	Buck 1	1.8 V	6 A	VCC1V8 (10)
	Buck 2	0–1.8 V	6 A	VADJ (11)
TPSM5D1806	Buck 3	1.2 V	6 A	QDR4_VDDQ_1V2 (8)
	Buck 4	Open	6 A	N/A

表 1-4. Xilinx Virtex-7® Power Tree Example (continued)

PARAMETER			LOAD CAPABILITY	RAIL NAME (SEQUENCE)
TPS650861	Buck Controller 1	1.2 V	20 A	MGTAVTT(3)
	Buck Controller 2	0.9 V	10 A	MTAVCC (6)
	Buck Controller 6	1.2 V	10 A	RLD3VDDQ_1V2(4)
	Buck Converter 3	1.2 V	3 A	DDR4 VDDQ (5)
	Buck Converter 4	1.8 V	1 A	MGTVCCAUX (7)
	Buck Converter 5	2.5 V	1 A	VCCAUX (9)

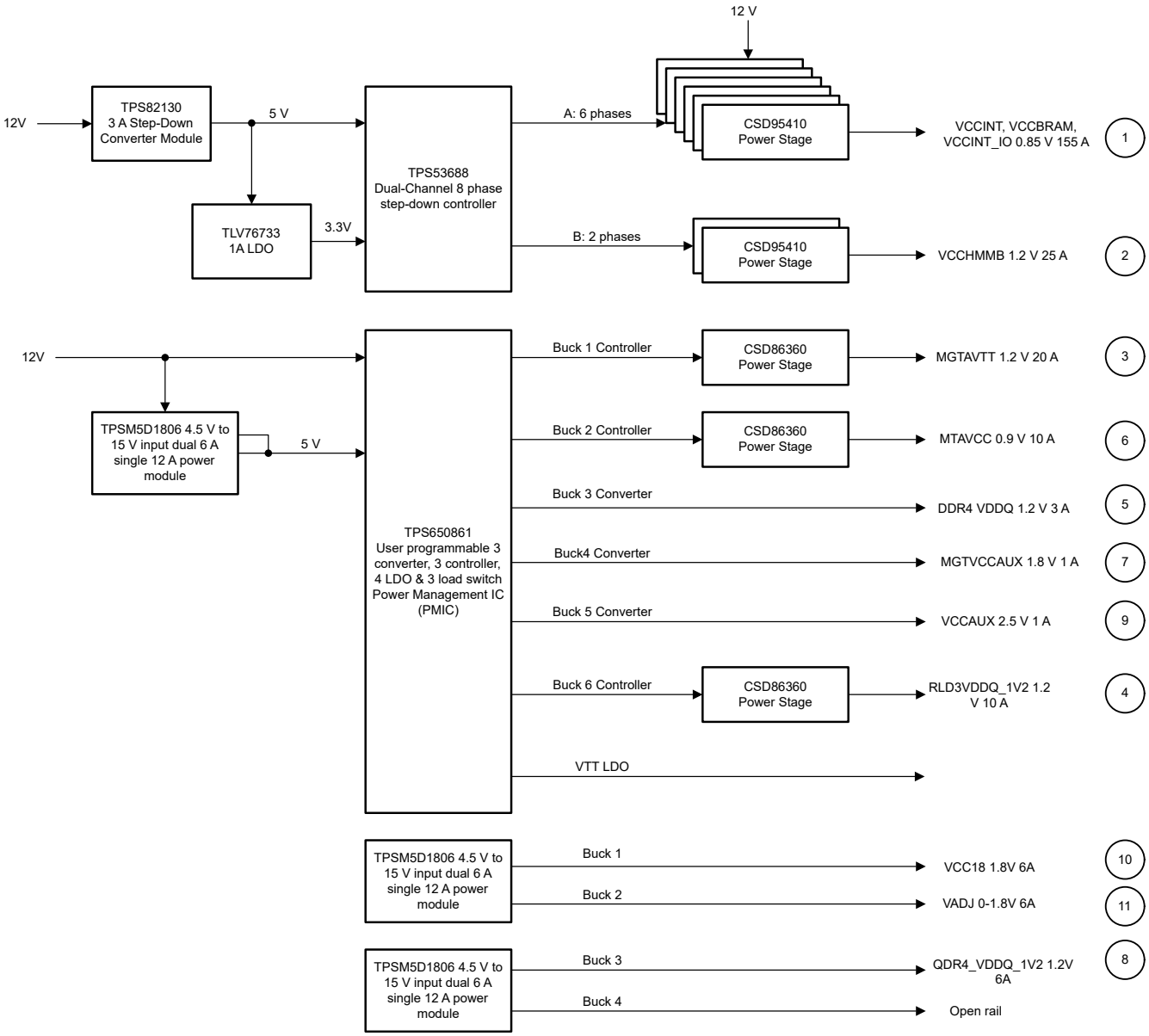


図 1-4. Xilinx Virtex-7® Power Tree and Rail Assignment

2 System Overview

2.1 Block Diagram

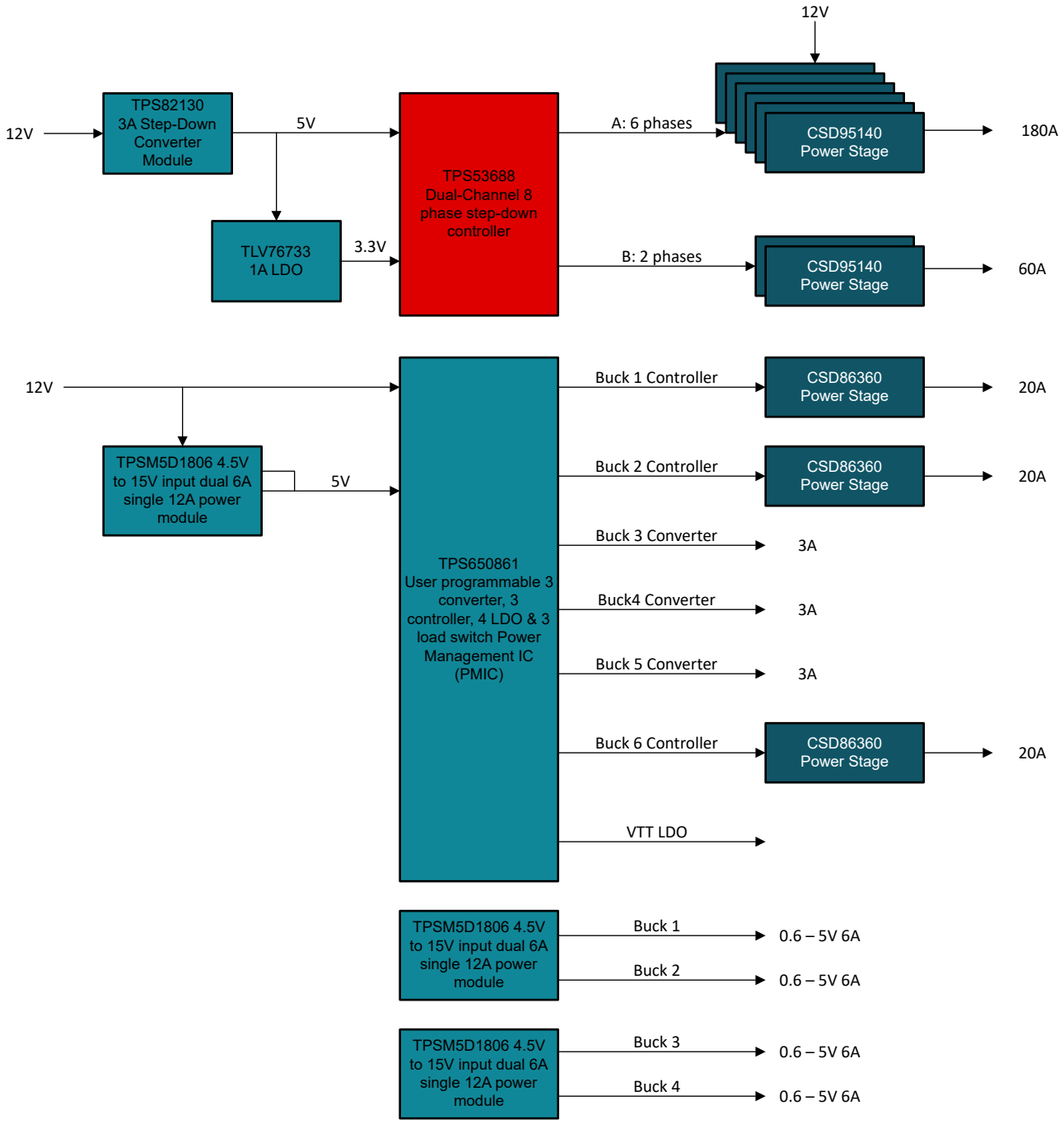


図 2-1. System Block Diagram

2.2 Design Considerations

In certain applications, these FPGAs are used on VPX cards which have a limited amount of space in all three dimensions. The layout of the design must fit within the 100-mm × 100-mm space of VPX cards. The Z axis is another constraint, with both passive component and ICs needing to be less than < 5 mm. This allows additional room for heat sinks and better cooling for VPX cards that are already slotted very closely with each other. Furthermore, this design needs to have flexibility in the rail assignment and sequence to match up to a wide variety of Intel and Xilinx power supplies.

2.3 Highlighted Products

2.3.1 TPS53688

From a performance standpoint the TPS53688 is capable of handling the high-current requirement and low-voltage output that is required for the core current rail for the FPGA. Furthermore the feedback scheme of DCAP+ allows it to have very good transient capabilities to achieve the typical < 1% requirement need on the core rail. Furthermore, its PMBUS and VR13.HC SVID allows it to interface with Intel and Xilinx FPGAs to provide dynamic voltage scaling (DVS) to the core rail to adjust the voltage depending on the mode the FPGA is operating in.

2.3.2 TPS650861

The TPS650861 is a configurable PMIC with one-time programmable memory (OTP) where the sequencing and the output voltage can be set on start-up. The device can also be interfaced via I2C for easy configuration changes. The TPS650861 device has three controllers that utilize D-CAP2™ technology allowing very good transient performance to meet FPGA requirements. The device also includes a VTT LDO that can be used for DDR memory in conjunction with Buck 6 of the TPS650861. Furthermore, there are three converters as well that require a 5-V input to the TPS650861, but these are lower current rails that used for the accessory rails on the FPGA.

The power sequencing is controlled by the TPS650861 and can be set with OTP. The TPS650861 has four GPIOs can be programmed to turn on independently in the sequence or come up with the other regulators in the TSP650861. Additionally, the TPS650861 comes with six CTRL pins that can also be used for sequencing. For example, if an external converter has power good functionality, the converter can be tied to one of the six CTRL pins to trigger the rest of the sequence.

For more information on the how to program the TPS650861, there is a booster pack evaluation kit to help users easily program the TPS650861. Additionally, the *TPS65086100 Non-Volatile Memory Programming Guide* steps users through the programming process.

2.3.3 TPSM5D1806

The TPSM5D1806 is a module that can either be dual 6-A converters, or a single 12-A multiphase converter. Furthermore, because the TPSM5D1806 is a module, the overall solution size is relatively small for the power output it is capable of providing. The TPSM5D1806 is used for higher current accessory rails, system rails, and is used to provide the 5-V intermediate rail needed by the TPS650861 converters.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

The following list shows all of the hardware needed to power up the design and communicate with the TPS650861 PMIC, TPSM5D1806 power module, and the TPS53688 controller. The power supply must be able to supply 12 V and must be able to supply a current of at least 20 A.

- PC with USB Port
- USB2ANY Interface adaptor to program the TPS650861
- USB-TO-GPIO USB interface adapter EVM to program the TPS53688
- Power supply
- Electronic load

図 3-1 shows how to connect to the board to program the TPS650861 and the TPS53688.

3.2 Test Setup

3.2.1 TPS53688 Programming Setup

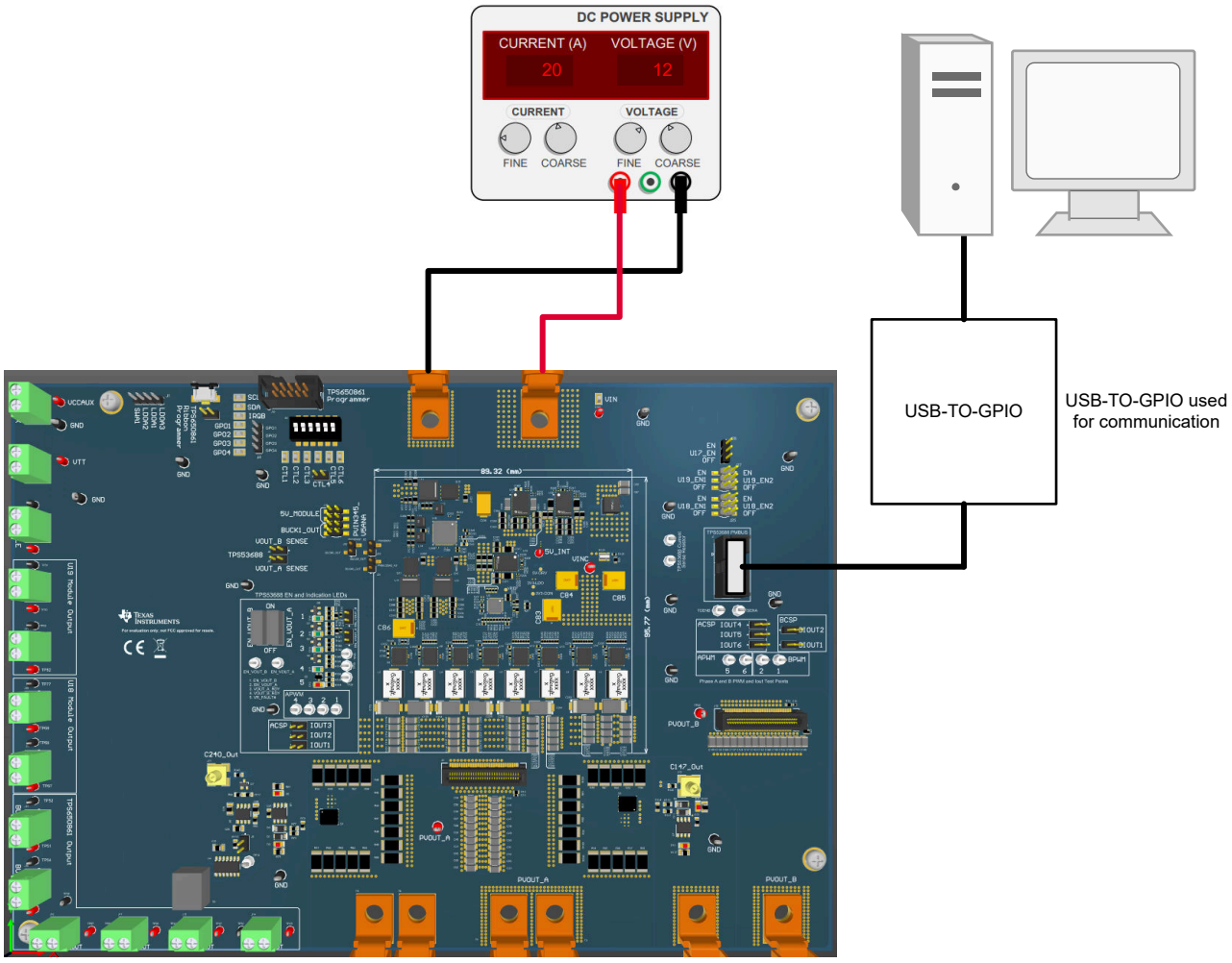


図 3-1. TPS53688 USB-to-GPIO Setup

To adjust the settings for the TPS53688, the USB-to-GPIO and the FUSION-PRODUCTIO-GUI are needed to interface between the board and the computer. For more information on how to interface with the TPS53688, request the full data sheet on the product page on ti.com

3.2.2 TPS53688 Transient Test Setup

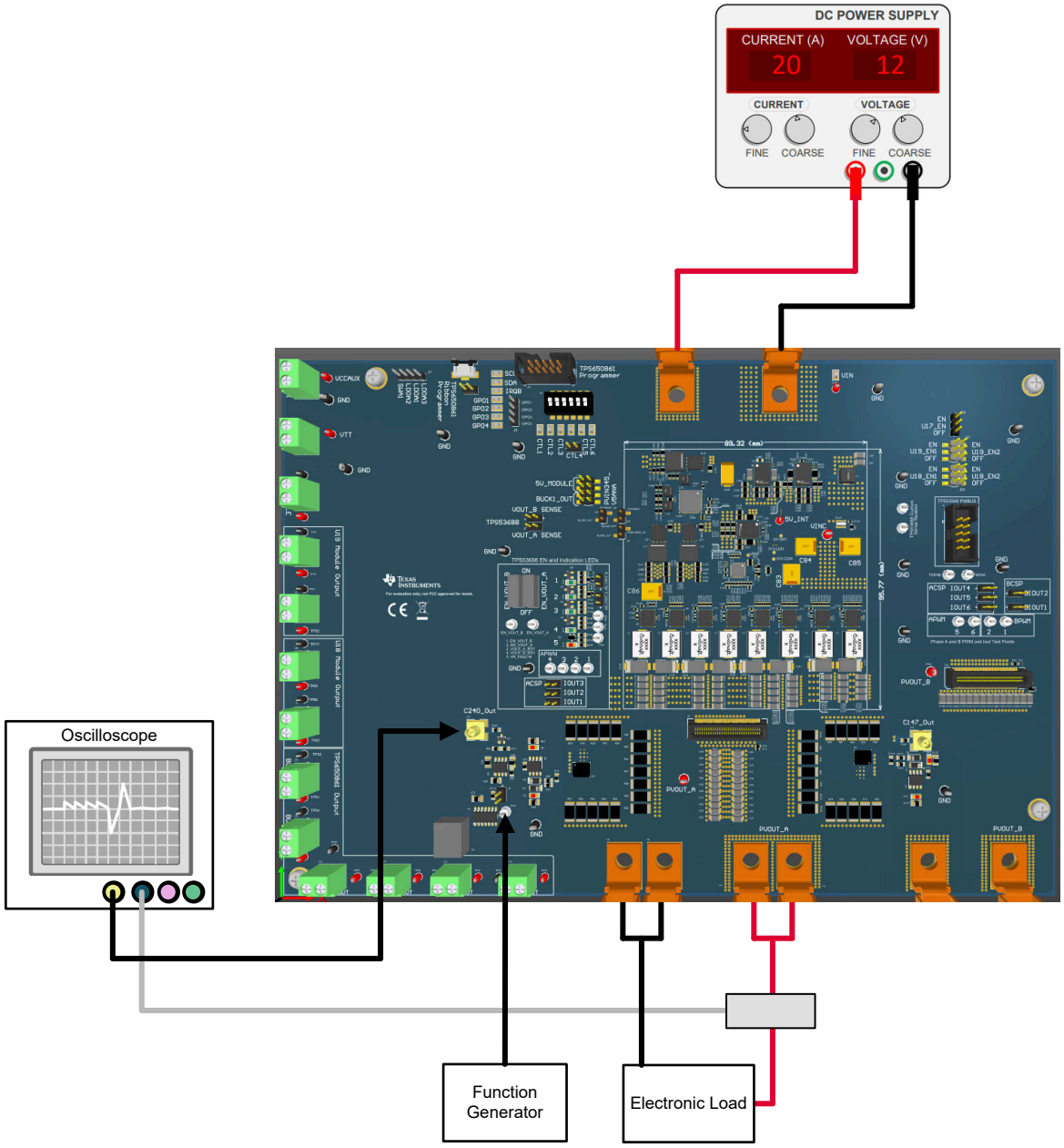


図 3-2. TPS53688 Transient Test Setup

To test the transient performance of the TPS53688, the following equipment is needed to test both phase A and phase B:

- Power supply capable of high current to test the full capability of the 180 A on phase A of the TPS53688 and the 60 A on phase B
- Electronic load set the current levels of the transient
- Function generator to provide the switching waveform to the onboard load transient circuit
- Oscilloscope to measure the load step and probe the voltage across the output capacitor to measure the transient performance. Voltage measurements across the output capacitor can be take directly from J11 (for phase A) and J12 (for phase B).

3.2.3 TPS650861 Programming Setup

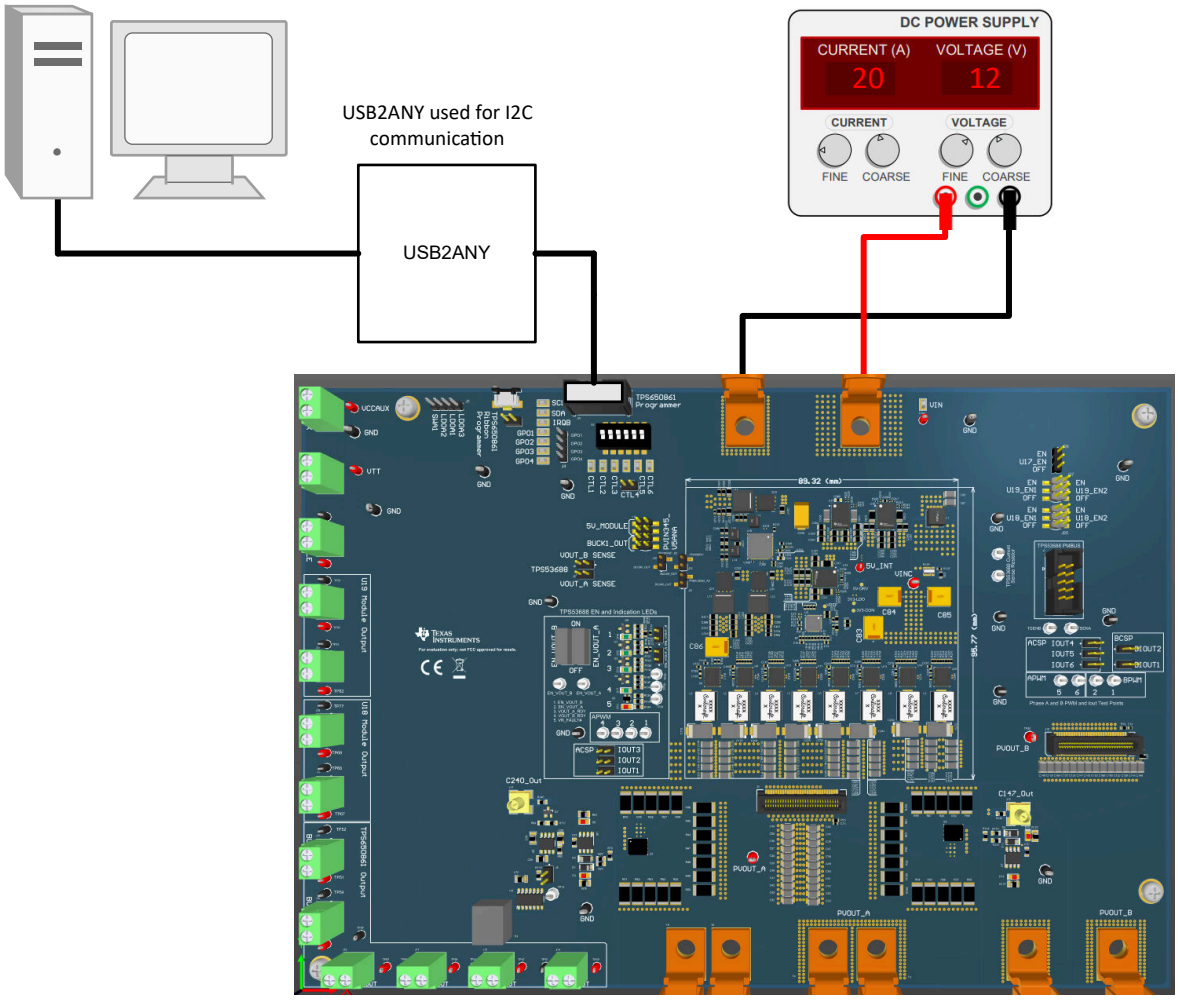


図 3-3. TPS650861 USB2ANY Setup

The TPS650861 requires a USB2ANY and the IPG-UI GUI to interface, and modify the TPS650861 voltage outputs and sequencing. For more information on how to use the IPG-UI GUI and how to program the TPS650862 see the *TPS65086100 Non-Volatile Memory Programming Guide*.

3.2.4 TPS650861 and TPSM5D1806 Transient Test Setup

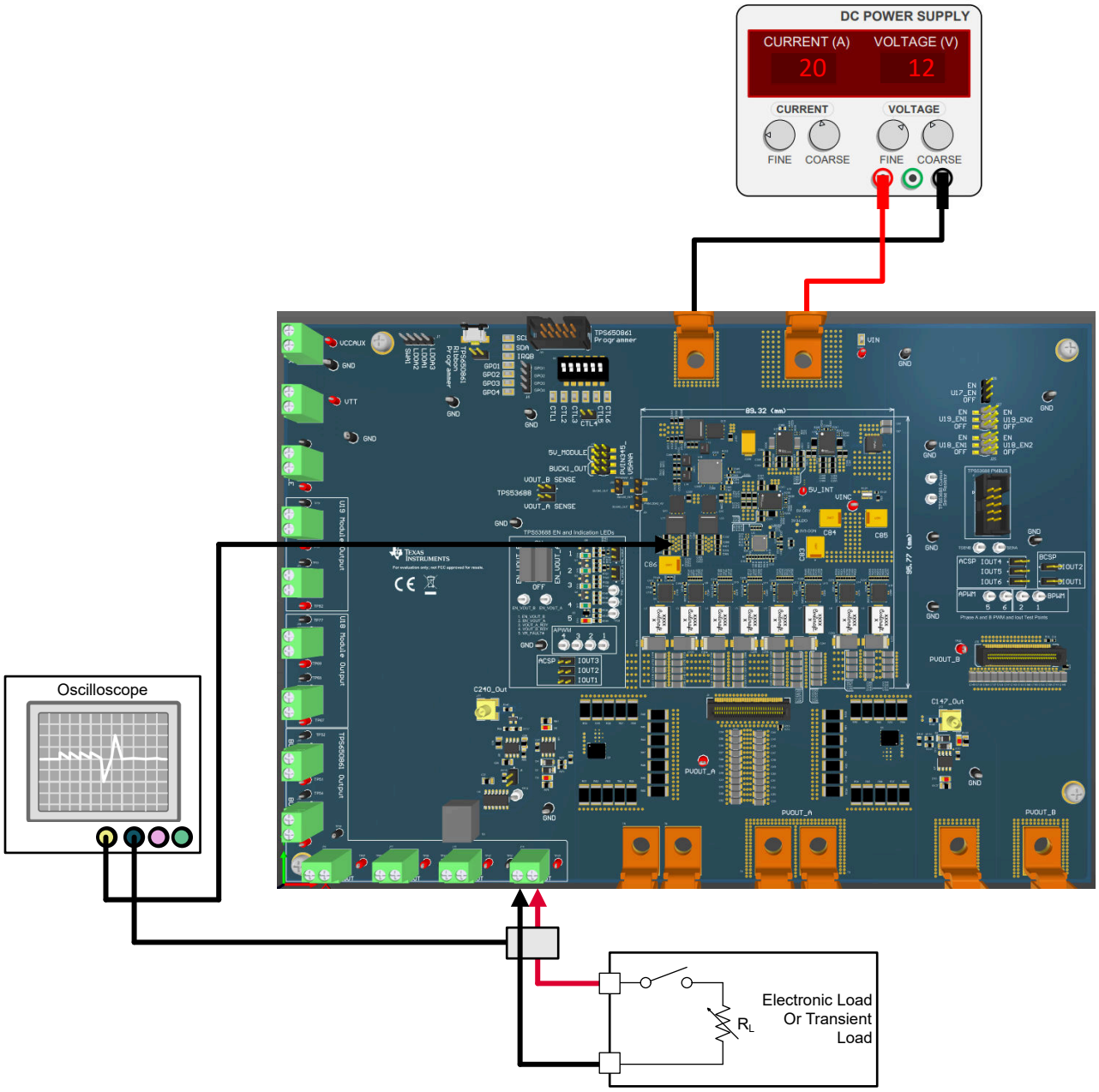


図 3-4. TPS650861 and TPSM5D1806 Transient Test Setup

To test the capability of the TPS650861 and TPSM5D1806 devices, the following equipment is needed:

- Electronic load to provide the current load and provide the transient step
  - Another option is to use a load slammer circuit and use the electronic load to provide the baseline current and use the load slammer circuit to switch between the two currents
- Oscilloscope to measure the current of the transient and then another to measure the voltage across the capacitor to measure the transient capability of the converter

3.3 Test Results

3.3.1 Efficiency Results

Efficiency graphs are shown in the following images.

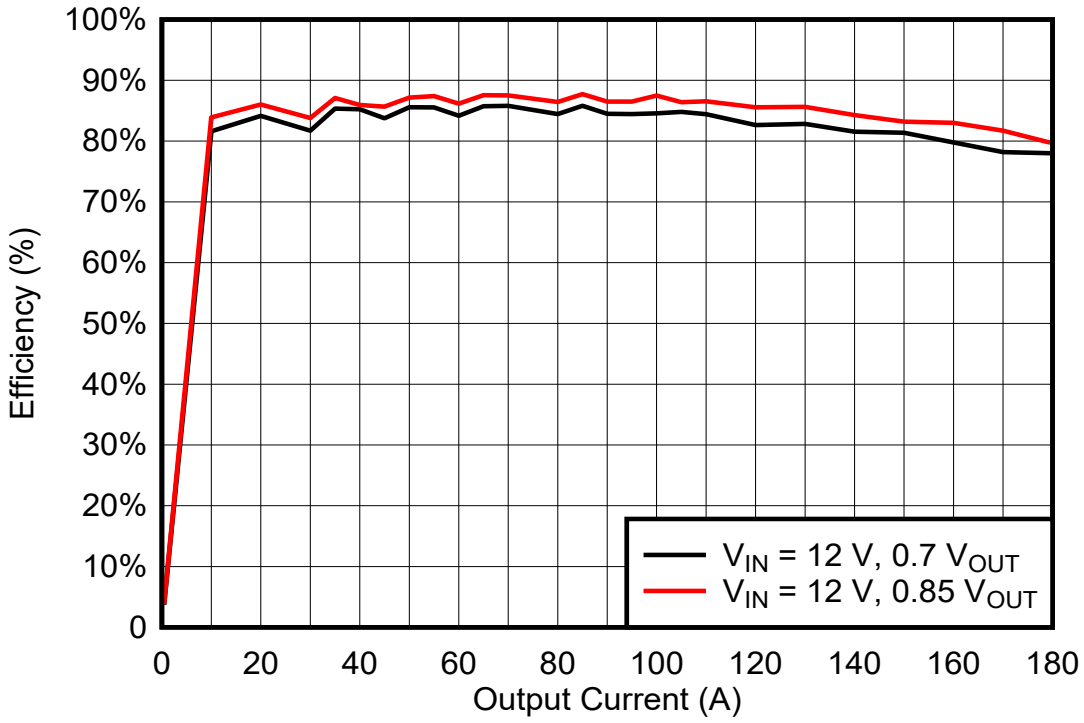


図 3-5. TPS53688 Phase A Efficiency

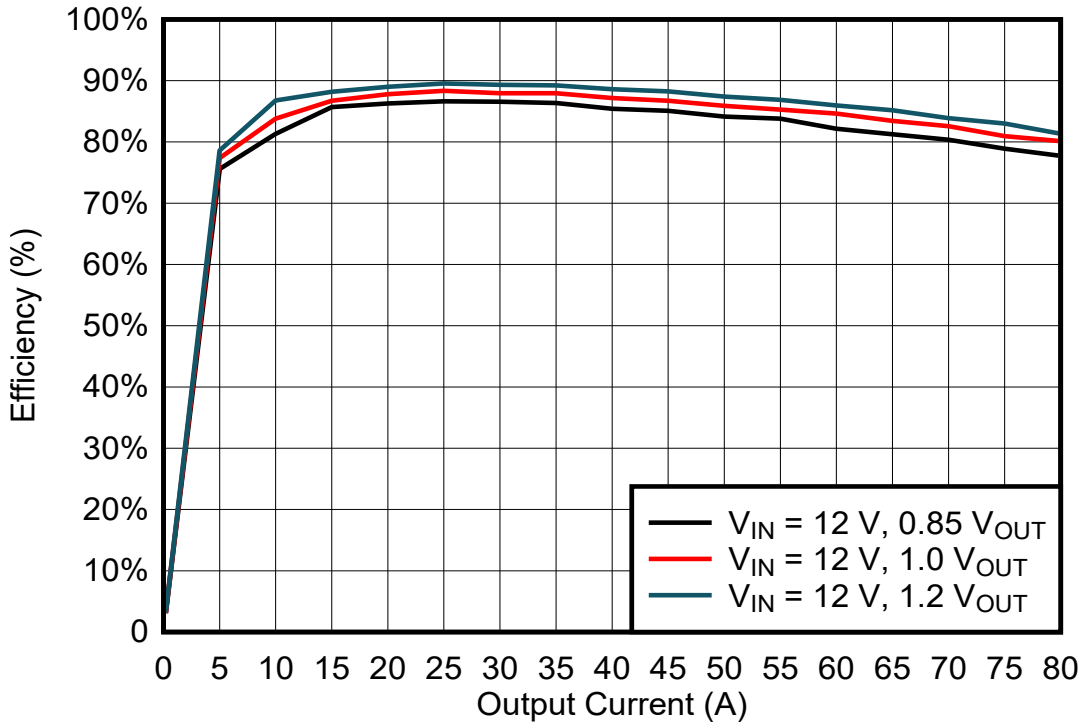


図 3-6. TPS53688 Phase B Efficiency

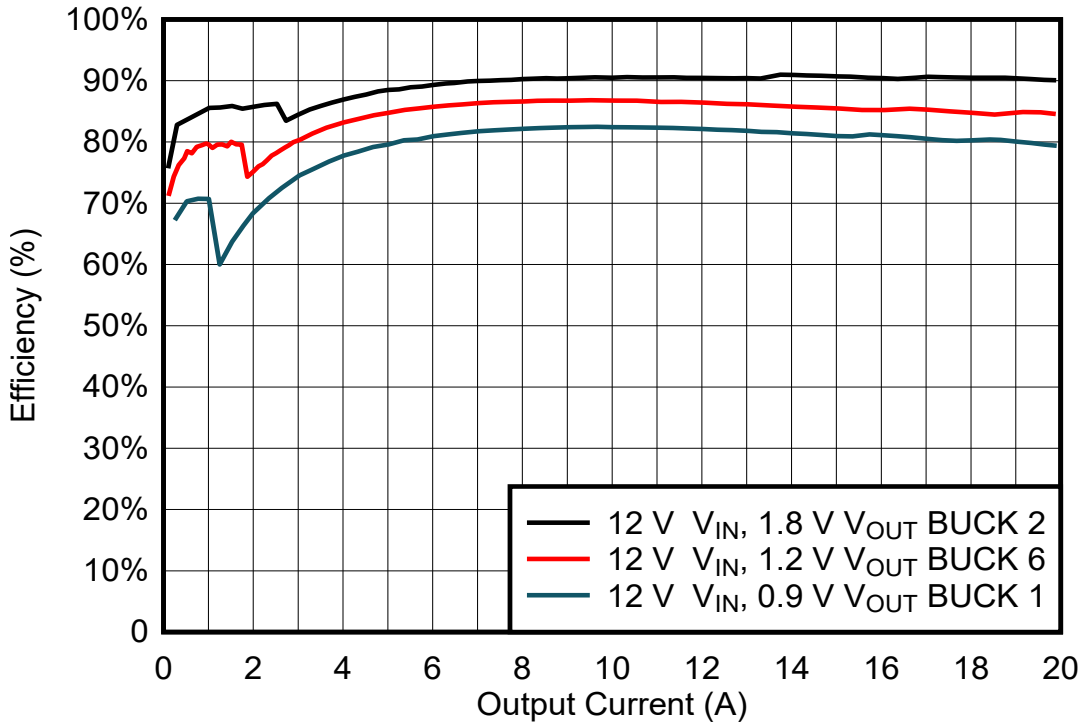


図 3-7. TPS650861 Buck Controller Efficiency

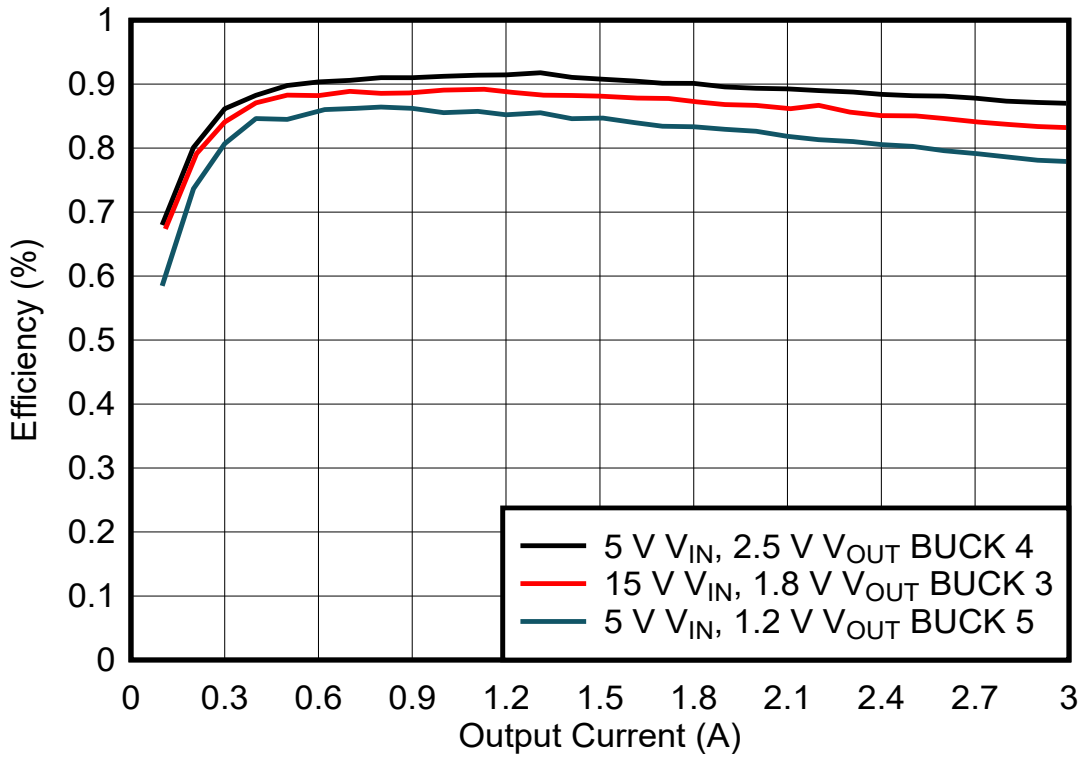


図 3-8. TPS650861 Buck Converter Efficiency

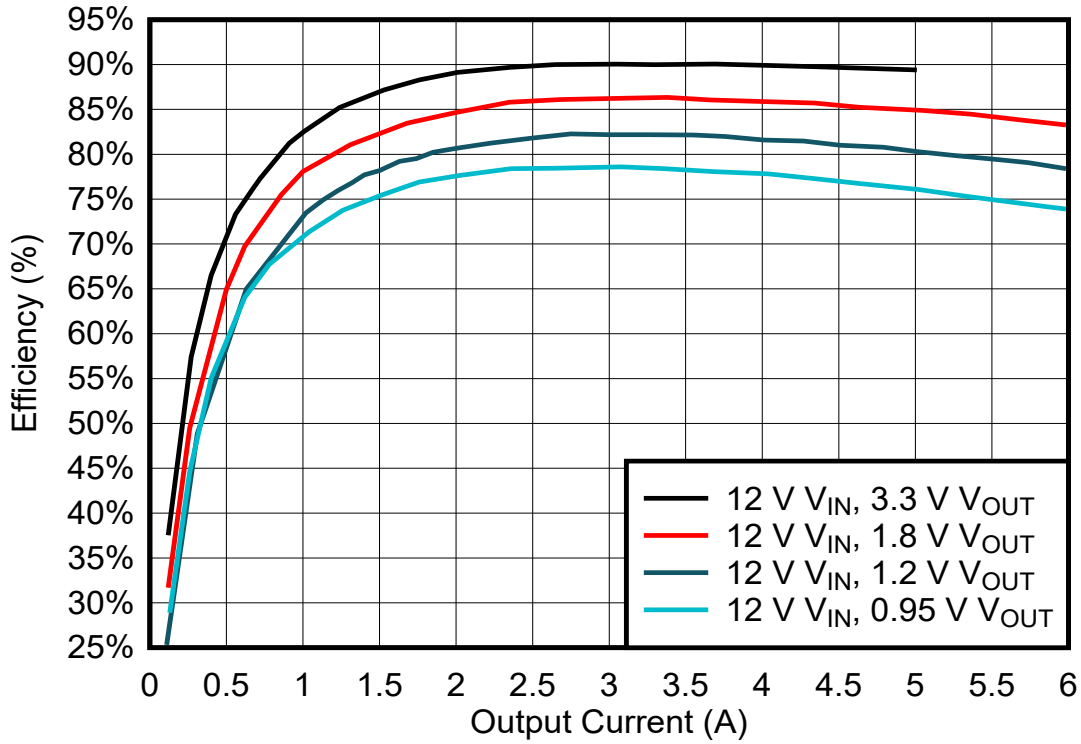


図 3-9. TPSM5D1806 Multi-output Efficiency

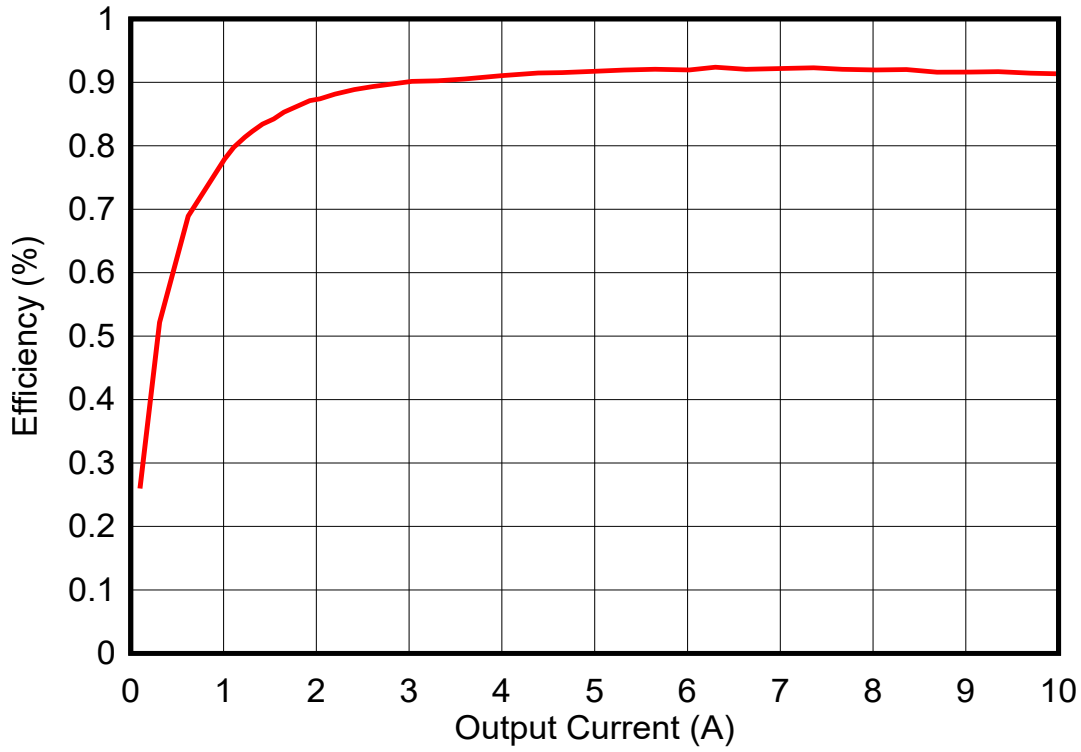


図 3-10. TPSM5D1806 Single-Output Efficiency 5-V Output

3.3.2 Transient Results

3.3.2.1 TPS53688 Transient Results

The following images show the TPS53688 transient waveforms.

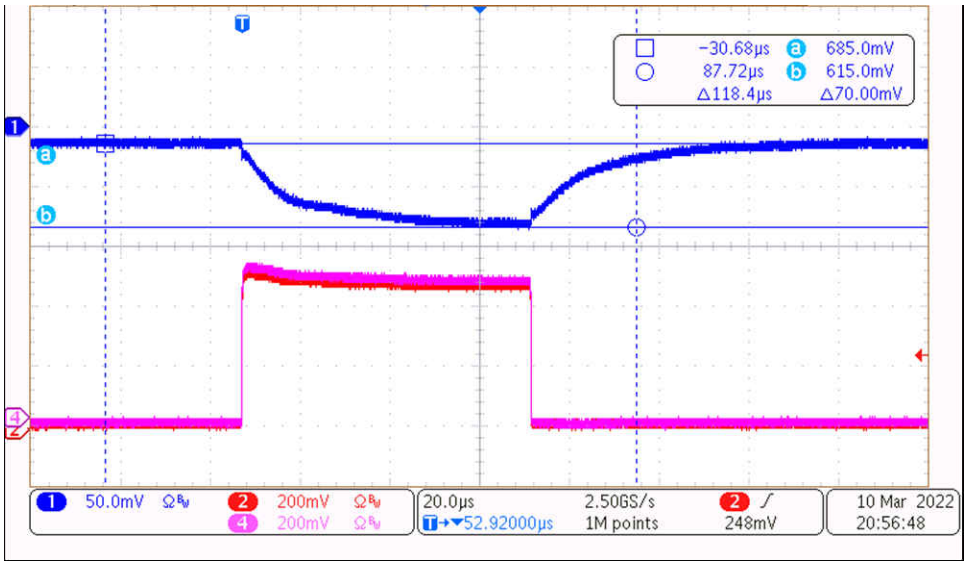


図 3-11. TPS53688 Phase A Transient 0.7 V, 145 A

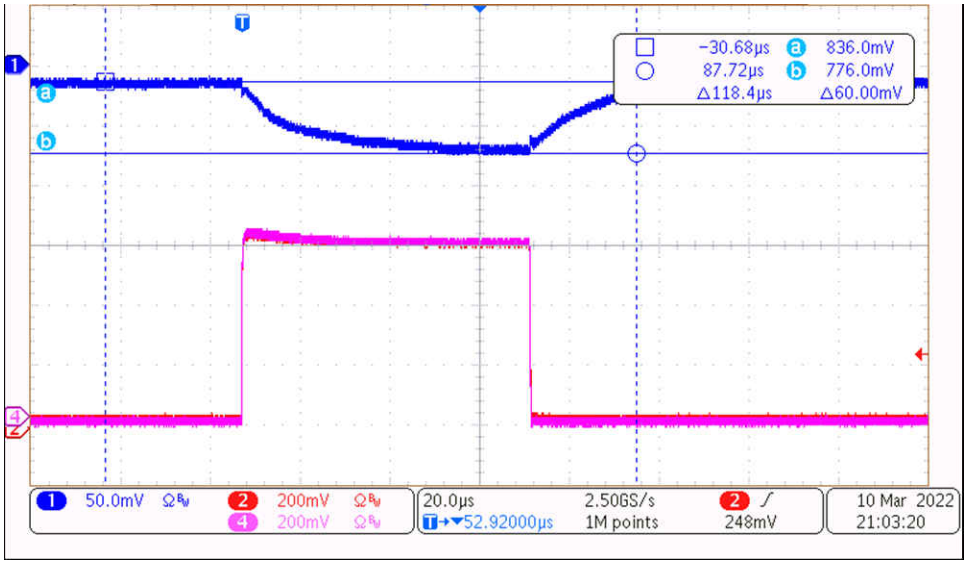


図 3-12. TPS53688 Phase A Transient 0.85 V, 120 A

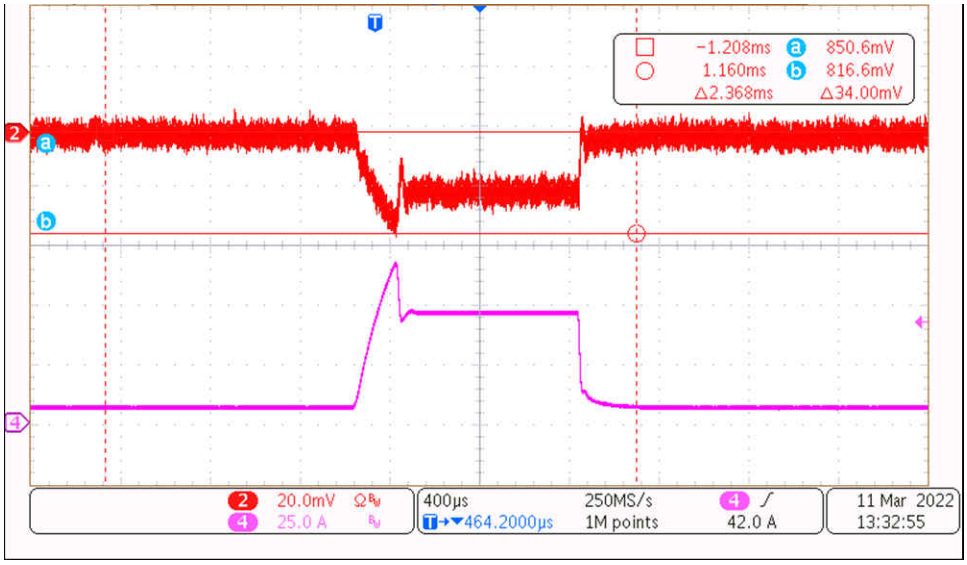


図 3-13. TPS53688 Phase B Transient 0.85 V, 45 A

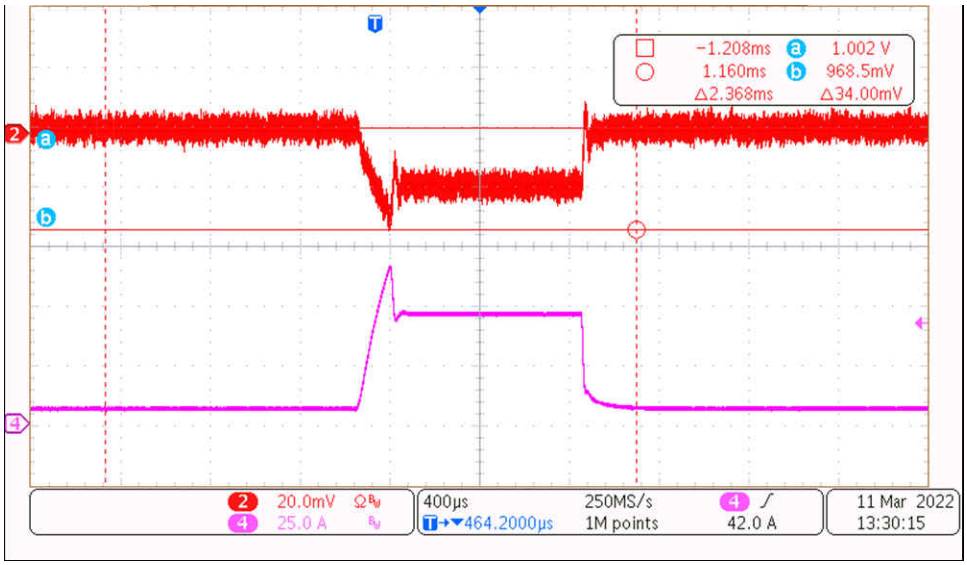


図 3-14. TPS53688 Phase B Transient 1 V, 45 A

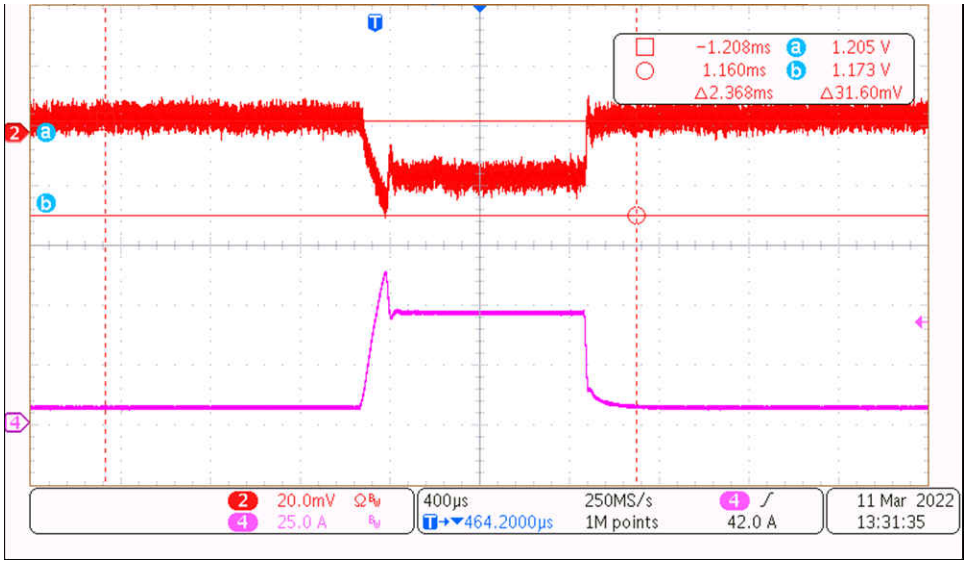


図 3-15. TPS53688 Phase B Transient 1.2 V, 45 A

3.3.2.2 TPS650861 Transient Results

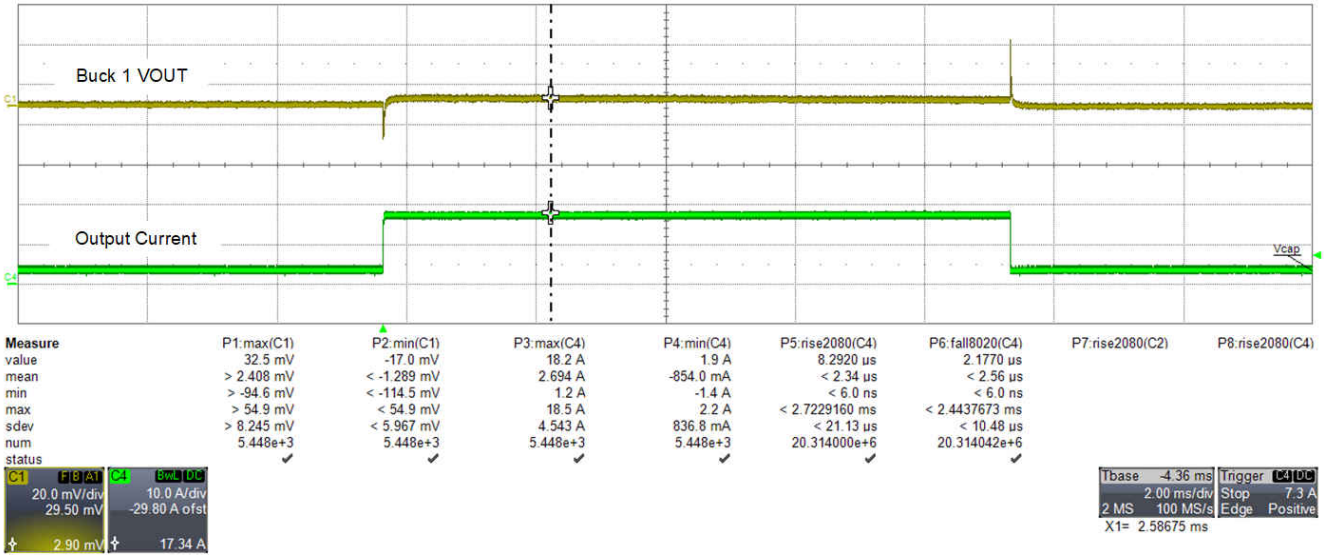


図 3-16. TPS650861 Buck 1 Transient 0.9 V, 20 A

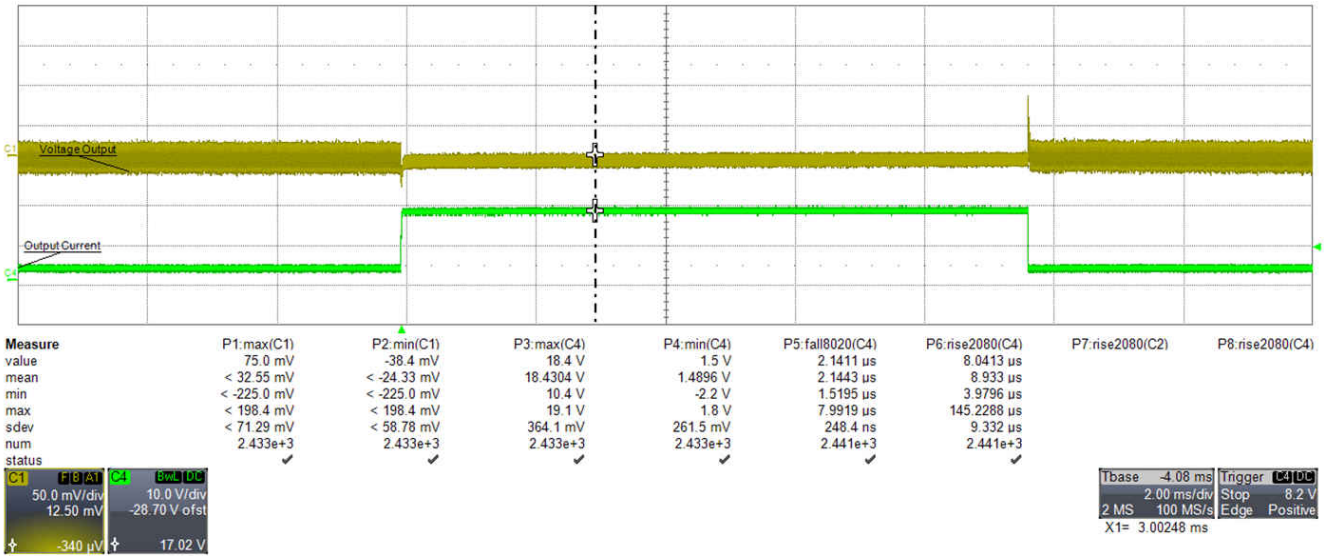


図 3-17. TPS650861 Buck 2 Transient 1.8 V, 20 A

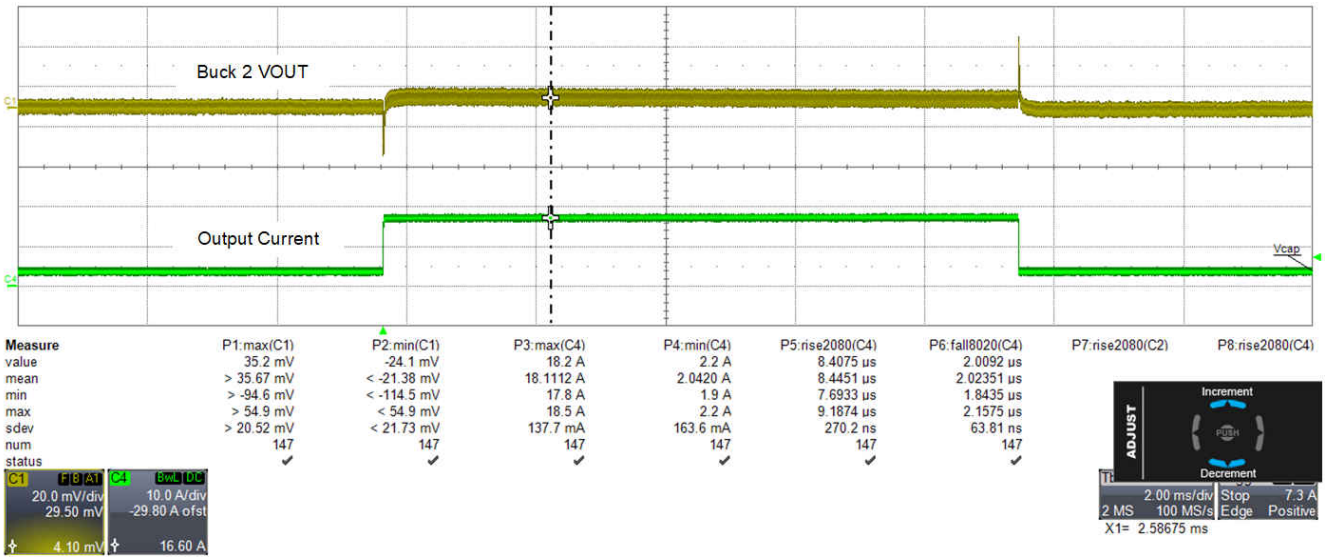


図 3-18. TPS650861 Buck 6 Transient 1.2 V, 20 A

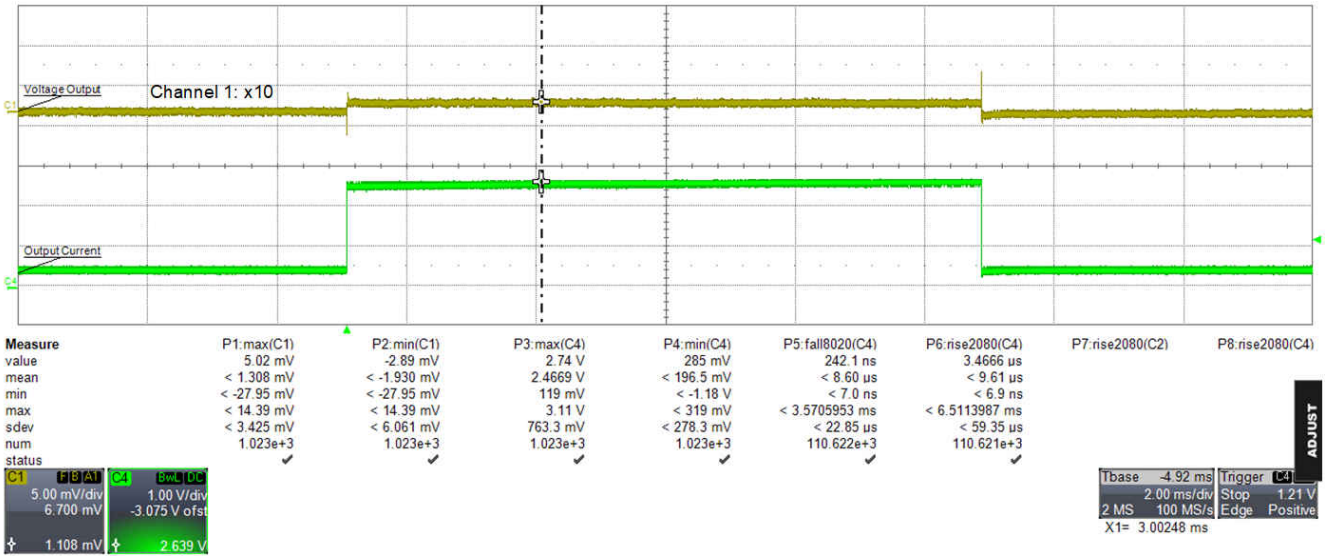


図 3-19. TPS650861 Buck 3 Transient 1.8 V, 3 A

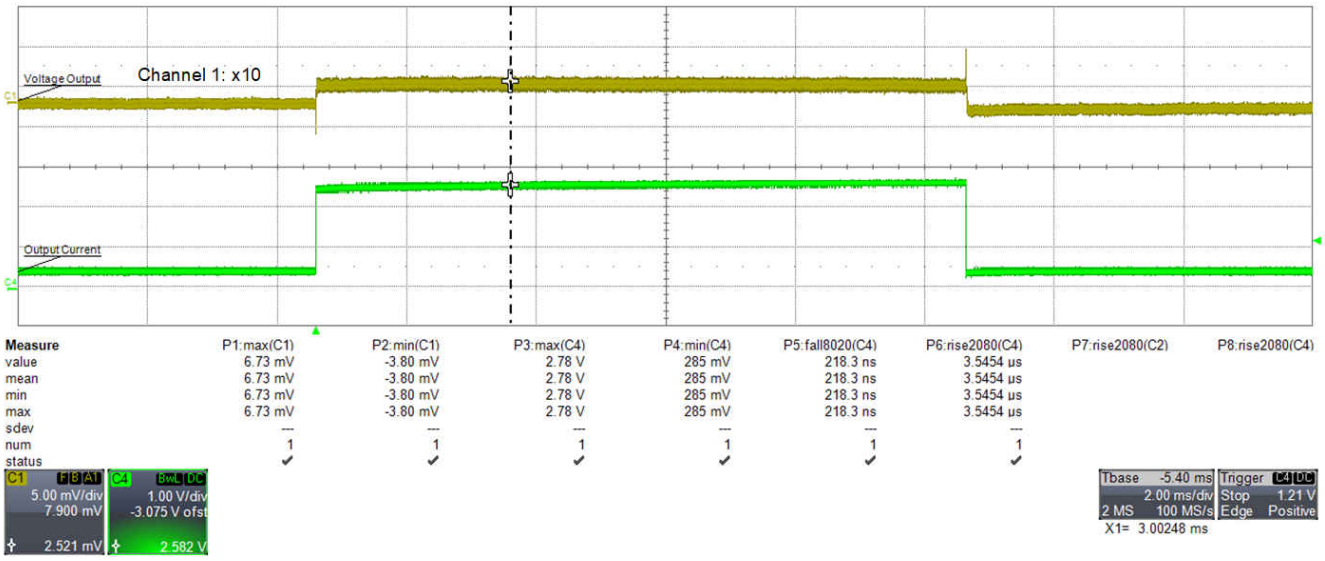


図 3-20. TPS650861 Buck 4 Transient 2.5 V, 3 A

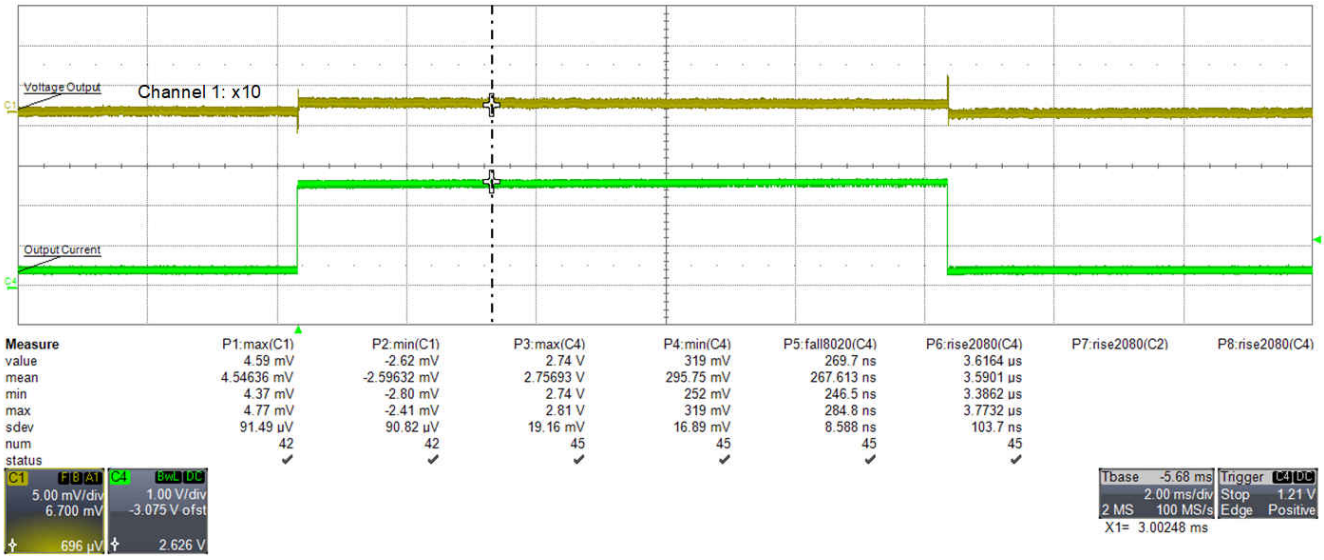


図 3-21. TPS650861 Buck 5 Transient 1.2 V, 3 A

3.3.2.3 TPSM5D1806 Transient Results

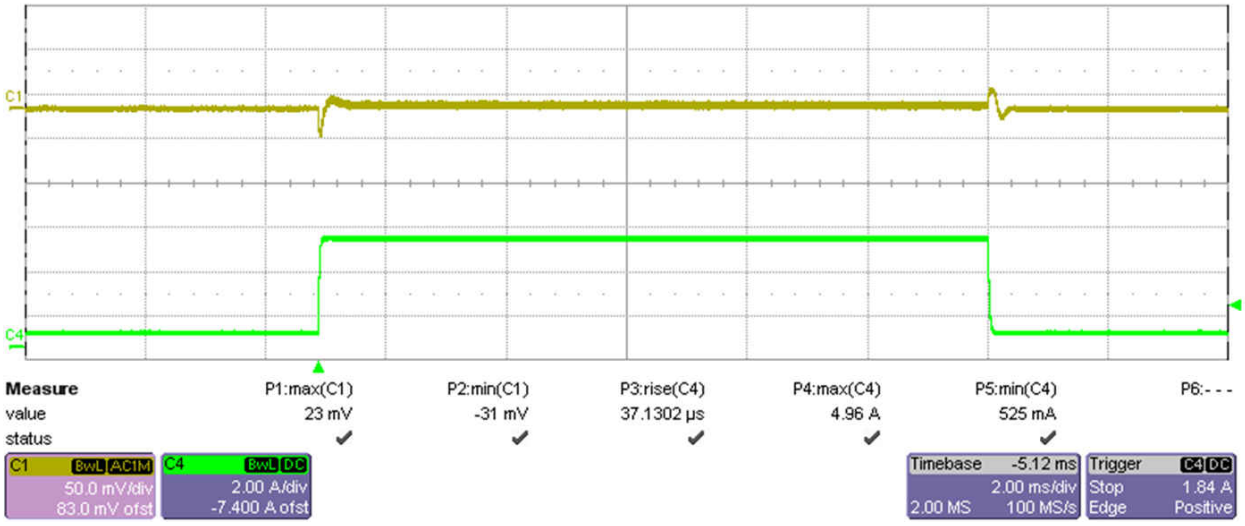


図 3-22. TPSM5D1806 Transient 0.9 V, 6 A

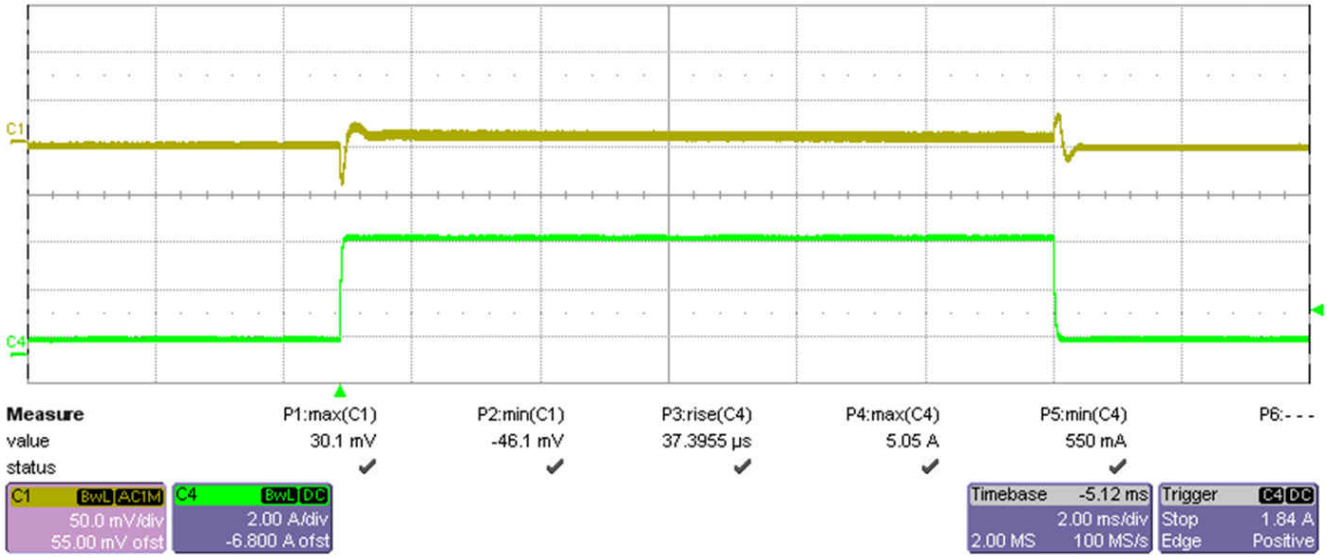


図 3-23. TPSM5D1806 Transient 1.2 V, 6 A

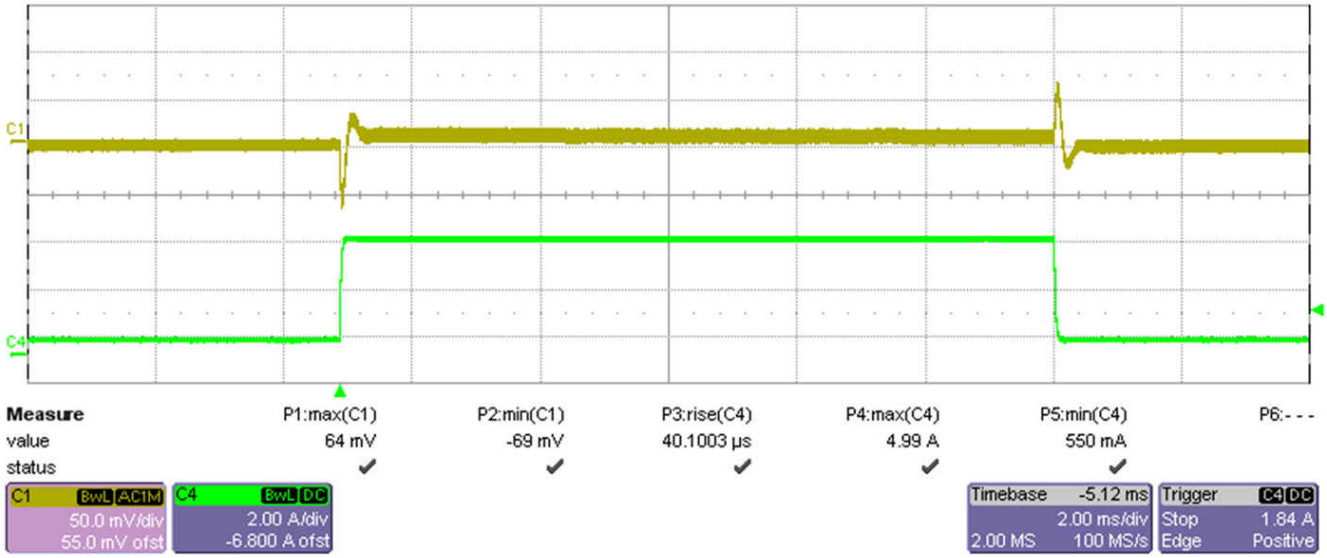


図 3-24. TPSM5D1806 Transient 1.8 V, 6 A

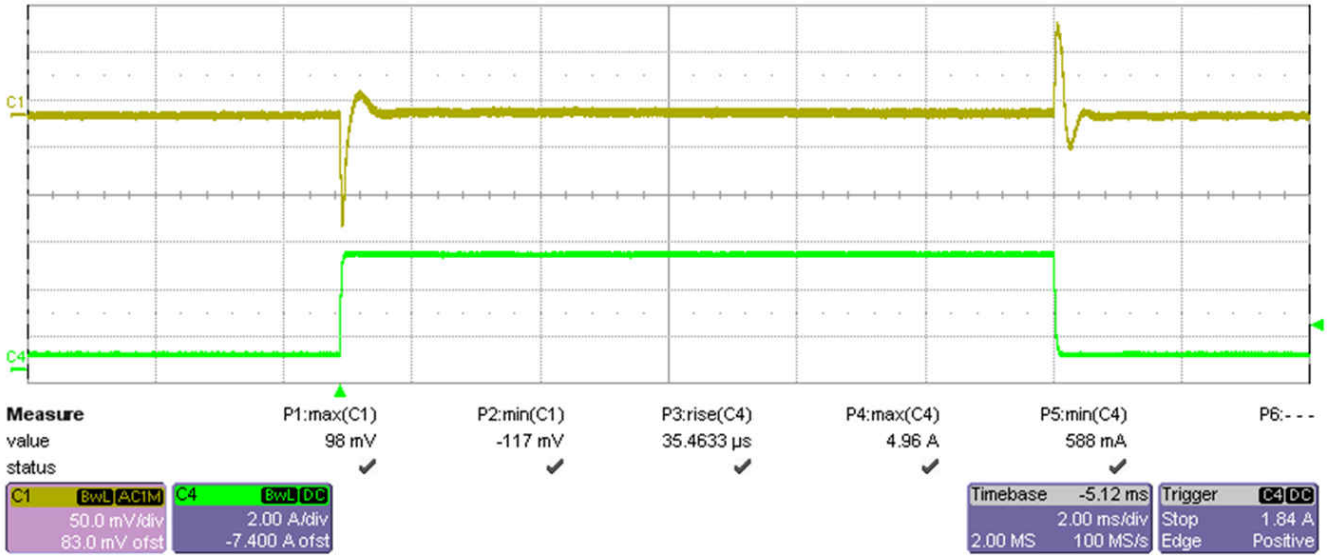


図 3-25. TPSM5D1806 Transient 3.3 V, 5 A

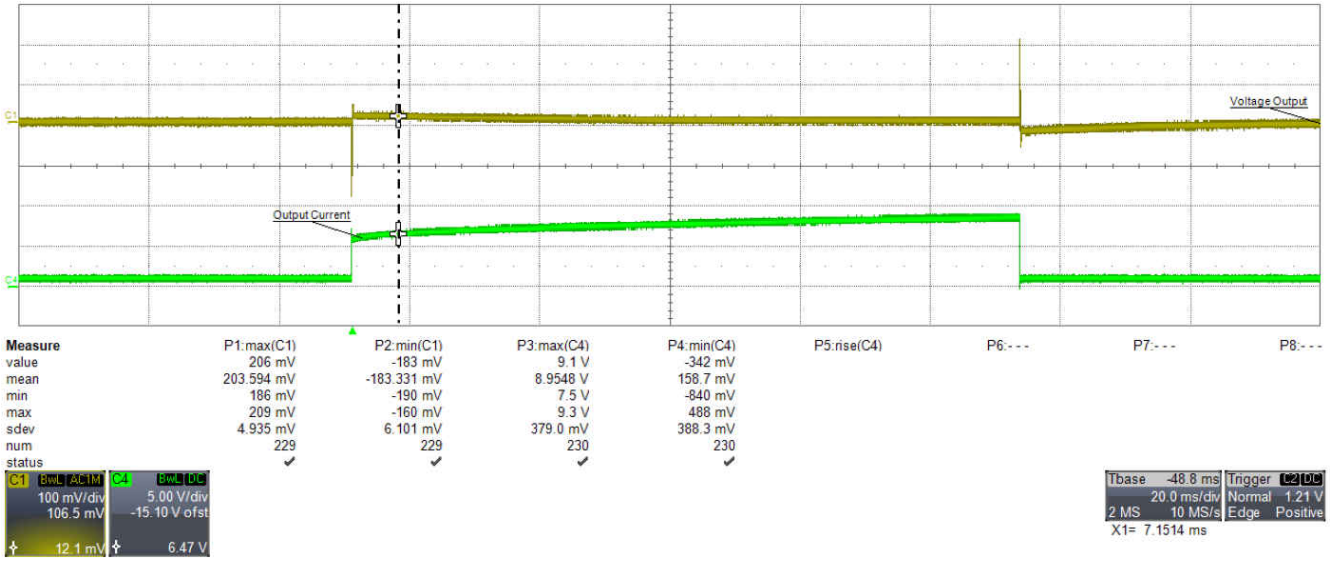


図 3-26. TPSM5D1806 Transient 5 V, 10 A

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010241.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010241.

4.2 Tools and Software

Tools

USB2ANY	Interface adapter to interface with the TPS650861
USB-TO-GPIO	Interface adapter to interface with the TPS53688

Software

IPG-UI GUI	Software to interface with the TPS650861
FUSION_DIGITAL_POWER_DESIGNER	Software to interface with TPS53688

4.3 Documentation Support

1. Texas Instruments, *TPS53688 Dual-Channel, 8-phase step-down, digital multiphase D-CAP+™ controller with VR13.HC SVID and PMBus* product page
2. Texas Instruments, *CSD95410RRB 90-A peak continuous synchronous buck NexFET™ smart power stage* product page
3. Texas Instruments, *TPS650861 Programmable Multirail PMU for Multicore Processors, FPGAs, and Systems* data sheet
4. Texas Instruments, *TPSM5D1806 4.5-V to 15-V Input, Dual 6-A / Single 12-A Output Power Module* data sheet
5. Texas Instruments, *TPS65086100 Non-Volatile Memory Programming Guide*

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5 About the Author

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