参考資料

Design Guide: TIDA-010239

AC レベル 2 充電器プラットフォームのリファレンス・デザイン

概要

電気自動車サービス機器 (EVSE) を使用すると、グリッドから電気自動車に電力を安全に供給できます。EVSE 制御システムは、補助電力段、オフボードの AC/DC 高電力段 (DC 充電ステーションのみ)、電力量計ユニット、AC および DC 残留電流検出器、絶縁監視ユニット、ドライバ付きリレーおよびコンタクタ、単線による双方向通信、サービスおよびユーザー・インターフェイスで構成されます。このリファレンス・デザインは、コンバータとリニア・レギュレータに接続する超低スタンバイ電力の絶縁型 AC/DC 補助電力段、IEC61851 規格に適合するためのコンパレータ・ベースの制御パイロット・インターフェイス、効率的なリレーとコンタクタの駆動、プラグ・ロック・モーター駆動、RCD アプリケーションの AC/DC 電流を検出するフラックス・ゲート回路、リレー / コンタクタ両端の絶縁型ライン電圧検出を特長としています。

リソース

TIDA-010239	デザイン・フォルダ
UCC28742、TLV1805	プロダクト・フォルダ
ISO1212、DRV8220	プロダクト・フォルダ
ADC122S051	プロダクト・フォルダ
TPS7A39、TPS7A20、ATL431、TL431	プロダクト・フォルダ
TPS563210A、TPS55330	プロダクト・フォルダ
TPS259470、TL7705A	プロダクト・フォルダ

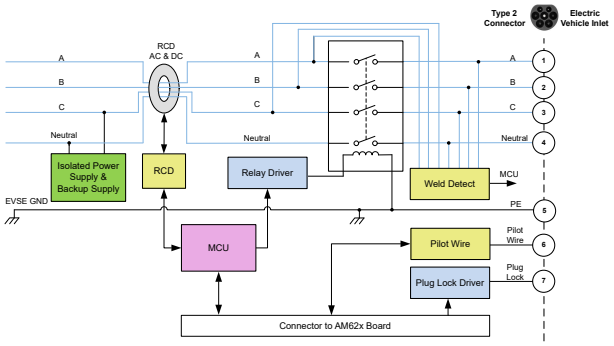
テキサス・インスツルメンツの TI E2E™ サポート・エキスパートにお問い合わせください。

特長

- 超低スタンバイ UCC28742 ベースの絶縁型 29W AC/DC 段により、エネルギー効率が向上します
- エネルギー・ストレージの解放中に最大 7.5W を 3 秒間供給するスーパーキャパシタ・バックアップ (AC 電源障害)
- 制御パイロット・インターフェイス用の低ドロップアウト (LDO) の厳格な出力電圧レギュレーション (±5% 未満) と TLV1805 デバイスの高いスルー・レート
- コスト最適化された超低スタンバイ電力のコンバータおよびリニア・レギュレータにより、ポイント・オブ・ロードに電力を供給
- 熱保護、RCD AC および DC 検出、プラグ・ロック制御のための大電流リレーおよびコンタクタを駆動する DRV8220 電流コントローラ
- ISO1212 デジタル入力レシーバを使用した絶縁型ライン電圧センシングにより、リレーとコンタクタの接点溶着を検出

アプリケーション

- AC 充電 (パイル) ステーション



1 System Description

Electric vehicles (EVs), including plug-in hybrid electric vehicles (PHEVs), receive energy from the electrical grid through electric vehicle supply equipment (EVSE), more commonly known as EV chargers. To facilitate the power delivery to the vehicle, the EVSE sits between a stable grid connection and the vehicle as shown in 図 1-1.

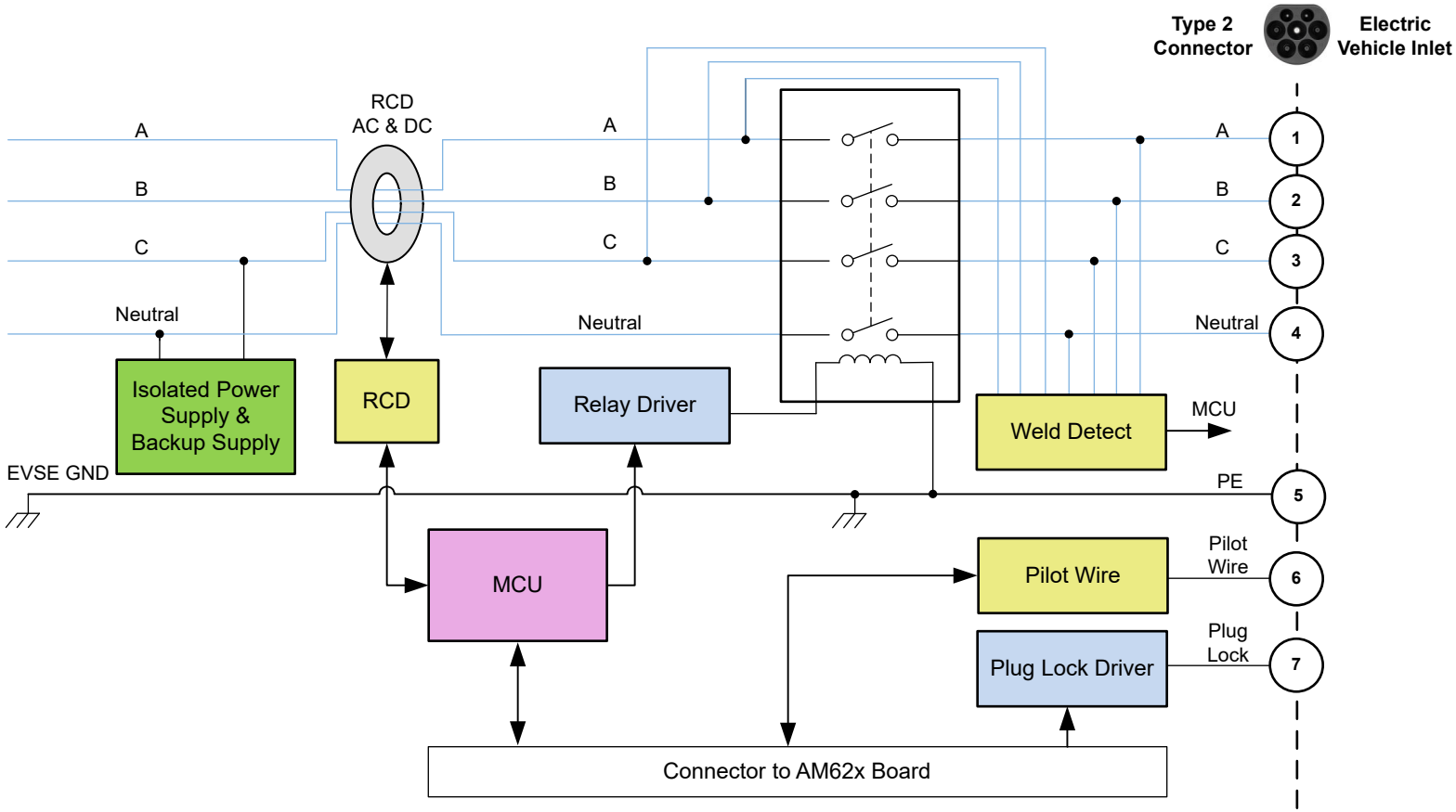


図 1-1. AC Level 2 Charger High-Level Block Diagram

The primary EVSE functionality includes:

- Regulated electrical current - makes sure that the best possible current is provided and falls within the maximum current the EV can handle.
- AC/DC residual current detection (RCD)
- Relay and contactor drive and latched contact detection
- Energy metering
- Automatic disconnect - when a hardware fault is detected, the power is shut off, to avoid risks like battery damage, an electrical short, or a fire.
- Safety lock-out feature - prevents current from flowing when the charger is not connected to an EV.

An EVSE control system mainly consists of auxiliary power stage, off-board AC/DC high power stage (only in DC charging stations), energy metering, AC and DC residual current detection, isolation monitor unit, relays and contactors with drive, two-way communication, and service and user interfaces.

1.1 EV Charging Station Challenges

The EVSE design for EV charging stations presents several challenges including those presented in the following sections.

1.1.1 SAE J1772 or Equivalent Standard Compliant EV Charging Stations

Many electric vehicle manufacturers have adopted the SAE J1772 standard for electrical connections to an EV. The same specifications also translate into international localizations, with differing form factors. The control pilot is the primary control conductor and is connected to the equipment ground through control circuitry on the vehicle and performs the following functions:

- Verifies that the vehicle is present and connected
- Permits energization and de-energization of the supply
- Transmits supply equipment current rating to the vehicle
- Monitors the presence of the equipment ground
- Establishes vehicle ventilation requirements

表 1-1 shows the SAE J1772 standard mandates control pilot circuit generator parameters.

表 1-1. Control Pilot Signal Generator Parameters per SAE J1772

PARAMETER(1)	MIN	NOM	MAX	UNITS
Voltage high, open circuit	11.40	12.00	12.60	V
Voltage low, open circuit	–11.40	–12.00	–12.60	V
Frequency		1000		Hz
Pulse width(2)		5		µs
Rise time(3)		2		µs
Fall time(3)		2		µs
Settling time(4)		3		µs

(1) Tolerances to be maintained over the environmental conditions and useful life as specified by the manufacturer
(2) Measured at 50% points of complete negative-to-positive or positive-to-negative transitions
(3) 10% to 90% of complete negative-to-positive transition or 90% to 10% of complete positive-to-negative transition measured between the pulse generator output and R1. Note that the term *generator* refers to the EVSE circuitry prior to and driving the 1-kΩ source resistor with a ±12-V square wave. This circuitry must have rise and fall times faster than 2 µs. Rise and fall times slower than 2 µs begin to add noticeably to the output rise and fall times dictated by the 1-kΩ resistor and all the capacitance on the pilot line.
(4) To 95% of steady-state value, measured from the start of transition

1.1.2 AC and DC Leakage, Residual Current Detection (RCD)

The primary requirement in providing protection during EV charging is the ability to detect AC and DC residual currents and thereby mitigate the risk of electric shock or fire.

1.1.3 Efficient Relay and Contactor Drive

In normal use cases, high-current relays or contactors can typically draw 10s to 100s of milliamps as an inductive load, requiring specific drive architectures. Because of the amount of time that a relay or contactor requires to remain powered, an efficient drive solution is preferred to avoid thermal problems.

1.1.4 Contact Weld Detection

For safety reasons, detecting the output voltage of the relay and contactor is critical. The contacts can experience arcing and become fused together, providing power to the plug even when not powered by the system. Checking that the operation completed correctly is important and is to be done every time the relay is opened.

This reference design showcases ultra-low standby isolated AC/DC auxiliary power stage followed by ultra-low I_Q as well as cost-optimized converters and linear regulators, comparator-based control pilot interface to meet SAE J1772 standard, efficient relay and contactor driver design, and digital isolator based line voltage sensing to detect fusing of relay and contactor contacts due to arcing.

1.2 Key System Specifications

表 1-2. Key System Specifications

PARAMETER	NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT	DETAILS
INPUT CHARACTERISTICS						
Input voltage,V_{IN}		85	120, 230	460	V_{RMS}	Line voltage
Line frequency, f_{LINE}		47	60, 50	63	Hz	
OUTPUT CHARACTERISTICS						
Output voltage, V_{OUT1}	Flyback output 1		12		V	UCC28742-based AC/DC flyback power stage with 3 outputs
Output current, I_{OUT1}			2.2		A	
Output voltage, V_{OUT2}	Flyback output 2		14		V	
Output current, I_{OUT2}			0.1		A	
Output voltage, V_{OUT3}	Flyback output 3		–14		V	
Output current, I_{OUT3}			0.1		A	
Total output power, P_{OUT}	Output power of flyback power stage			28.8	W	
POINT OF LOAD AND AUXILIARY SECTION CHARACTERISTICS						
TPS7A3901	Dual LDO		+12		V	Nominal current = 100 mA
TPS7A3901			–12		V	Nominal current = 100 mA
TPS76318	LDO		+1.8		V	Nominal current = 30 mA
TPS259470	eFuse		+5		V	Overcurrent protection = 4.5 A
TPS563210A	Sync-Buck		+5		V	Nominal current = 1.2 A, 1.3 A max
TPS563210A	Sync-Buck		+3.3		V	Nominal current = 0.8 A, 1.5 A max
TPS65130	Dual converter (Boost + inverting-Buck/Boost)" active during energy storage release		± 14		V	Nominal current = 0.1 A
TPS55330	Non-sync Boost: active during energy storage release		+11.5		V	Nominal current = 1.8 A
SUPERCAPACITOR BACKUP CHARACTERISTICS						
Supercap normal operating voltage	2 × 2.5-µF supercapacitors in series. Charger charges to 7.8 V. Boost UVLO sets min operating voltage to 4.3 V. Supplying 7.5 W for 3 s (after boost) during energy storage release (AC mains failing)	+4.3	+7.8		V	Peak current = 4.06 A, for 1 s from full rate voltage to half voltage.
TL7705A	Voltage supervisor for EoC of 2 × 2.5-µF supercapacitors in series		+7.49		V	Threshold for End of Charge
Linear charger	Charges supercapacitors from 0 V to 7.8 V in 81 s and from 4.3 V to 7.8 V in 36 s		+120		mA	

2 System Overview

2.1 Block Diagram

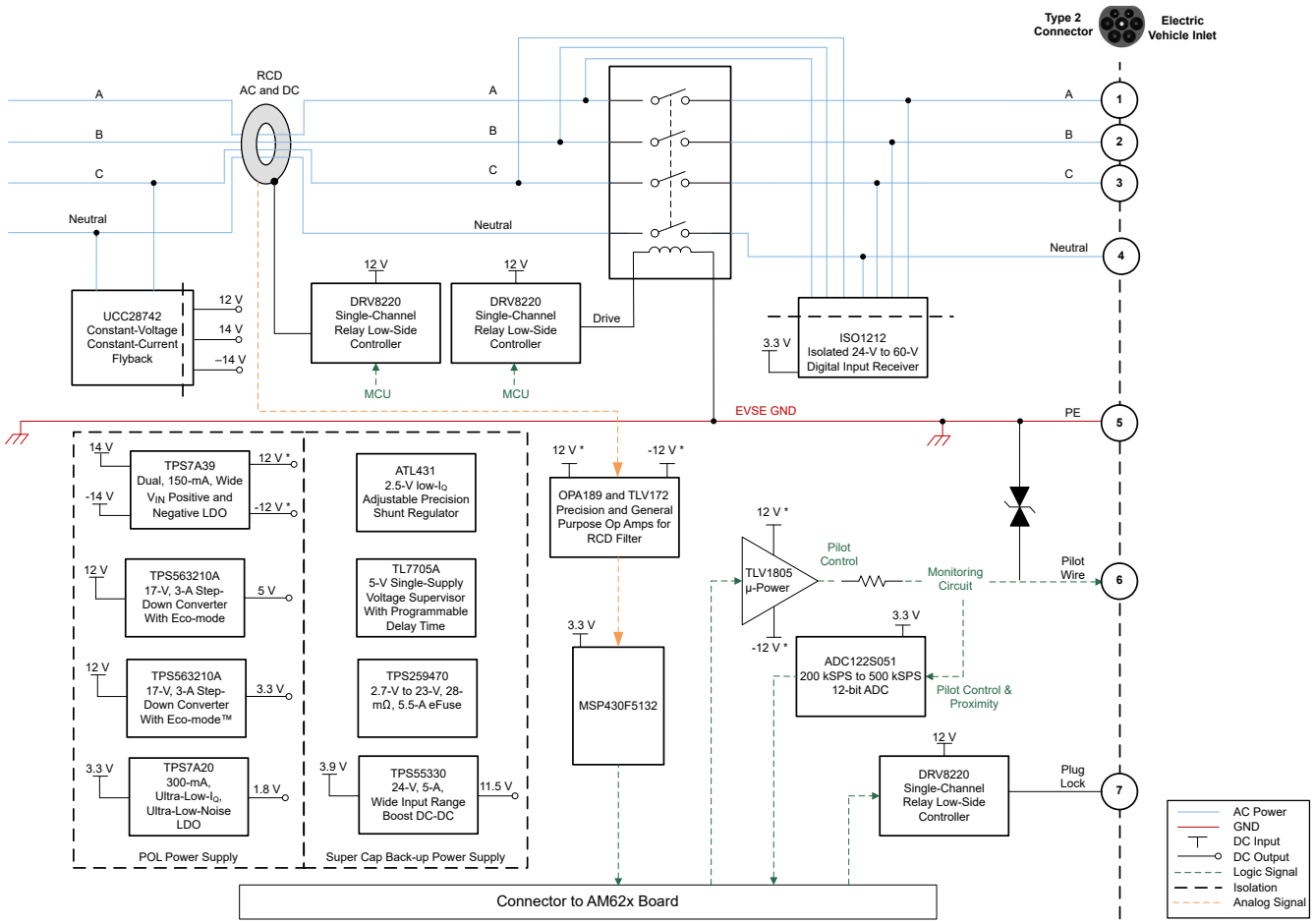


図 2-1. TIDA-010239 Block Diagram

2.2 Design Considerations

2.2.1 Isolated AC/DC Power Supply Design

The isolated AC/DC power stage is multiple outputs winding flyback stage based on the UCC28742 device. The UCC28742 controller provides constant-voltage (CV) using an optical coupler to improve transient response to large-load steps. Constant-current (CC) regulation is accomplished through primary-side regulation (PSR) techniques. This device processes information from the optocoupled feedback and an auxiliary flyback winding for precise high-performance control of the output voltage and current. 図 2-2 shows the system block diagram for the power supply design and the design parameters are shown in 表 2-1.

These are the main components of the power supply:

- A three-phase input flyback with synchronous rectification supplies three voltages: 12 V (power) and ± 14 V (low power)
- Two buck converters (based on TPS563210), one dual-LDO (TPS7A3901) and a second LDO (TPS7A2018) take the power from the flyback and supply further 5 V, 3.3 V, 1.8 V, and ± 12 V
- Two supercapacitors, 2.5 µF each are connected in series and are charged by means of a 120-mA constant current linear regulator, setting the charging voltage to 7.8 V
- A boost converter with TPS55330 supplies all voltages as soon as mains power is missing
- A further 12-V input port, protected against overcurrent and reverse polarity, is managed by the eFuse TPS259470, useful during debug. This way the whole system can be supplied without the need of single or three-phase high-voltage input
- An inverting buck-boost generates ±14 V for the dual-LDO during energy storage discharge, taking power from the regulated 5-V rail

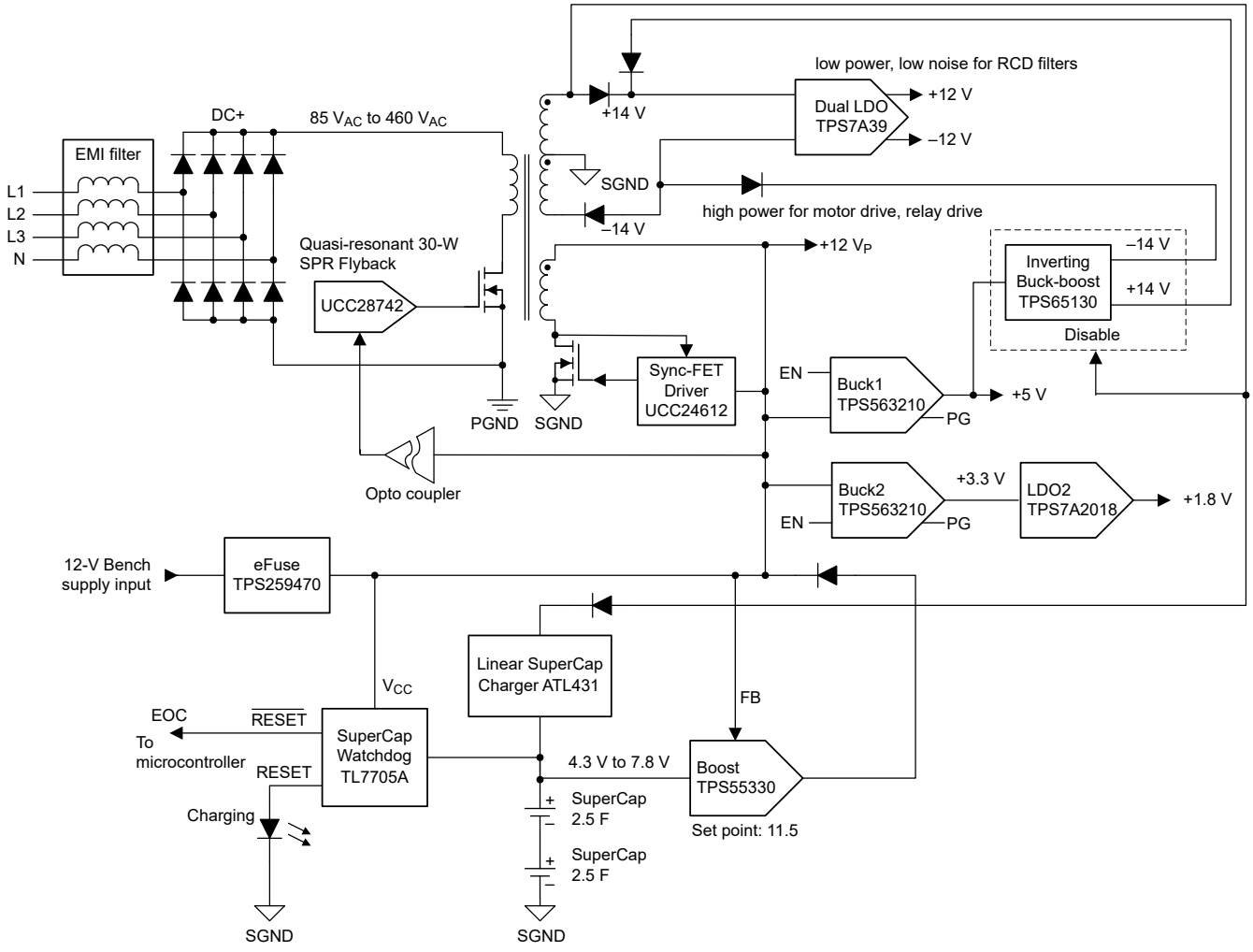


図 2-2. Isolated AC/DC Power Supply Block Diagram

表 2-1. Design Parameters

PARAMETER	NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS					
Input voltage,V_{IN}		85	115, 230	460	V_{RMS}
Maximum input current	$V_{IN} = V_{IN(min)}$, $I_{OUT} = I_{OUT(max)}$		0.8		A_{RMS}
Line frequency		47	60, 50	63	Hz
Desired capacitor bulk voltage, $V_{BULK(desired)}$		85			V
No load input power consumption	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, I_{OUT} = 0 A			500	mW
OUTPUT CHARACTERISTICS					
Output voltage, V_{OUT1}	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$	11.4	12	12.6	V
Output current, I_{OUT1}				2.2	A
Output voltage, V_{OUT2}	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$	10.5	12	12.1	V
Output current, I_{OUT2}				0.1	A
Output voltage, V_{OUT3}	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$	–10.5	–12	–12.1	V
Output current, I_{OUT3}				0.1	A
Total output power, P_{OUT}				28.8	W
Output voltage regulation	Line regulation: $V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, $I_{OUT1} \le I_{OUT1(max)}$		0.1%		
	Load regulation: 0 A $\le I_{OUT1} \le I_{OUT1(max)}$		0.2%		
Output voltage ripple	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, 0 A $\le I_{OUT1} \le I_{OUT1(max)}$			100	mVpp
Total output overcurrent, I_{OCC}	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$			2.4	A
Minimum output voltage, CC mode	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, $I_{OUT} = I_{OCC}$		5		V
Brown-out protection	$I_{OUT} = I_{OUT(max)}$	49.9	55.9	61.8	V_{RMS}
Transient response overshoot	$I_{OUT} = I_{OUT(max)}$ to 0-A load transient			0.2	V
Transient response time	$I_{OUT} = I_{OUT(max)}$ to 0-A load transient			5	ms
SYSTEMS CHARACTERISTICS					
Switching frequency, f_{SW}		1.2		40	kHz
Average efficiency	25%, 50%, 75%, 100% load average at nominal input voltages	84.8	85.5	86.2	%
Operating temperature			25		°C

2.2.1.1 Input Bulk Capacitance and Minimum Bulk Voltage

The minimum voltage on the input bulk capacitance is needed to determine the maximum primary-to-secondary turns-ratio of the transformer. The input power of the converter based on target full-load efficiency, the minimum input RMS voltage, and the minimum AC input frequency determine the input capacitance requirement. Maximum input power is determined based on 式 1:

$$P_{IN} = \frac{V_{OCV} \times I_{OCC}}{\eta} = \frac{12\ V \times 2.2\ A + |-14\ V| \times 0.1\ A + |+14\ V| \times 0.1\ A}{0.8} \approx 36.5\ W \quad (1)$$

where

- V_{OCV} is the regulated output voltage of the converter
- I_{OCC} is the converter total output CC target
- η is the converter overall efficiency at full-power output

式 2 provides an accurate solution for the total input capacitance based on a target minimum bulk capacitor voltage. Alternatively, to target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance value.

$$C_{BULK} = \frac{2P_{IN} \times \left\{0.25 + \frac{1}{2\pi} \times arcsin\left(\frac{V_{BULK(\text{desired})}}{\sqrt{2} \times V_{IN(\text{min})}}\right)\right\}}{\left(2V_{IN(\text{min})}{}^2 - V_{BULK(\text{desired})}{}^2\right) \times f_{LINE(\text{min})}} \approx 58.9\ \mu F \quad (2)$$

$$C_{BULK(selected)} = 68\ \mu F \quad (3)$$

Four 68-µF electrolytic capacitors were used at the input to create an equivalent 68-µF bulk capacitor to support a maximum input voltage of 460 V_{RMS}. This selection changes the minimum V_{BULK} voltage to 90.7 V (also called V_{BULK_VALLEY}) per the UCC28742 design calculator.

2.2.1.2 Transformer Turns-Ratio, Primary Inductance, and Primary Peak Current

The target maximum switching frequency at full load, the minimum input-capacitor bulk voltage, and the estimated DCM resonant time determine the maximum primary-to-secondary turns-ratio of the transformer. Initially, determine the maximum-available total duty-cycle of the on-time and secondary conduction time based on the target switching frequency (f_{MAX}) and DCM resonant time (t_R).

At the transition-mode operation limit of DCM, the interval required from the end of the secondary current conduction to the first valley of the V_{DS} voltage is ½ of the DCM resonant period (t_R), or 1 µs assuming 500-kHz DCM resonant frequency. The maximum allowable MOSFET on-time D_{MAX} is determined using 式 4:

$$D_{MAX} = 1 - D_{MAGCC} - \left(\frac{t_R}{2} \times f_{MAX}\right) = 1 - 0.475 - 38\ kHz \times \frac{2\ \mu s}{2} = 0.485 \quad (4)$$

where

- t_R is the estimated period of the LC resonant frequency at the switch node
- D_{MAGCC} is defined as the duty cycle of the secondary-diode conduction during CC operation and is fixed internally by the UCC28742 device at 0.475

When D_{MAX} is known, the maximum primary-to-secondary turns ratio is determined with 式 5. The total voltage on the secondary winding must be determined, which is the sum of V_{OCV} and V_F.

$$N_{PS(\text{max})} = \frac{D_{MAX} \times V_{BULK\_VALLEY}}{D_{MAGCC} \times (V_{OCV} + V_F)} \quad (5)$$

Assuming V_F = 0.8 V:

$$N_{PS(max)} = \frac{0.485 \times 90.7\ V}{0.475 \times (12\ V + 0.8\ V)} = 7.24 \quad (6)$$

$$N_{PS(selected)} = 7 \quad (7)$$

A higher turns-ratio generally improves efficiency, but can limit operation at a low input voltage. Transformer design iterations are generally necessary to evaluate system-level performance trade-offs.

The primary transformer inductance is calculated using the standard energy storage equation for flyback transformers. The primary current, maximum switching frequency, output voltage and current targets, and transformer power losses are included in 式 8:

$$L_P = \frac{2 \times (V_{OCV} + V_F) \times I_{OCC}}{\eta_{XFMR} \times I^2_{PP(max)} \times f_{MAX}} = 627.7\ \mu H \quad (8)$$

$$L_{P(selected)} = 700\ \mu H \quad (9)$$

The UCC28742 CC regulation is achieved by maintaining D_{MAGCC} at the maximum primary peak current setting. The product of D_{MAGCC} and $V_{CST(max)}$ defines a CC-regulating voltage factor V_{CCR} which is used with N_{PS} to determine the current-sense resistor value necessary to achieve the regulated CC target, I_{OCC} (see 式 10).

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 \times I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (10)$$

$$R_{CS} = \frac{0.363\ V \times 7}{2 \times 2.2\ A} \times \sqrt{0.9} = 0.547\ \Omega \quad (11)$$

$$R_{CS(selected)} = 0.5\ \Omega \quad (12)$$

where

- V_{CCR} is the CC regulation factor (from the *UCC28742 High-Efficiency Flyback Controller with Optocoupler Feedback* data sheet)
- V_{CST} is the CS-pin current-sense threshold (from the *data sheet*)

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} = \frac{0.83\ V}{0.5\ \Omega} = 1.66\ A \quad (13)$$

$$I_{PP(nom)} = \frac{V_{CST(nom)}}{R_{CS}} = \frac{0.77\ V}{0.5\ \Omega} = 1.54A \quad (14)$$

N_{AS} is determined by the lowest target operating output voltage while in CC regulation and by the V_{DD} UVLO turnoff threshold of the UCC28742 device. Additional energy is supplied to V_{DD} from the transformer leakage-inductance which allows a lower turns ratio to be used in many designs.

$$N_{AS} = \frac{V_{DD(off)} + V_{FA}}{V_{OCC} + V_F} = \frac{8.15\ V + 0.8\ V}{5\ V + 0.8\ V} = 1.54 \quad (15)$$

where

- $V_{DD(off)}$ is UCC28742 turnoff threshold (from the *data sheet*)
- V_{OCC} is the lowest output voltage target of the converter while in constant-current regulation
- V_{FA} is voltage drop across rectifier diode on auxiliary side of flyback stage

$$N_{AS(selected)} = 1.455 \quad (16)$$

This implies:

$$N_{PA(selected)} = 4.81 \quad (17)$$

Since the ±14-V rails are unregulated, the turn ratio determines their output voltage:

$$N_{PT} = \frac{N_{PS}}{(V_{OV14} + V_F)/(V_{OCV} + V_F)} = \frac{7}{(14\ V + 0.8\ V)/(12\ V + 0.8\ V)} = 6.05 \quad (18)$$

$$N_{PT(selected)} = 5.92 \quad (19)$$

2.2.1.3 Transformer Parameter Calculations: Primary and Secondary RMS Currents

With the primary inductance of 700 µH, the absolute maximum switching frequency is calculated from:

$$f_{MAX} = \frac{2 \times (12\ V + 0.8\ V) \times 2.2\ A}{0.9 \times \left(1.54\ A\right)^2 \times 700\ \mu H} = 37.7\ kHz \quad (20)$$

The maximum switching period is:

$$t_{SW} = \frac{1}{f_{MAX}} = \frac{1}{37.7\ kHz} = 26.5\ \mu s \quad (21)$$

The actual maximum on-time is given by:

$$t_{ON(\max)} = \frac{I_{PP(nom)} \times L_P}{V_{BULK\_VALLEY}} = \frac{1.54\ A \times 700\ \mu H}{90.7\ V} = 11.88\ \mu s \quad (22)$$

The maximum duty cycle of operation (D_{MAX}) is:

$$D_{MAX} = \frac{t_{ON(max)}}{t_{SW}} = \frac{11.88\ \mu s}{26.5\ \mu s} = 0.448 \quad (23)$$

The transformer primary RMS current (I_{PRMS}) is:

$$I_{PRMS} = I_{PP(max)}\sqrt{\frac{D_{MAX}}{3}} = 1.66\ A \times \sqrt{\frac{0.448}{3}} = 0.641\ A \quad (24)$$

The transformer secondary peak current RMS current ($I_{SEC(max)}$) is:

$$I_{SEC(max)} = I_{PP(max)} \times N_{PS} = 1.66\ A \times 7 = 11.62\ A \quad (25)$$

The transformer secondary RMS current (I_{SEC_RMS}) is:

$$I_{SEC\_RMS} = I_{SEC(max)}\sqrt{\frac{D_{MAX}}{3}} = 11.62\ A \times \sqrt{\frac{0.448}{3}} = 4.49\ A \quad (26)$$

Based on these calculations, a Würth Elektronik™ transformer was designed for this application (part number 750320029), which has the following specifications:

- N_{PS} = 7 ±2% (primary to secondary turns-ratio)
- N_{PT} = 5.92 ±2% (primary to tertiary turns-ratio)
- N_{PA} = 4.81 ±2% (primary to auxiliary turns-ratio)
- L_P = 700 ±10% µH (primary inductance)
- L_{LK} = 10 µH (primary leakage inductance)

2.2.1.4 Main Switching Power MOSFET Selection

The drain-to-source RMS current, I_{DS_RMS}, through switching FET is calculated using:

$$I_{DS\_RMS} = I_{PRMS} = 0.641\ A \quad (27)$$

Select a MOSFET with five times the I_{DS_RMS} calculated. The maximum voltage across the FET can be estimated using:

$$V_{DSPK} = \left(V_{IN(max)} \times \sqrt{2}\right) + \left(V_{OCV} + V_F\right) \times N_{PS} + V_{LK} = \left(460\ V \times \sqrt{2}\right) + \left(12\ V + 0.8\ V\right) \times 7 + 63\ V = 803.1\ V \quad (28)$$

Considering a de-rating of 15% and leakage spike of around 150 V, the voltage rating of the MOSFET must be around 925-V DC. A 950-V MOSFET is selected.

2.2.1.5 Rectifying Diode Selection

Calculate the secondary output diode or synchronous rectifier FET reverse voltage or blocking voltage needed ($V_{DIODE\_BLOCKING}$):

$$V_{DIODE\_BLOCKING} = \frac{V_{IN\_DC(max)}}{N_{PS}} + V_{OCV} = \frac{460\ V \times \sqrt{2}}{7} + 12\ V = 104.9\ V \quad (29)$$

For this reference design, a 200-V, 24-A rated synchronous rectifier FET is selected for the +12-Vp rail to reduce losses. For the ±14 rails, Schottky diodes with 200-V voltage and 1-A forward current ratings are selected.

$$V_{DIODE\_BLOCKING\_AUX} = \frac{V_{IN\_DC(max)}}{N_{PA}} + \left(V_{OCV} + V_F\right) \times N_{AS} - V_{FA} = \frac{460\ V \times \sqrt{2}}{4.81} + \left(12\ V + 0.8\ V\right) \times 1.455 - 0.6\ V = 153\ V \quad (30)$$

For the auxiliary rail, a Schottky diode with 400-V voltage and 1-A forward current ratings is selected. Here normally a 200-V diode is sufficient, but spikes over 153 V must be considered. If a 300-V diode, is selected, the diode does not bring any advantage because 300-V and 400-V small diodes have no difference in terms of reverse recovery time, nor V_F.

2.2.1.6 Output Capacitor Selection

For this reference design, the output capacitor (C_{OUT}) for output is selected to prevent V_{OUT} (12 V) from dropping below the minimum output voltage (V_{OTRM}) during transients up to 0.1 V and ripple voltage less than 100 mV.

$$C_{OUT} \geq \frac{\frac{I_{OCC}}{2} \times \left(t\right)}{V_{OCV} - V_{OTRM}} \quad (31)$$

Assuming V_{OTRM} = 11.9 V,

$$C_{OUT} \geq \frac{\frac{2.2\ A}{2} \times (50\ \mu s)}{12\ V - 11.9\ V} \geq 550\ \mu F \quad (32)$$

$$C_{OUT(selected)} = 2\ \times\ 680\ \mu F \quad (33)$$

Considering the allowable output ripple voltage of 100 mV (5%), the ESR and RMS current of the capacitor must be:

$$ESR = \frac{V_{OUT\_RIPPLE}}{I_{SEC(max)}} = \frac{200\ mV}{11.62\ A} = 17.2\ m\Omega \quad (34)$$

$$I_{COUT\_RMS} = \sqrt{\left(I_{SEC\_RMS}\right)^2 - \left(I_{OCC}\right)^2} = \sqrt{\left(4.49\ A\right)^2 - \left(2.2\ A\right)^2} = 5.0\ A \quad (35)$$

2.2.1.7 Capacitance on VDD Pin

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in CC regulation. The capacitance on VDD must supply the primary-side operating current used during start-up and between low-frequency switching pulses. The largest result of two independent calculations denoted in 式 36 determines the value of C_{VDD}.

At start-up, when $V_{VDD(on)}$ is reached, C_{VDD} alone supplies the device operating current and MOSFET gate current until the output of the converter reaches the target minimum operating voltage in CC regulation, V_{OCC}. Now the auxiliary winding sustains VDD for the UCC28742 device above UVLO. The total output current available to the load and to charge the output capacitors is the CC-regulation target, I_{OCC}. 式 36 assumes that all of the output current of the converter is available to charge the output capacitance until V_{OCC} is achieved. For

typical applications, 式 37 includes an estimated $q_G \times f_{SW(max)}$ of average gate drive current and a 1-V margin added to V_{VDD}.

$$C_{VDD} \geq \frac{\left(I_{RUN} + q_G f_{SW(max)}\right) \times \frac{C_{OUT} \times V_{OCC}}{I_{OCC}}}{V_{DD(on)} - \left(V_{DD(off)} + 1\ V\right)} \tag{36}$$

$$C_{VDD} \geq \frac{(2\ mA + 10\ nC \times 37.7\ kHz) \times \frac{1360\ \mu F \times 12\ V}{2.2\ V}}{21\ V - (8.5\ V + 1\ V)} \geq 0.128\ \mu F \tag{37}$$

The current design uses 10-µF and 0.1-µF capacitors.

2.2.1.8 Open-loop Voltage Regulation Versus Pin Resistor Divider, Line Compensation Resistor

The resistor divider at the VS pin determines the output voltage regulation point of the flyback converter. Also, the high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous DRV operation. R_{S1} is initially determined based on transformer auxiliary-to-primary turns ratio and desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(min)}} \tag{38}$$

where

- N_{PA} is the transformer primary-to-auxiliary turns ratio
- $V_{IN(run)}$ is the AC_{RMS} voltage to enable turn-on of the controller (run); in case of DC input, leave out the $\sqrt{2}$ term in the equation
- $V_{SL(run)}$ is the run threshold for the current pulled out of the VS pin during the switch on-time (see the *Electrical Characteristics* section of the UCC28742 data sheet)

$$R_{S1} = \frac{80\ V \times \sqrt{2}}{4.81 \times 210\ \mu A} = 112\ k\Omega \tag{39}$$

$$R_{S1(selected)} = 121\ k\Omega \tag{40}$$

The low-side VS pin resistor is selected based on the desired V_{OUT} regulation voltage in open-loop conditions and sets the maximum allowable voltage during open-loop conditions.

$$R_{S2} = \frac{R_{S1} \times V_{OVPTH}}{N_{AS} \times (V_{OV} + V_F) - V_{OVPTH}} \tag{41}$$

where

- V_{OV} is the maximum allowable peak voltage at the converter output
- V_F is the output-rectifier forward drop at near-zero current
- N_{AS} is the transformer auxiliary-to-secondary turns ratio
- V_{OVPTH} is the overvoltage detection threshold at the VS input (see the Electrical Characteristics section of the UCC28742 data sheet)

$$R_{S2} = \frac{121\ k\Omega \times 4.65\ V}{1.455 \times (15\ V + 0.8\ V) - 4.65\ V} = 30.7\ k\Omega \tag{42}$$

$$R_{S2(selected)} = 33.2\ k\Omega \tag{43}$$

The UCC28742 device maintains tight CC regulation over varying input lines by using the line-compensation feature. The line-compensation resistor (R_{LC}) value is determined by the current flowing in R_{S1} and the total internal gate drive and external MOSFET turn-off delay. Assuming an internal delay of 50 ns in the UCC28742 device:

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \quad (44)$$

where

- t_D is the current-sense delay including MOSFET turn-off delay
- K_{LC} is a current-scaling constant (see the Electrical Characteristics section of the UCC28742 data sheet)

$$R_{LC} = \frac{25 \times 121\ k\Omega \times 0.5\ \Omega \times (46\ ns + 50\ ns) \times 4.81}{700\ \mu H} = 998\ \Omega \quad (45)$$

$$R_{LC(selected)} = 1\ k\Omega \quad (46)$$

2.2.1.9 Feedback Elements

The output voltage is set through the sense network resistors R_{FB1} and R_{FB2}. Select the value of the feedback resistor based on the desired output voltage with:

$$V_{th} = \frac{V_{OCV} \times R_{FB2}}{R_{FB1} + R_{FB2}} \quad (47)$$

where

- V_{th} = 2.5 V

The op amp compensation network, Z_{FB}, is determined using well-established design techniques for control-loop stability. Typically, a type-II compensation network is used. See the *UCC28742 data sheet* and the design calculator for details.

2.2.1.10 Backup Power Supply

There are three possible power scenarios:

1. Single or three-phase power available:
   a. The converter supplies all voltages and charges the supercapacitors in a variable time between 1 minute and 21 seconds as first charge, and 36 seconds as successive recharges.
   b. The switching waveform present on the secondary side winding is peak-rectified and is used to disable the inverting buck-boost.
   c. At the same time, as the voltage on the supercapacitors is in the range 4.3 V–7.8 V, the boost converter is active and delivers 11.5 V. This voltage level, slightly lower than 12 V, is on purpose to avoid delivering current when mains is present. Keeping the boost converter active eliminates the delay due to the device soft start.
   d. When the supercapacitors are charged, a voltage supervisor TL7705A is enabling the flag “EOC” (end of charge, useful for a digital output to uC) and turning an LED on.
2. Power unavailable:
   a. Since the boost converter with TPS55330 is always active, the 12-Vp bus droops from 12 V to 11.5 V, keeping all rails alive.
   b. At the same time, both ± 14-V outputs from the flyback converter go to zero and the peak rectified voltage used for the signal *Disable* goes to zero.
   c. Then the inverting buck-boost starts and supplies ±14 V, which are connected by ORing diodes to the input of the dual LDO, supplying ± 12 V.
   d. The power is delivered until the supercapacitors are discharged below boost UVLO (4.3 V). At this point all rails are off.
3. 12-V bench supply on:
   a. Here the supercapacitors are not recharged because there is no voltage on auxiliary winding of the flyback.
   b. The 12 V from bench power is supplying all the rails normally. The inverting buck-boost is also supplying ±14 V for dual LDO.

2.2.1.11 Supercapacitor Selection

The supercapacitors supplies the 12-V and the 5-V rails (AM62 SOM) in case of unexpected AC input shut down to turn off the main relay and unlock the plug. Assume 1 s duration time as the initial specification.

- 12-V rail: Peak current 1.8 A for 200 ms (unlock plug and relay off)
- 12-V rail: Average current 1.8 A × 0.2 s + 0.1 A × 0.8 s = 0.44 A
- 5-V rail: Average current 0.275 A for 1 s

The total peak power required from supercap, P_{PK_SC}:

$$P_{PK\_SC} = (V_{12Vp} \times I_{PK\_1} + V_{5V} \times I_{PK\_2} / \eta_{BUCK}) / \eta_{BOOST} \quad (48)$$

$$P_{PK\_SC} = (12\ V \times 1.8\ A + 5\ V \times 0.275\ A / 0.9) / 0.85 = 27.2\ W \quad (49)$$

Total 27.2 W peak for 200 ms or a peak current of approximately 3.5 A (that is, 27.2 W / 7.8 V). Total average power required from supercapacitor, P_{AVE_SC}:

$$P_{AVE\_SC} = (V_{12Vp} \times I_{AVE\_1} + V_{5V} \times I_{AVE\_2} / \eta_{BUCK}) / \eta_{BOOST} \quad (50)$$

$$P_{AVE\_SC} = (12\ V \times 0.44\ A + 5\ V \times 0.275\ A / 0.9) / 0.85 = 8\ W \text{ (that is, 8 J in 1 s)} \quad (51)$$

Consider that the supercapacitor is charged up to 7.8 V and then discharged down to 4.3 V (that is, UVLO of the TPS55330 boost converter):

$$C_{MIN\_SERIES} = 2 \times (E) / ((V_2)^2 - (V_1)^2) = 2 \times (8\ J) / ((7.8\ V)^2 - (4.3\ V)^2) = 0.3778\ F. \quad (52)$$

$$C_{MIN} = 2 \times C_{MIN\_SERIES} = 0.76\ F \text{ (for 1 s)} \quad (53)$$

where

- C_{MIN_SERIES} is the minimum equivalent series capacitor
- C_{MIN} is the minimum individual capacitance

Now, for 3 s we need $C_{MIN} = 3 \times 0.76 = 2.28$ F.

For this design, two 2.5-F in series that support up to 47.5 W and 4 A peak are selected.

Note that the TL7705 voltage supervisor monitors for charge completion at an slightly lower voltage of 7.49 V. The supercapacitor energy available from 7.49 V to 4.3 V, E_{SC_7p5}:

$$E_{SC\_7p5} = 0.5 \times C \times (V_1^{\ 2} - V_2^{\ 2}) = 0.5 \times 1.25\ F \times (7.49^2 - 4.3^2) = 23.5\ J \quad (54)$$

The energy available after accounting for boost efficiency, $E_{SC\_7p5\_BOOST}$:

$$E_{SC\_7p5\_BOOST} = E_{SC\_7p5} \times \eta_{BOOST} = 23.5\ J \times 0.85 = 20\ J \quad (55)$$

The power available during 3 s, P_{SC_7p5}:

$$P_{SC\_7p5} = E_{SC\_7p5\_BOOST} / \text{time} = 20\ J / 3\ s = 6.65\ W \quad (56)$$

The supercapacitor energy available from 7.8 V to 4.3 V, E_{SC_7p8}:

$$E_{SC\_7p8} = 0.5 \times C \times (V_1^{\ 2} - V_2^{\ 2}) = 0.5 \times 1.25\ F \times (7.8^2 - 4.3^2) = 26.5\ J \quad (57)$$

The energy available after accounting for boost efficiency, $E_{SC\_7p8\_BOOST}$:

$$E_{SC\_7p8\_BOOST} = E_{SC\_7p8} \times \eta_{BOOST} = 26.5\ J \times 0.85 = 22.5\ J \quad (58)$$

The power available during 3 s, P_{SC_7p8}:

$$P_{SC\_7p8} = E_{SC\_7p8\_BOOST} / \text{time} = 22.5\ J / 3\ s = 7.5\ W \quad (59)$$

2.2.1.12 Supercapacitor Charger Design

The shunt voltage reference (U6_P) sets the final charge voltage to 7.8 V. The NPN transistor (Q4_P) and 4.99-Ω resistor (R38_P) limit the charge current to approximately 120 mA (0.6 V / 4.99 Ω). The NMOS FET (Q3_P) operates in saturation region to maintain the required charge voltage drop. U6_P pulls down the gate of Q3_P as soon as Vbackup (as shown in the schematic) reaches 7.8 V. This way, Vbackup stays constant at the nominal 7.8 V. There are two charging scenarios:

1. Charging time as first power supply turn-on: here Vbackup is zero. The ΔV that must be covered is from zero to 7.8 V; therefore, the charging time is ΔT = C × ΔV / I = 1.25 F × 7.8 V / 120 mA = 81.25 seconds (1 minute and 21 seconds).
2. Charging time after energy storage release: here Vbackup is the UVLO of the boost converter (4.3 V). The ΔV that must be covered is from 4.3 V to 7.8 V; the charging time is ΔT = C × ΔV / I = 1.25 F × (7.8 V – 4.3 V) / 120 mA = 36.46 seconds.

In summary, the worst-case charging time is 1 minute and 21 seconds, while recharging between energy storage releases is 36.46 seconds.

2.2.2 Control Pilot Signal Interface

The control pilot circuit is the primary control means to make sure of proper operation when connecting an EV or PHEV to the EVSE. The pilot signal is the key method through which a J1772-compliant EVSE communicates with a vehicle. The pilot signal is based on a 1-kHz, ±12-V PWM signal that is transmitted to a vehicle over the charging chord. The vehicle can then respond by placing various loads on the line, affecting the voltage, which the EVSE measures.

2.2.2.1 J1772 Duty Cycle

The duty cycle of the pilot signals communicate the limit of current the EVSE is capable of supplying to the vehicle; the vehicle can then use up to that amount of current for the charging circuitry. This current rating is primarily determined by the electromechanical components in the EVSE, such as conductors, relays, contactors, and the service connection.

The relationship between duty cycle and current is defined by two different equations depending on the current range specified; for a 6- to 51-A service, is:

$$\text{Duty cycle} = \frac{\text{Amps}}{0.6} \tag{60}$$

For a higher service in the 51- to 80-A range, is:

$$\text{Duty cycle} = \frac{\text{Amps}}{2.5} + 64 \tag{61}$$

To demonstrate this relationship further, 表 2-2 shows some of the common service ratings.

表 2-2. Pilot Signal Example Duty Cycle

AMPS	DUTY CYCLE
5	8.3%
15	25%
30	50%
40	66.6%
65	90%
80	96%

In this design, the PWM is generated by a timer module on the MSP430™ MCU. The current rating can typically be set as a permanent value in the firmware because the current rating is so tightly coupled to the external hardware.

Advanced EVSEs with a human machine interface (HMI) can enable the current to be derated if the service line is unable to provide enough current with a stable voltage. A significant voltage drop as a result of wire loss is possible in these high-current applications.

2.2.2.1.1 Control Pilot Signal States

The EVSE connection and negotiation occurs through various states of the PWM signal and load resistances of the vehicle. 表 2-3 highlights these states.

表 2-3. Pilot Signal State Parameters

STATE	PILOT HIGH VOLTAGE	PILOT LOW VOLTAGE	FREQUENCY	RESISTANCE	DESCRIPTION
State A	12 V	N/A	DC	N/A	Not connected
State B	9 V	–12 V	1 kHz	2.74 kΩ	EV connected, ready to charge
State C	6 V	–12 V	1 kHz	882 Ω	EV charging
State D	3 V	–12 V	1 kHz	246 Ω	EV charging, ventilation required
State E	0 V	0 V	N/A	—	Error
State F	N/A	–12 V	N/A	—	Unknown error

States A, B, and C are the core functionality and define the normal operation. An EVSE typically performs several self-tests upon initially powering on and then enters State A. When ready, the normal connection process follows several steps:

1. The EVSE puts 12 V on the pilot wire. This transmission signals the vehicle when the plug is connected.
2. When the plug is connected, the vehicle places a 2.74-kΩ load on the pilot line, which drops the voltage to 9 V.
3. The EVSE moves to State B, where the EVSE enables the PWM, which signals the vehicle how much current the vehicle can draw. The EVSE also closes the relays, providing power to the vehicle.
4. The vehicle starts to draw power and switches to the 822-Ω load, which drops the voltage to 6 V, signaling the EVSE that charging has started.
5. Most vehicles continue to pull low amounts of power in state C, even when fully charged, so the charging process is ended by unplugging the cable, which returns the voltage to 12 V. The EVSE measures this process and closes the relays and returns to State A.

Additional error handling such as missing diodes in the vehicle or an improper connection can be detected and handled by the EVSE by cutting the power, as well.

2.2.2.1.2 Control Pilot Signal Circuit

The pilot signal is required to travel down several meters of cable and through a load resistance. The pilot signal is also a bipolar ±12-V signal, which requires special consideration. To accommodate these parameters, an amplifier with a wide input range and reasonable power output is selected. The TLV1805 device has a voltage rating of ±18 V and a current rating of 475 mA, making the device a good match for the application. In addition, while most EVSEs do not require an automotive qualification, a Q1-rated variant of the TLV1805-Q1 device exists, if this feature is desired.

The amplification circuit is a simple rail-to-rail output configuration of the TLV1805 device, with the MCU I/O driving the positive input. The output of the pilot amplifier is also fed into a simple voltage divider so that the MCU can measure the voltage during operation and detect the load resistance of the vehicle. 図 2-3 shows the full schematic of this subsystem.

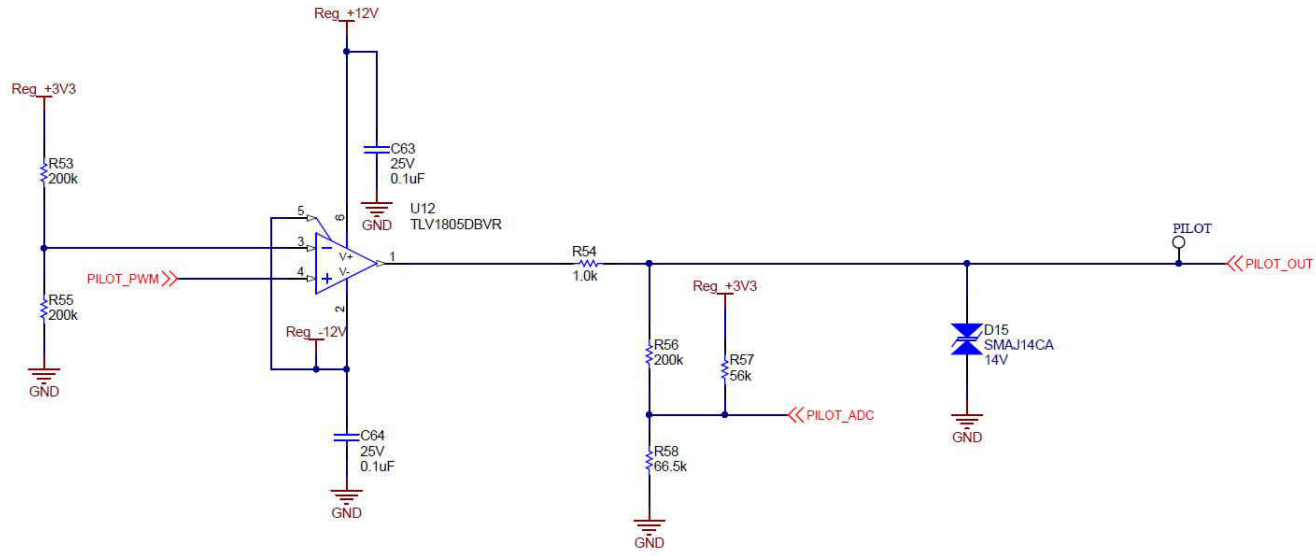


図 2-3. Control Pilot Signal Generator Circuit

To validate the architecture, the design was tested in the TINA-TI™ software from TI, which is a spice-based simulation tool.

2.2.3 Relay Drive and Weld Detect

The primary functionality of the EVSE is the reliable control of large currents directed toward an electric vehicle at the mains voltage. In a normal use case, the relay or contactor must be held closed for several hours to fully charge a vehicle; however, the relays cannot be welded because of safety concerns. If something fails in the control system, the relays must fail open. These high current relays or contactors can typically draw tens to hundreds of milliamps as an inductive load, requiring specific drive architectures.

Because of the amount of time that a relay or contactor requires to remain powered, an efficient drive device is preferred to the typical Darlington array, or even discrete transistor configuration. For this reason, the DRV8220 current controller is selected to drive the relays or contactors in the design. The DRV8220 device is designed to regulate the current with a well-controlled waveform to reduce power dissipation.

Relays and contactors use electromechanical solenoids for their operation. Activation starts when EN pin voltage is pulled high either by an external driver or internal pullup. Once the EN pin is driven to GND, the DRV8220 device allows the solenoid current to decay to zero. The solenoid current is ramped up fast to enable opening of the relay or contactor. After initial ramping, the solenoid current is kept at a peak value to maintain correct operation, after which the current is reduced to a lower hold level to avoid thermal problems and reduce power dissipation.

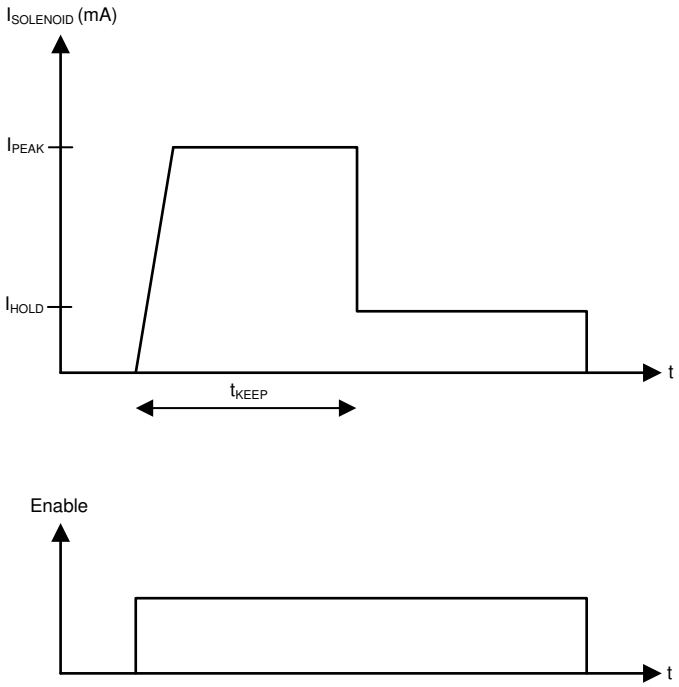


図 2-4. Typical Current Waveform Through the Solenoid

For safety reasons, detecting the output voltage of the primary relay is critical. The contacts can experience arcing and become fused together, providing power to the plug even when the contacts are not enabled. Checking that the operation completed correctly is important and must be done every time the relay is opened. To implement this check, the ISO1212 fully-integrated, isolated digital-input receiver is used to sense line voltage.

The outputs (OUT1 and OUT2) from the ISO1212 device are GPIO-level DC signals that are high when voltage is present and are fed directly into the MCU for fault detection. For this reference design, the high and low thresholds are set to 125 V_{RMS} and 121 V_{RMS}, respectively. The full circuit is shown in 図 2-5. To learn more about AC and DC detection with ISO1212, see *ISO121x Threshold Calculator for 9V to 300V DC and AC Voltage Detection*.

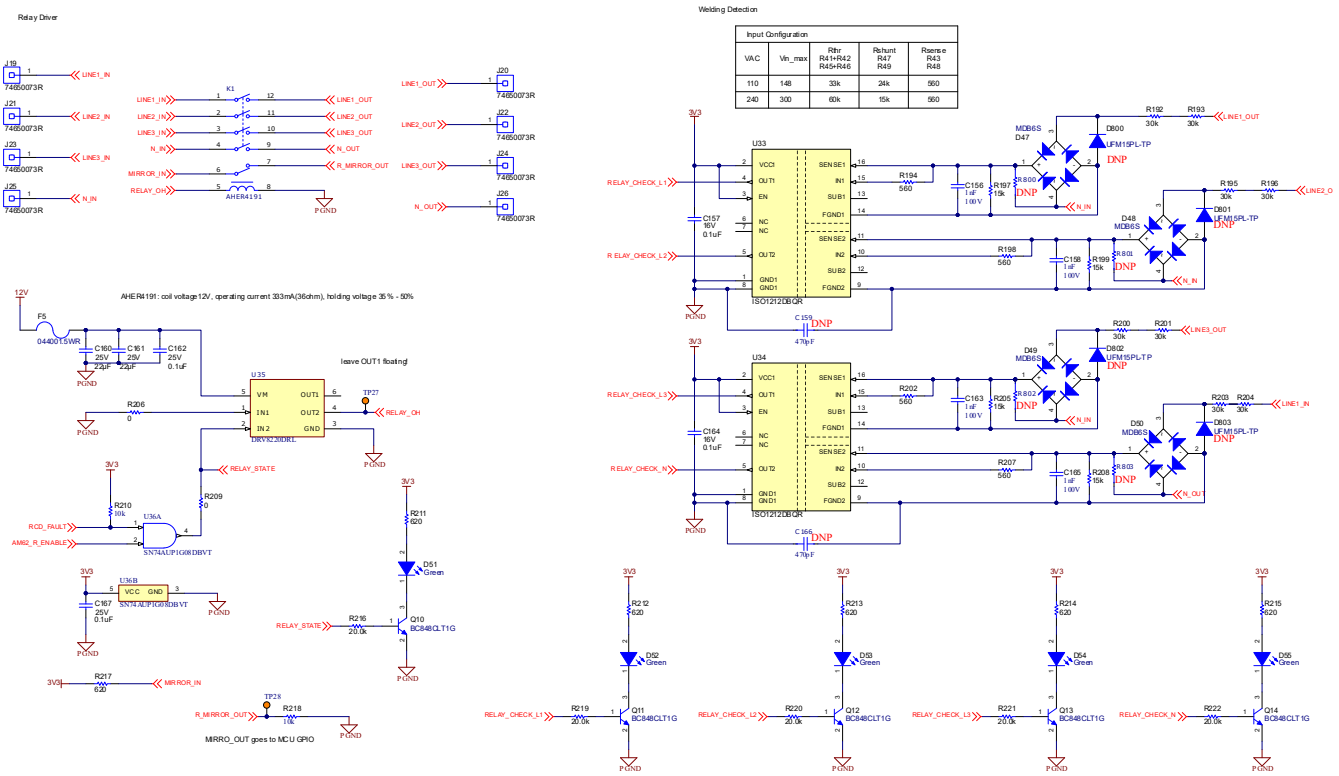


図 2-5. AC Weld Detect Circuit

2.2.4 Residual Current Detection

This reference design implements a discrete version of residual current detection (RCD) capable of detecting two types of ground faults, AC current of 30 mA_{RMS} and DC current of 6 mA. This detection is enabled utilizing an auto-oscillation circuit along with a receiver filter circuit. For the auto-oscillation circuit, the DRV8220 H-bridge is used to drive the magnetic core in and out of saturation. In addition, a feedback circuit is used to determine when the core reaches saturation and switches the drive coil current in the opposite direction. This enables the design to detect small amounts of DC current with a single toroidal magnetic core. The receive filter stage is used to filter the auto-oscillation driving frequency and signal condition the fault current signal. This filtered signal is captured by the internal ADC of the MSP430 with a sampling rate of 25,000 samples per second. The signal highest and lowest values are stored over 10 ms to determine if the fault type is AC or DC. The AC and DC trip thresholds can be adjusted via software to support different regional specifications. If the stored values are above trip thresholds, the MCU outputs a GPIO high, which is intended to interface with a relay driver to trip the relay. The GPIO returns low when the fault current lowers below an adjustable hysteresis. A summary of the sub-circuits follows for the AC and DC leakage current detection circuit.

注

The following RCD description references component designators from the TIDA-010237 schematic. For a more detailed RCD description see the TIDA-010237 user's guide.

2.2.4.1 Auto-Oscillation Circuit

The auto-oscillation sub-circuit detects when the fluxgate sensor reaches saturation, then reverses the current direction. When saturation is reached, current sense voltage exceeds the comparator threshold, which causes the DFF to flip control signals to the DRV8220 H-bridge. This drives the fluxgate sensor core to saturation in the opposite direction.

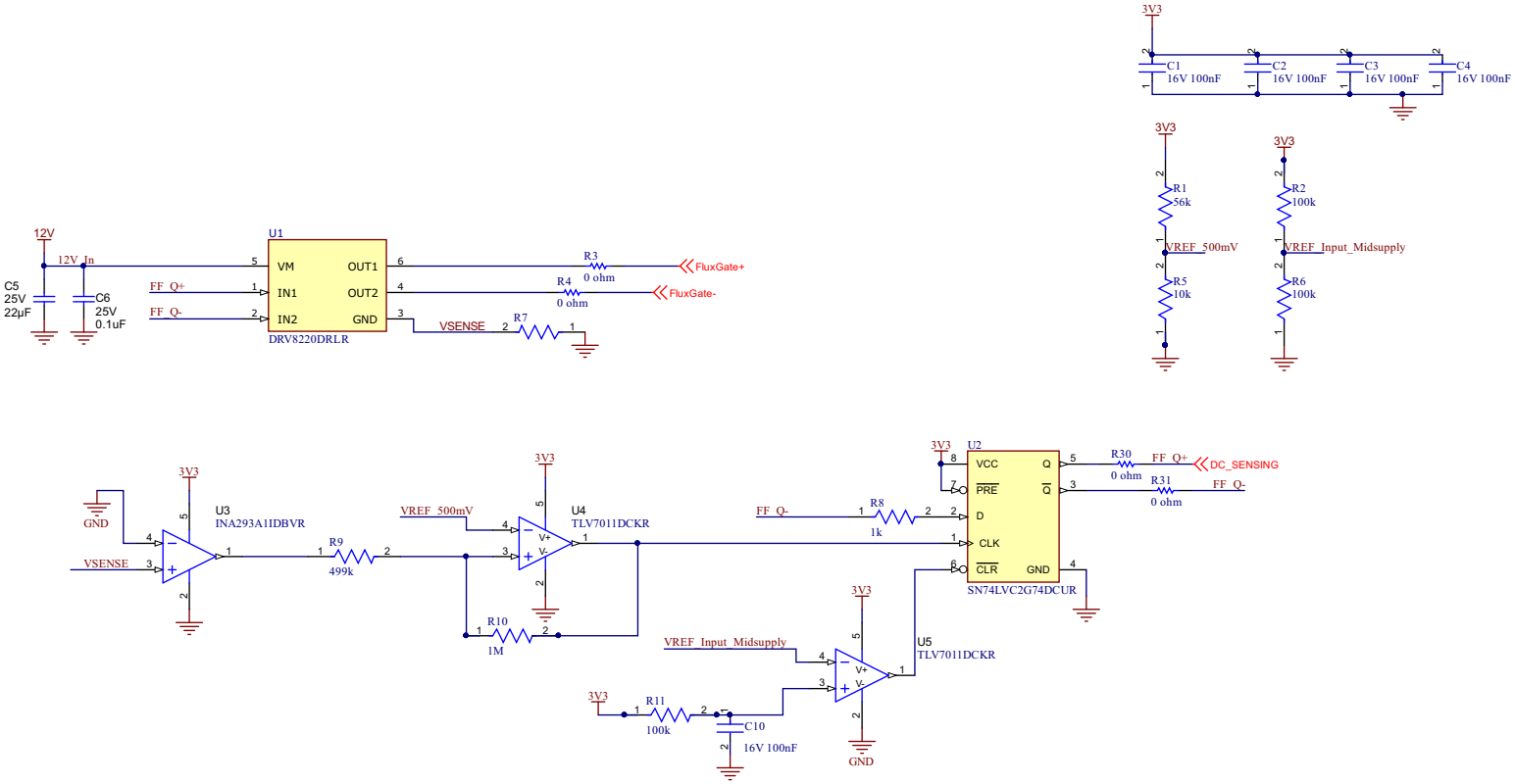


図 2-6. Auto-Oscillation Circuit Schematic

This circuit monitors the current flowing through the fluxgate and reverses drive current direction once saturation is reached. The auto-oscillation circuit is needed to detect DC faults.

The phase lines and neutral wires go through a fluxgate sensor. During normal operation without a fault condition, the sum of currents equals zero.

During a ground fault condition, the sum of currents is not equal to zero. During a DC fault, there is an imbalance of current flowing through the line and current returning through the neutral wire. The fluxgate does not detect steady DC current. An oscillating drive current is pushed through the fluxgate sensor coil. This DC fault current produces a magnetic field which opposes fluxgate drive in one direction, and assists fluxgate drive in the opposite direction; resulting in a duty cycle shift. Under normal conditions, the duty cycle of the switching is 50%. During a DC fault, the duty cycle shifts.

The oscillation frequency depends on the signal chain between R7 to pin 1 of the DFF. Match the current sense amplifier gain and V_{REF} voltage to make sure the core is driven to saturation. Driving the core deeper into saturation reduces noise, removing the need for degaussing. When the core is fully saturated, all material within the core is magnetically aligned. When all material is aligned, there are no stray fields within the material to contribute noise.

2.2.4.2 DRV8220 H-Bridge

The DRV8220 is an integrated motor driver with four N-channel power FETs, charge pump regulator, and protection circuitry. The device can supply up to 1.76 A of output current, operating on a supply voltage from 4.5 V to 18 V. The driver offers robust internal protection including undervoltage lockout, output overcurrent, and device overtemperature. The DRV8220 drives current through the magnetic core to saturate the core. This device is the smallest, most cost-effective device capable of driving enough current. The output of the DRV8220 is controlled by pins 1 and 2. The state of these pins determines which direction current flows through the magnetic coil. When the saturation detection circuit threshold is passed, the control signals to pins 1 and 2 flip, which flips the DRV8220 output. The low-side current sense resistor (R7) detects current through the DRV8220. The current spikes when the core reaches saturation, which is read by the saturation detection circuit.

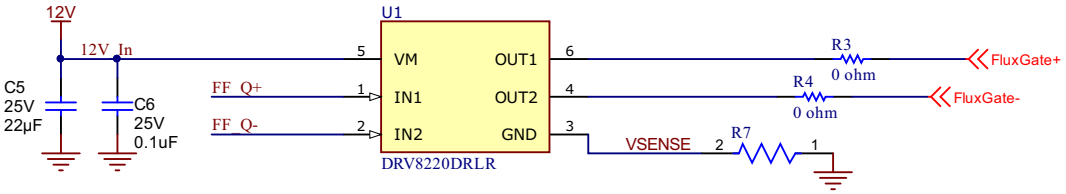


図 2-7. DRV8220 Schematic

2.2.4.3 Saturation Detection Circuit

The saturation detection circuit is made of the low-side current sense resistor (R7), current sense amplifier INA293, and comparator TLV7011. The comparator outputs high when the fluxgate sensor coil saturation is reached. The circuit shown in 図 2-8 is used to determine when the fluxgate sensor has reached saturation.

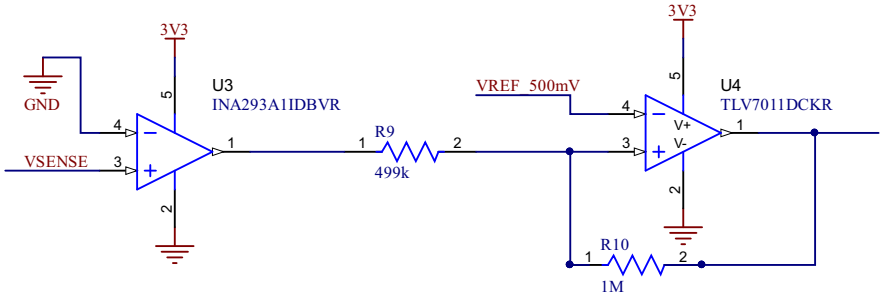


図 2-8. Saturation Detection Schematic

V_{SENSE} is read from the low-side shunt resistor of the DRV8220. V_{SENSE} gives the current through the fluxgate sensor coil. This signal is gained up by current sense amplifier INA293, with a fixed gain of 20 V/V. The gained signal is compared to a reference voltage V_{REF} of 500 mV, which is sourced from a resistor divider. When the current sense signal passes the V_{REF} voltage, the core has saturated and the DRV8220 must switch the output directions. The output of comparator TLV7011 feeds into a DFF which is explained more in the H-Bridge Controlled by DFF section.

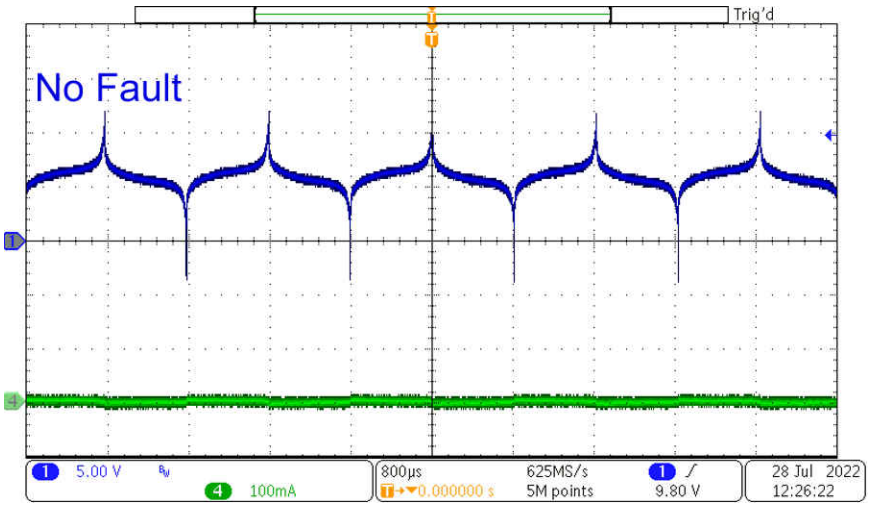


図 2-9. Burden Resistor Going Into Saturation

2.2.4.4 H-Bridge Controlled by DFF

The output logic to control DRV8220 reverses output Q with each positive CLK edge. The DFF circuit reverses output Q with each positive CLK edge. Inverted output $\overline{Q}$ is connected to input data D, so each positive clock edge inverts the outputs.

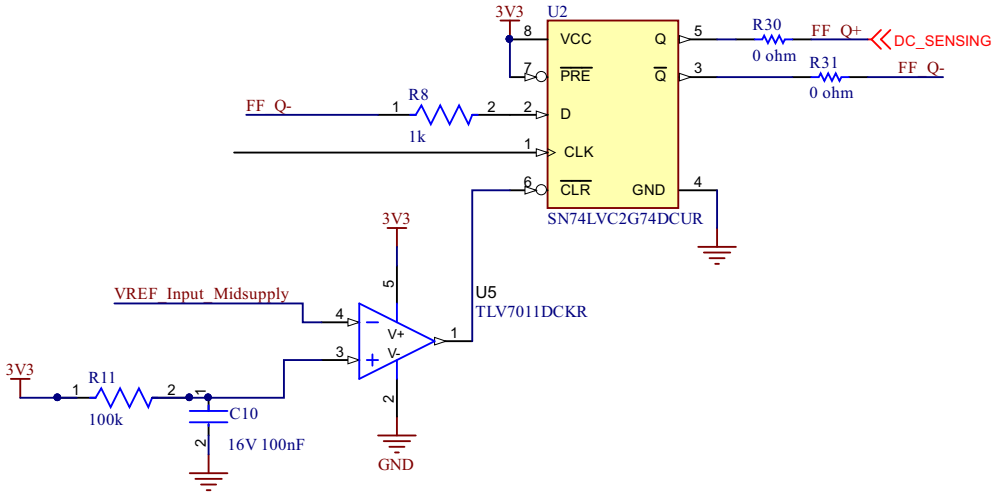


図 2-10. DFF SN74LVC2G74 Circuit

2.2.4.5 Filter Stage

The three goals of filter stage are to gain the ground fault detection signal, filter the noise created by the auto-oscillation circuit, and correct a DC bias inherent to the fluxgate core. The filter filters noise in the signal path from the burden resistor to the ADC. Too much noise can trigger false trips. The major source of noise is switching noise caused by the auto-oscillation circuit generating switching of the DRV8220. The auto-oscillation switching frequency changes with fluxgate sensor permeability, burden resistance, or adjusting the saturation detection circuit. The Hitachi nanocrystalline cores used for testing ranged from 600 Hz to 800 Hz with a 1-kΩ burden resistor.

During a fault, the filter stage outputs a detectable signal read by the ADC. A fault trip occurs when the filter stage output signal passes a threshold and the MCU determines the fault type, as AC and DC faults have separate trip thresholds adjustable within software. In this design with a gain of 20 dB, a DC fault of 6-mA outputs a 200-mV offset. An AC fault of 30-mA_{RMS} outputs a peak of 600 mV. The gain can be increased, make sure the trip threshold is below the rail of op amps. The filter stage is designed to gain the fault signal by 20 dB and attenuate frequencies above 70 Hz. The filter stage consists of four subsections: differential to single end, low-pass filter, full-wave rectifier, and a DC offset circuit in place of R23.

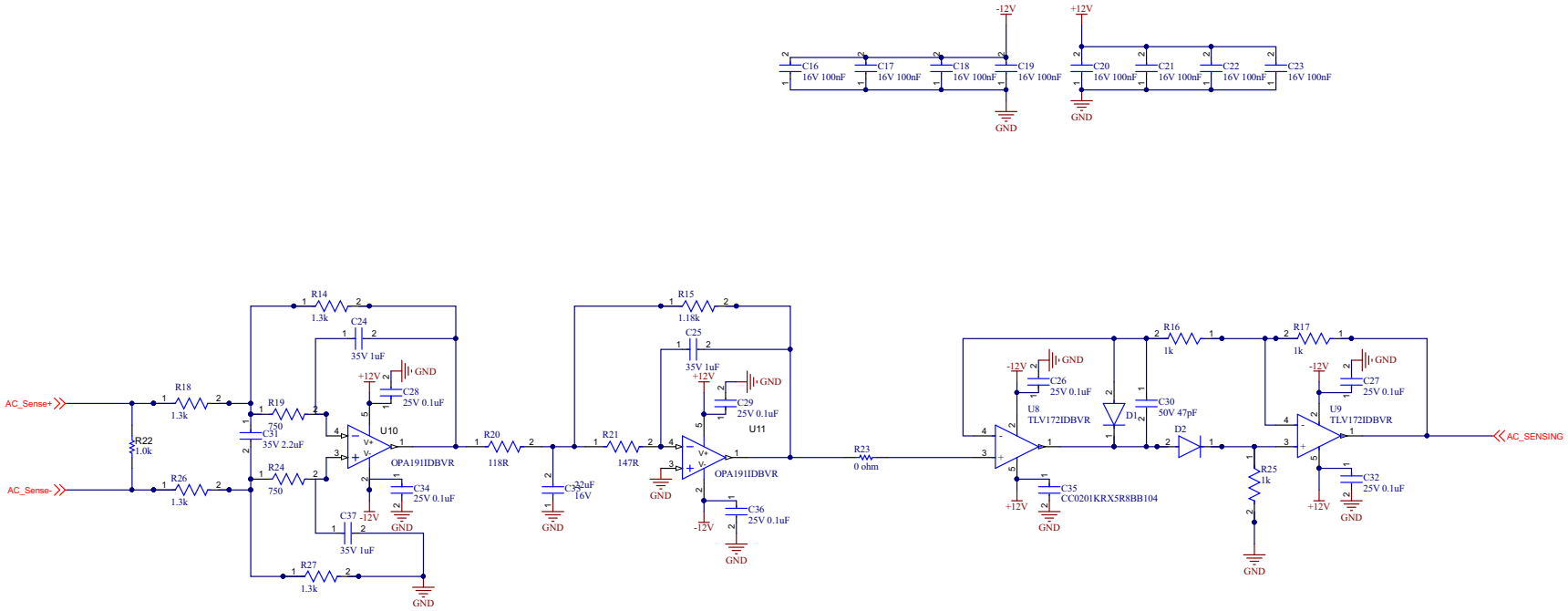


図 2-11. Filter Stage Schematic

The filter topology used is the Multiple FeedBack (MFB) topology and is often preferred due to low sensitivity to component variations. The MFB topology creates an inverting second-order stage. This inversion can be a concern in the filter application. The MFB filter circuit can be configured as a low-pass filter, high-pass filter, or band-pass filter based on the component selection. For this application, a fourth-order low-pass filter with a Butterworth response was used.

2.2.4.6 Differential to Single-Ended Converter

The differential to single-end conversion is performed by the first part of the signal chain. The first op amp converts the differential signal across the fluxgate burden resistor to a single-ended signal. This simplifies later signal conditioning and allows the ADC to read a ground referenced signal. R22 is the burden resistor across the coils of the fluxgate sensor.

Impedance matching to op amp inputs is important to minimize error. Mismatched impedance adds error to the fault detection signal. Trace from R22 to U10 can be similar to reduce error. To increase the ground fault signal, replace R18 and R26 with buffer op amps or resistors an order of magnitude larger. A higher impedance relative to the burden resistor (R22) gives a higher ground fault signal due to the resistor divider effect.

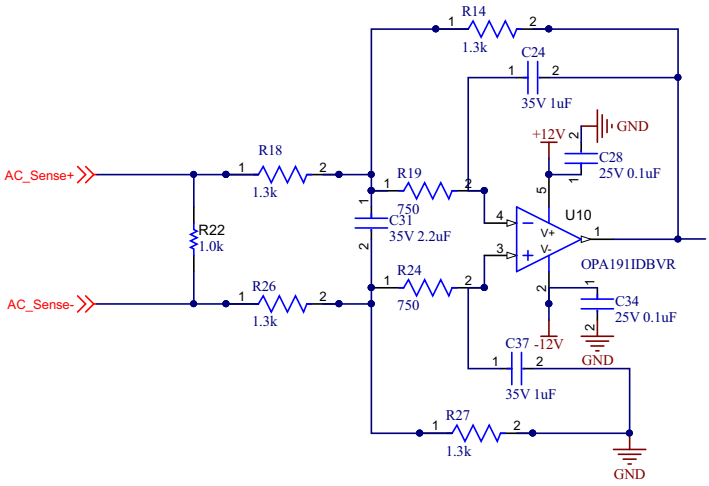


図 2-12. Differential to Single-Ended Schematic

2.2.4.7 Low-Pass Filter

The low-pass filter is optimized to attenuate auto-oscillation frequencies. The goal is to reduce noise to prevent false trips. This design has a gain of 20 dB at 0 Hz and a cutoff frequency of 70 Hz. The auto-oscillation frequency depends on many variables: magnetic core material, burden resistance, and the auto-oscillation signal chain. This design with a nanocrystalline core material results an oscillation around 800 Hz. The low-pass filter is optimized to attenuate noise created by the auto-oscillation circuit.

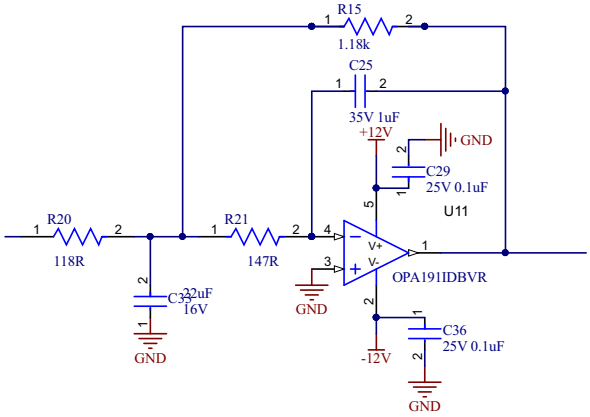


図 2-13. Low-Pass Filter Schematic

2.2.4.8 Full-Wave Rectifier

The full-wave rectifier only flips negative voltage to positive. The full-wave rectifier allows the same trip threshold for negative and positive fault current. The other reason for using the full-wave rectifier is to convert the negative polarity of the signal to positive voltage within the input range of the ADC of the MCU and prevent Electrical Overstress (EOS).

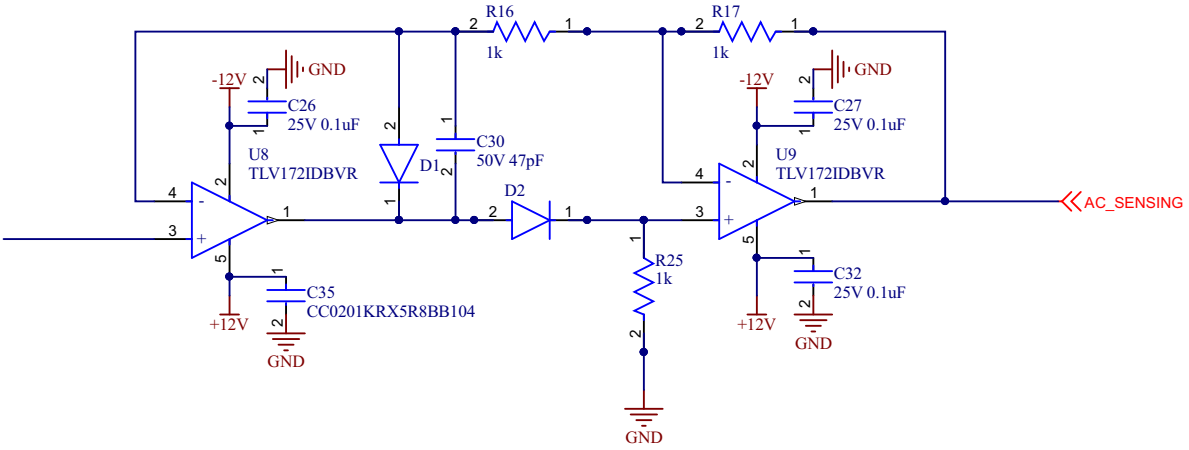


図 2-14. Full-Wave Rectifier Schematic

This precision full-wave rectifier can turn alternating current (AC) signals to single polarity signals. The op amps, U8 and U9, buffer the input signal and compensate for the voltage drops across D1 and D2 allowing for small signal inputs. The circuit is used in this application to quantify the absolute value of input signals which have both positive and negative polarities.

This topology was chosen over other full-wave rectifier topologies for the simplicity while achieving the desired performance. U1A and U1B control the biasing of D1 and D2 to change the signal path based on the polarity of the input signal achieving the full-wave rectification. The input impedance of the circuit is set by the termination resistor R4 and can be set to match the source impedance or as high as the input impedance of the U1A amplifier.

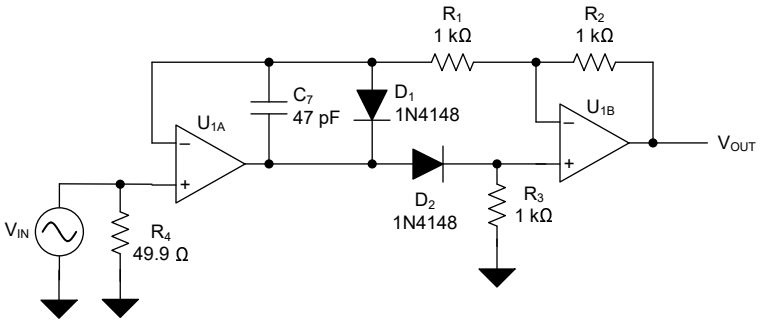


図 2-15. Circuit Schematic

図 2-16 and 式 62 show the circuit schematic and transfer function for positive input signals. Positive input signals reverse-bias D1 and forward-bias D2 making the components act like an open circuit and short circuit, respectively. In this configuration, the U1A amplifier drives the non-inverting input of U1B such that the voltage at the inverting input of U1A is equal to V_{IN}. Because current does not flow into the high-impedance inverting input of U1A, there is no current through R1 or R2 and U1B acts as a buffer. U1A must therefore also act as a buffer and V_{OUT} is simply equal to V_{IN}.

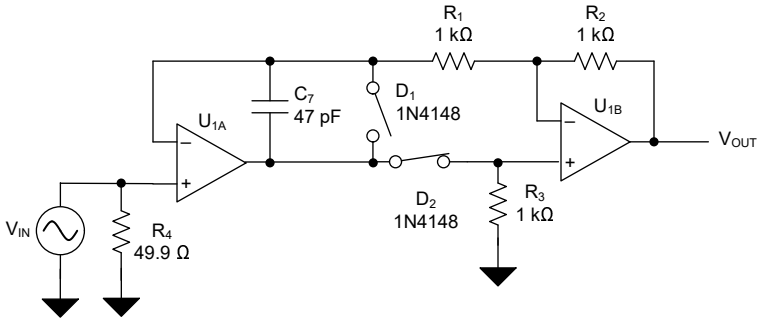


図 2-16. Simplified Circuit for Positive Input Signals

$$V_{OUT} = V_{IN} \tag{62}$$

図 2-17 and 式 63 show the circuit and transfer function for negative inputs. Negative input signals forward bias D1 and reverse bias D2. Therefore, U1A drives U1B like a standard inverting amplifier while R3 biases the non-inverting node of U1B to GND. In this configuration, the output is now positive for negative input signals achieving the full-wave rectification.

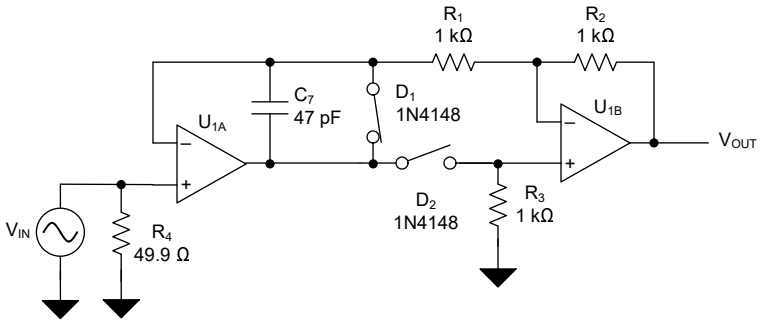


図 2-17. Simplified Circuit for Negative Input Signals

$$\frac{V_{OUT}}{V_{IN}} = \left(-\frac{R_2}{R_1}\right) \tag{63}$$

$$\frac{V_{OUT}}{V_{IN}} = -1\frac{V}{V} \tag{64}$$

2.2.4.9 MCU Selection

For this design, the MSP430F5131 MCU is chosen for the high clock speed required for timer capture DC fault detection. The timer capture method directly measured duty cycle changes by triggering a timer on each duty cycle edge, so a high clock speed was required. This timer capture method is used in many existing RCD modules. Alternatively, a lower BOM cost is possible by reading DC fault with an ADC instead of using the timer capture method.

The most important specification of MCU selection is the integrated ADC. The ADC must have an effective resolution small enough to consistently differentiate between a fault. This design sees a 200-mV filter output during a 6-mA DC fault, and 600-mV maximum filter output during an 30-mA_{RMS} AC fault[1]. This design uses a 10-bit ADC with a full scale range of 1.5 V integrated in the MSP430F5131 MCU.

The ADC needs a sample speed faster than 2000 samples per second. The software stores the low value read by the ADC and uses the low value to determine if an AC or DC fault occurred. The ADC must sample quickly enough to consistently detect a low value during an AC waveform to differentiate AC versus DC fault.

The largest source of noise is the ADC reference voltage error. This design has a total reference voltage error of 1.5%. The fault detection signal needs to be amplified as much as possible to make this error less significant.

[1] These fault threshold values can be increased by increasing the gain of the filter stage.

2.3 Highlighted Products

2.3.1 UCC28742

The UCC28742 is a flyback power-supply controller which provides high-performance voltage regulation using an optically coupled feedback signal from a secondary-side voltage regulator. The device provides accurate constant-current regulation using primary-side feedback. The controller operates in discontinuous-conduction mode (DCM) with valley-switching to minimize switching losses and allow for the use of low cost output rectifiers. The control law scheme combines frequency with primary peak-current amplitude modulation to provide high conversion efficiency across the load range. The control law provides a wide dynamic operating range of output power which allows the power-supply designer to achieve low standby power dissipation. During low-power operating conditions, the power-management features of the controller reduce the device operating current at switching frequencies below 25 kHz. At and above this frequency, the UCC28742 includes features in the modulator to reduce the EMI peak energy of the fundamental switching frequency and harmonics. A complete low-cost and low component-count system is realized using a straight-forward design process.

2.3.2 TLV1805

The TLV1805 comparator features rail-to-rail inputs with a push-pull output stage that operates at supply voltages as high as 40 V or ±20 V. The rail-to-rail input stage enables detection of signals close to the supply and ground while the push-pull output stage creates fast transition edges to either supply rail. A low supply current of 135 µA per channel with small, space-saving packages, makes these comparators versatile for use in a wide range of applications, from portable to industrial.

2.3.3 DRV8220

DRV8220 is an integrated H-bridge driver with multiple control interface options: PWM (IN1, IN2) interface (DRL and DSG packages), PH/EN (DSG only), or half-bridge interface (DSG only). To reduce area and external components on a printed circuit board, the device integrates a charge pump regulator and its capacitors. Both DSG and DRL packages support a timed auto-sleep mode which reduces microcontroller GPIO connections by eliminating a disable/sleep pin and automatically putting the device into a low-power sleep mode when the inputs remain inactive for 1-2 ms. When using autosleep for PWM or PH/EN mode, the nSLEEP pin can be tied high. The nSLEEP pin allows the device to be put to sleep in half-bridge mode where autosleep is not available.

2.3.4 ISO1212

The ISO1211 and ISO1212 devices are fully-integrated, isolated digital-input receivers with IEC 61131-2 Type 1, 2, and 3 characteristics. The devices receive 24-V to 60-V digital-input signals and provide isolated digital outputs. No field-side power supply is required. An external resistor, R_{SENSE}, on the input-signal path precisely sets the limit for the current drawn from the field input based on an internal feedback loop. The voltage transition thresholds are compliant with Type 1, 2, and 3 and can be increased further using an external resistor, R_{THR}.

The ISO121x devices use an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage.

2.3.5 ADC122S051

The ADC122S051 and ADC122S051Q devices are low-power, two-channel CMOS 12-bit analog-to-digital converters with high-speed serial interface. Unlike the conventional practice of specifying performance at a single sample rate only, the ADC122S051 and ADC122S051Q is fully specified over a sample rate range of 200 ksps to 500 ksps. The converter is based on a successive-approximation register architecture with an internal track-and-hold circuit. It can be configured to accept one or two input at inputs IN1 and IN2.

2.3.6 TPS7A39

The TPS7A39 device is a dual, monolithic, high PSRR, positive and negative low-dropout (LDO) voltage regulator capable of sourcing (and sinking) up to 150 mA of current. The regulated outputs can be independently and externally adjusted to symmetrical or asymmetrical voltages, making this device an ideal dual, bipolar power supply for signal conditioning. Both positive and negative outputs of the TPS7A39 ratiometrically track each other during start-up to mitigate floating conditions and other power-supply sequencing issues common in dual-rail systems. The negative output can regulate up to 0 V, extending the common-mode range for single-supply

amplifiers. The TPS7A39 also features high PSRR to eliminate power-supply noise, such as switching noise, that can compromise signal integrity.

2.3.7 TPS7A20

The TPS7A20 is an ultra-small, low-dropout (LDO) linear regulator that can source 300 mA of output current. The TPS7A20 is designed to provide low noise, high PSRR, and excellent load and line transient performance that can meet the requirements of RF and other sensitive analog circuits. Using remarkable design techniques, the TPS7A20 offers an ultra-low noise performance without the addition of a noise bypass capacitor. The TPS7A20 also provides the advantage of low quiescent current, which can be good for battery-powered applications. With an input voltage range of 1.6 V to 6.0 V and an output range of 0.8 V to 5.5 V, the TPS7A20 can be used for a wide variety of applications. The device uses a precision reference circuit to provide a maximum accuracy of 1.5% over load, line, and temperature variations.

2.3.8 ATL431

The ATL431 and ATL432 are three-terminal adjustable shunt regulators, with specified thermal stability over applicable automotive, commercial, and industrial temperature ranges. The output voltage can be set to any value between Vref (approximately 2.5 V) and 36 V, with two external resistors. These devices have a typical output impedance of 0.05 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications, such as onboard regulation, adjustable power supplies, and switching power supplies.

2.3.9 TL431

The TL431 and TL432 devices are three-terminal adjustable shunt regulators, with specified thermal stability over applicable automotive, commercial, and military temperature ranges. The output voltage can be set to any value between Vref (approximately 2.5 V) and 36 V, with two external resistors. These devices have a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications, such as onboard regulation, adjustable power supplies, and switching power supplies. The TL432 device has exactly the same functionality and electrical specifications as the TL431 device, but has different pinouts for the DBV, DBZ, and PK packages.

2.3.10 TPS563210A

The TPS562210A and TPS563210A are simple, easy-to-use, 2-A, 3-A synchronous step-down converters in 8 pin SOT-23 package. The devices are optimized to operate with minimum external component counts and optimized to achieve low standby current. These switch mode power supply (SMPS) devices employ D-CAP2™ control mode providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

2.3.11 TPS55330

The TPS55330 is a monolithic nonsynchronous switching regulator with integrated 5-A, 24-V power switch. The device can be configured in several standard switching-regulator topologies, including boost, SEPIC, and isolated flyback. The device has a wide input voltage range to support applications with input voltage from multicell batteries or regulated 3.3- V, 5-V, and 12-V power rails. The TPS55330 regulates the output voltage with current mode pulse width modulation (PWM) control, and has an internal oscillator. The switching frequency of PWM is set by either an external resistor or by synchronizing to an external clock signal. The user can program the switching frequency from 100 kHz to 1.2 MHz.

2.3.12 TPS259470

The TPS25947xx family of eFuses is a highly integrated circuit protection and power management design in a small package. The devices provide multiple protection modes using very few external components and are a robust defense against overloads, short-circuits, voltage surges, reverse polarity and excessive inrush current. With integrated back-to-back FETs, reverse current flow from output to input is blocked at all times, making the devices a good choice for power MUX and ORing applications as well as systems which need load side energy hold up storage in case input power supply fails. The devices use linear ORing based scheme to make sure almost zero DC reverse current and emulate the best diode behavior with minimum forward voltage drop and power dissipation.

2.3.13 TL7705A

The TL77xxA family of integrated-circuit supply voltage supervisors is designed specifically for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input.

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware Requirements

図 3-1 shows the top view of the board and different sections of the TIDA-010239 PCB.

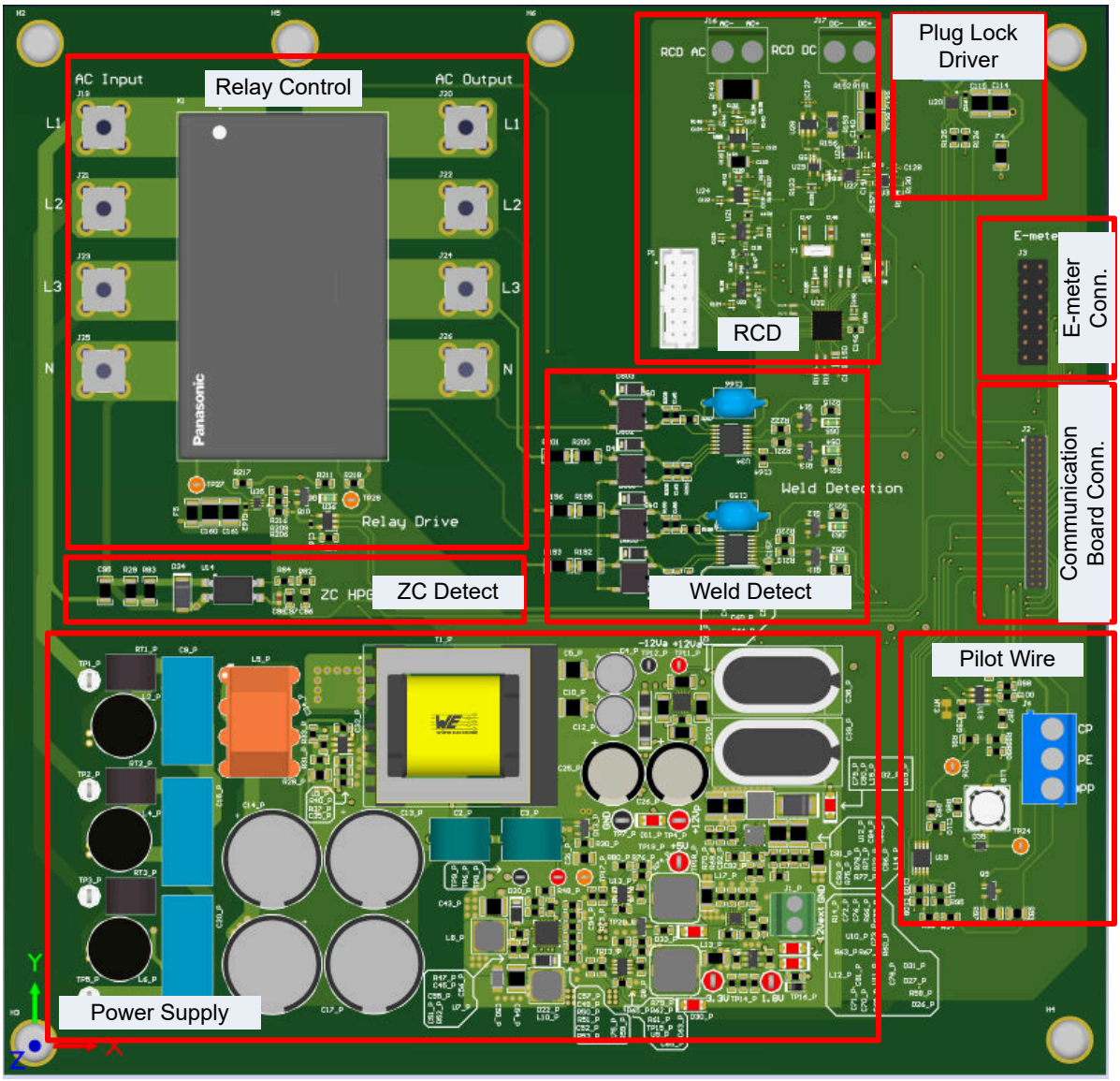


図 3-1. TIDA-010239 PCB Top View

3.2 Test Requirements

3.2.1 Power Supply Test Setup

図 3-2 shows a block diagram of the external component arrangement and final connections in the test setup.

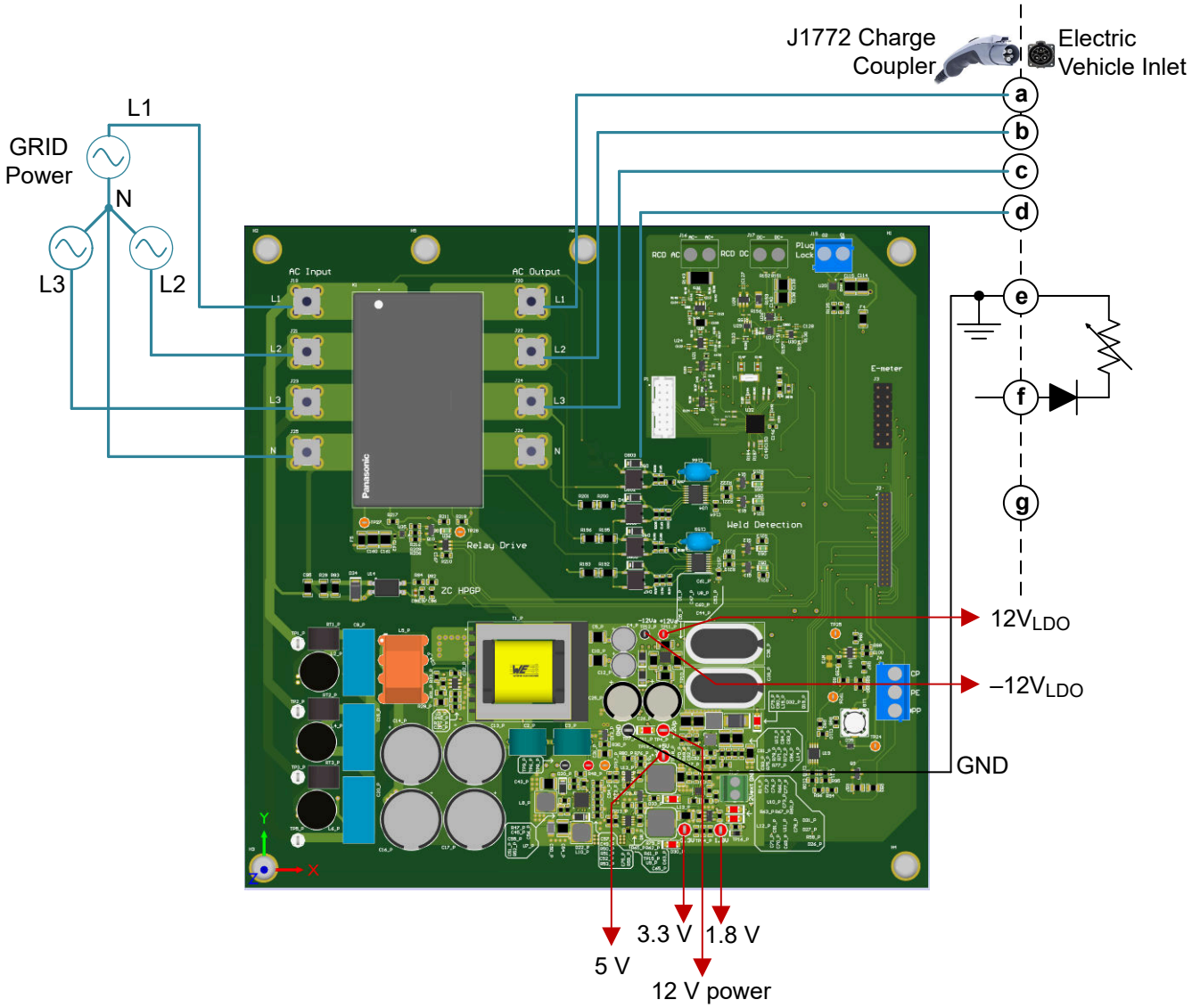


図 3-2. External Component Connections With TIDA-010239 Hardware

図 3-3 shows the test setup. The test setup for the linear regulator and converters consists of the TIDA-010239 board, DC supply, digital multimeter, electronic load, voltage and current probe.

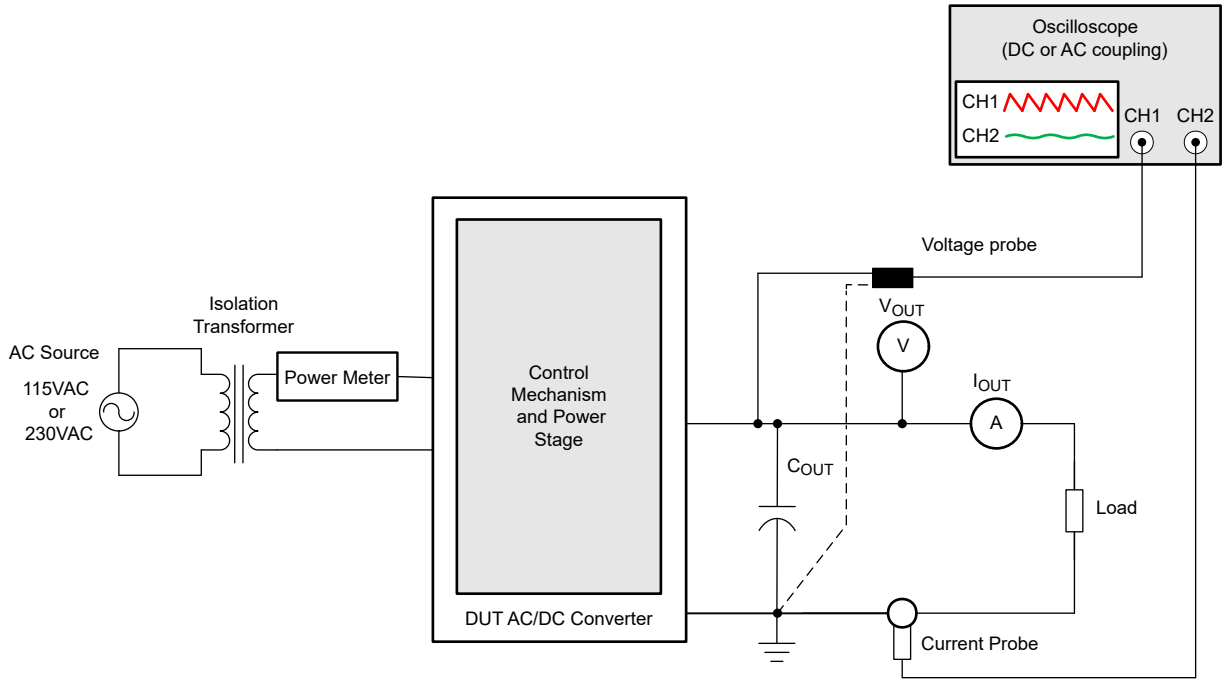


図 3-3. Test Setup for Linear Regulator and Converters in TIDA-010239

注

- DUT is Device Under Test.
- The oscilloscope analog signal bandwidth requires greater than 400 times the switching frequency.
- The oscilloscope requires higher memory depth and sampling rate to capture ripple waveform accurately (at least 4 GSPS, memory depth > 1Mpts).
- Oscilloscope probe terminated to 50 Ω.

The tests conducted for this design are as follows:

- Device efficiency and system efficiency at various loads
- Ripple voltage, ripple frequency at full and light load conditions, output voltage accuracy
- Load transient response

3.2.2 Weld Detect Test Setup

Overview:

- The system checks for the AC signal via ISO1212 when the relay is open. A normal (unwelded) condition means there are not any output pulses.
- The system checks for the AC signal via ISO1212 when the relay is closed. A normal (AC present) condition means there are no output pulses.

Complete the following work before powering the TIDA-010239 board.

Connect the *AM62_R_ENABLE* (pin 36, J2) to 3.3V (TP14_P) to enable the K1 relay at power up.

- Connect oscilloscope probe 1 to LINE1_IN (TP1_P). There is no need to connect the probe 1 reference clip.
- Connect oscilloscope probe 2 to RELAY_CHECK_L1 (J2). Connect the probe 2 reference clip to PGND (TP7_P).
- Connect oscilloscope probe 3 to RELAY_CHECK_L2 (J2). There is no need to connect the probe 3 reference clip.
- Connect oscilloscope probe 4 to RELAY_CHECK_L3 (J2). There is no need to connect the probe 4 reference clip.

注

1. The oscilloscope reference clip is tied to earth GND by default and for this test setup the reference clip was connected to PGND. This technically removes the functional isolation of the circuit but does make the functional testing easier. If isolated measurement is required, an isolation transformer can be used to power the scope.
2. RELAY_CHECK_N (J2) can also be checked if there is more than 4 channels.

Powering the board for measurement:

- Apply an external 12-V (500 mA) power supply to J1_P so that the relay can be enabled before turning on the AC line power. This prevents potential arcing when you enable the relay. Normally, AC zero crossing detection is required before operating the relay. In this case, we are testing with manual relay control.
- With the relay already closed, turn on the AC line power supply (240 V_{RMS}) and observe the waveforms on the scope.
- When finished, turn off the AC line power first before removing the 12-V supply. The backup supercapacitor can keep the relay closed for a while even when the AC line power is disconnected.
- The measurement can be repeated with the relay open by disconnecting the *AM62_R_ENABLE* from 3.3V.

3.3 Test Results

3.3.1 Isolated AC/DC Power Supply Based on UCC28742

This section shows test data for efficiency over full scale load variation, output voltage regulation, output ripple, cross regulation, and transient load response waveforms, as well as thermal performance. For all measurements shown in the screenshots, VAC was set to 115 V_{RMS}, 60 Hz with the oscilloscope set to 20-MHz bandwidth and in AC coupling (for the voltage ripple measurements).

注

- +12 V is the 12-V power output (TP4_P) here called also as “12-Vp, where *p* stands for *power*.
- +12 Va is the low noise +12-V out of U8_P.
- –12 Va is the low noise -12-V out of U8_P.
- 5 V and 3.3 V are the outputs of U9 and U13 buck converters.

3.3.1.1 Efficiency and Output Voltage Cross Regulation

Total zero-load current power consumption (all outputs active, ultra-capacitor charged):

- 115 VAC, 60 Hz: 485 mW
- 230 VAC, 50 Hz: 548 mW

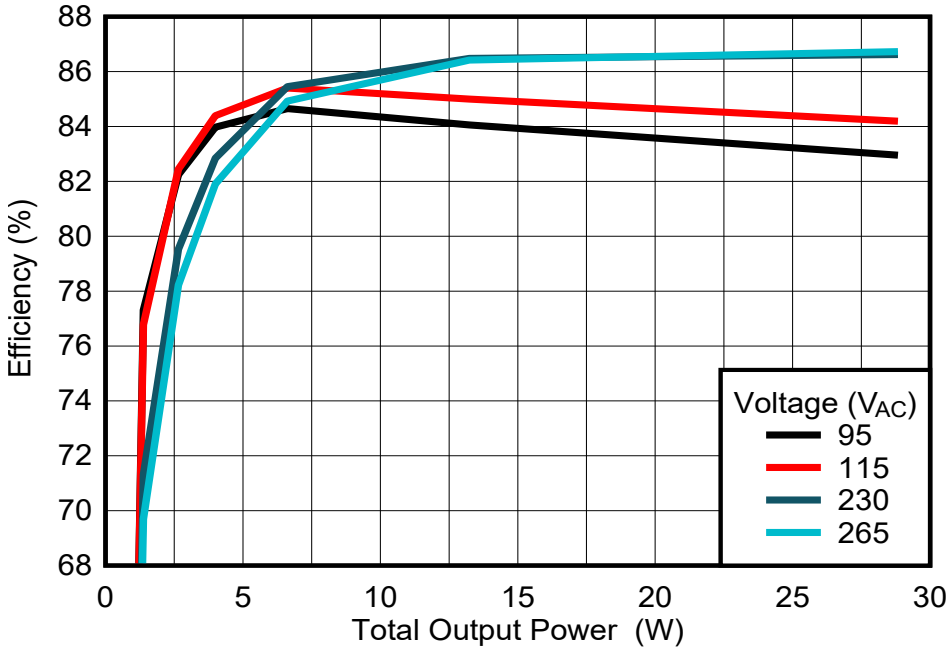


図 3-4. Output Power vs Efficiency at 95 V and 115 V AC, 60 Hz; 230 V and 265 V AC, 50 Hz

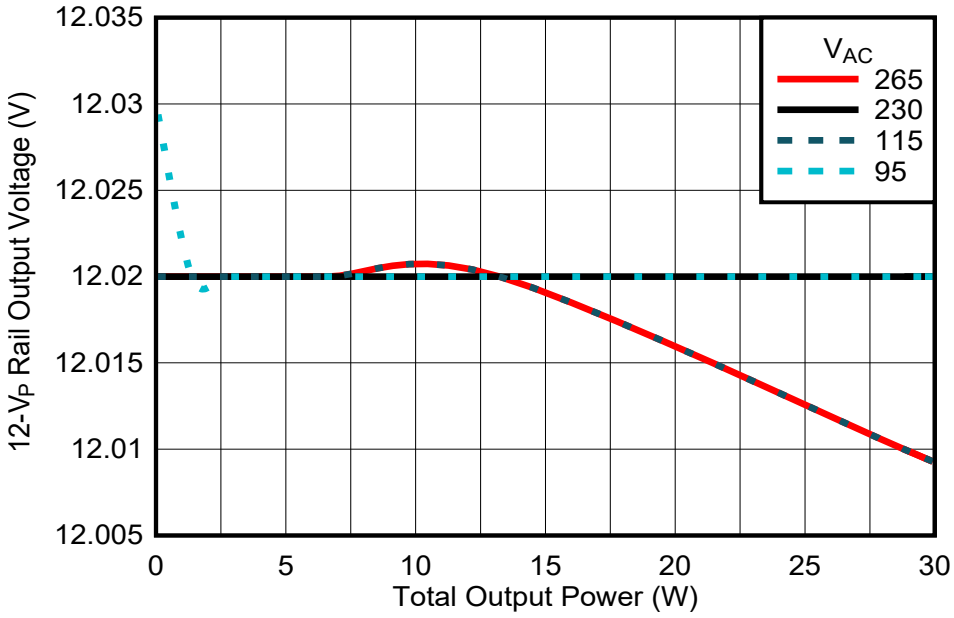


図 3-5. Output Power vs Voltage Regulation

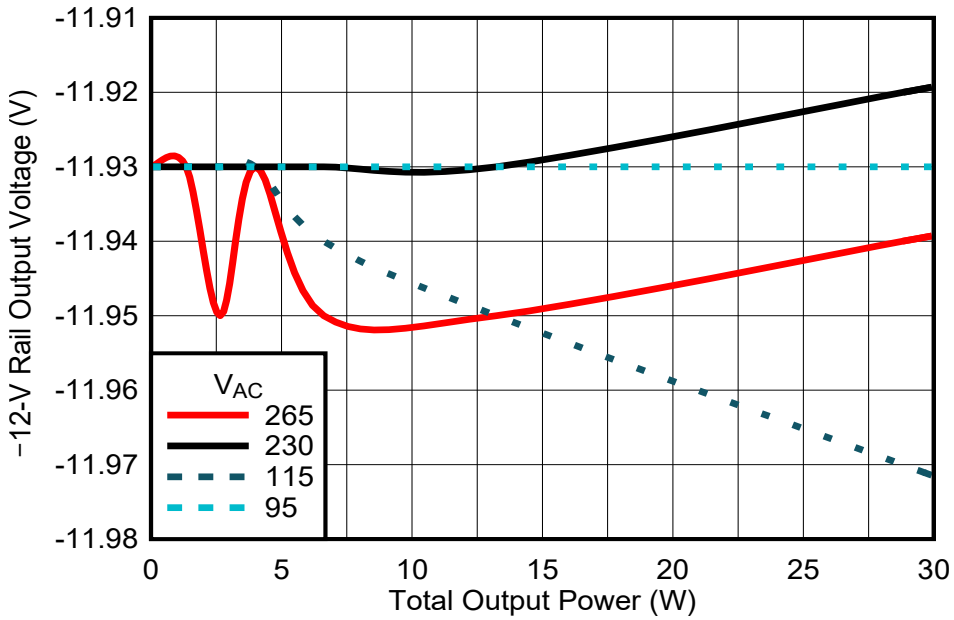


図 3-6. Output Power vs Voltage Regulation

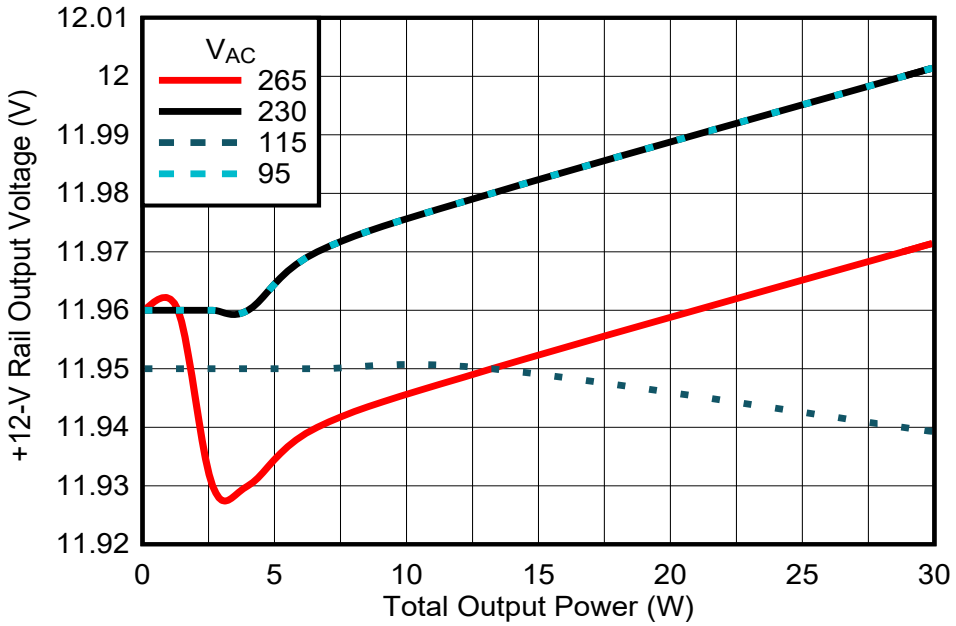


図 3-7. Output Power vs Voltage Regulation

表 3-1. Test Data at 95 VAC, 60 Hz AC Input

P_{IN} (W)	12 Vp (V)	+12 V (V)	–12 V (V)	I(12 Vp) (mA)	I(+12 V) (mA)	I(–12 V) (mA)	P_{OUT} (W)	Efficiency (%)
0.209	12.03	11.96	–11.93	0.00	0.00	0.00	0.00	0.00%
1.782	12.02	11.96	–11.93	104.7	4.98	–4.97	1.38	77.30%
3.225	12.02	11.96	–11.93	200.9	9.97	–9.94	2.65	82.24%
4.759	12.02	11.96	–11.93	302.8	14.95	–14.91	4.00	83.97%
7.821	12.02	11.97	–11.93	501.3	24.94	–24.85	6.62	84.65%
15.745	12.02	11.98	–11.93	1002.0	49.92	–49.71	13.24	84.06%
34.754	12.02	12.00	–11.93	2200.0	100.00	–99.42	28.83	82.95%

表 3-2. Test Data at 115 VAC, 60 Hz AC Input

P_{IN} (W)	12 Vp (V)	+12 V (V)	–12 V (V)	I(12 Vp) (mA)	I(+12 V) (mA)	I(–12 V) (mA)	P_{OUT} (W)	Efficiency (%)
0.216	12.02	11.95	–11.93	0.00	0.00	0.00	0.00	0.00%
1.753	12.02	11.95	–11.93	102.1	4.98	–4.97	1.35	76.78%
3.219	12.02	11.95	–11.93	201.0	9.96	–9.94	2.65	82.45%
4.735	12.02	11.95	–11.93	302.8	14.94	–14.91	4.00	84.39%
7.752	12.02	11.95	–11.94	501.3	24.90	–24.88	6.62	85.40%
15.570	12.02	11.95	–11.95	1002.0	49.79	–49.79	13.23	85.00%
34.213	12.01	11.94	–11.97	2200.0	99.50	–99.75	28.80	84.19%

表 3-3. Test Data at 230VAC, 50 Hz AC Input

P_{IN} (W)	12 Vp (V)	+12 V (V)	–12 V (V)	I(12 Vp) (mA)	I(+12 V) (mA)	I(–12 V) (mA)	P_{OUT} (W)	Efficiency (%)
0.308	12.02	11.96	–11.93	0.00	0.00	0.00	0.00	0.00%
1.888	12.02	11.96	–11.93	102.1	4.98	–4.97	1.35	71.30%
3.337	12.02	11.96	–11.93	201.0	9.97	–9.94	2.65	79.53%
4.824	12.02	11.96	–11.93	302.8	14.95	–14.91	4.00	82.84%
7.748	12.02	11.97	–11.93	501.3	24.94	–24.85	6.62	85.45%
15.304	12.02	11.98	–11.93	1002.0	49.92	–49.71	13.24	86.48%
33.280	12.02	12.00	–11.92	2200.0	100.00	–99.33	28.83	86.62%

表 3-4. Test Data at 260VAC, 50 Hz AC Input

P_{IN} (W)	12 Vp (V)	+12 V (V)	–12 V (V)	I(12 Vp) (mA)	I(+12 V) (mA)	I(–12 V) (mA)	P_{OUT} (W)	Efficiency (%)
0.334	12.02	11.96	–11.93	0.00	0.00	0.00	0.00	0.00%
1.932	12.02	11.96	–11.93	102.1	4.98	–4.97	1.35	69.69%
3.391	12.02	11.93	–11.95	200.9	9.94	–9.96	2.65	78.22%
4.878	12.02	11.93	–11.93	302.8	14.91	–14.91	4.00	81.91%
7.795	12.02	11.94	–11.95	501.3	24.88	–24.90	6.62	84.93%
15.312	12.02	11.95	–11.95	1001.9	49.79	–49.79	13.23	86.42%
33.212	12.01	11.97	–11.94	2200.0	99.75	–99.50	28.80	86.73%

表 3-5. Output Voltage Cross Regulation at 115-V AC, 60-Hz AC Input

I(12 Vp) (mA)	I(+12 V) (mA)	I(–12 V) (mA)	12 Vp (V)	+12 V (V)	–12 V (V)
2000	100	100.00	12.09	11.95	–11.94
5	100	100.0	12.01	10.88	–10.88
2000	100	0.0	12.09	11.92	–11.93
2000	0	100.0	12.09	11.94	–11.95
50	100	100.0	12.10	11.95	–11.95
0	0	100.0	12.10	11.94	–10.76
0	0	0.0	12.10	11.94	–11.91
0	100	0.0	12.10	10.48	–11.88
2000	0	0.0	12.09	11.94	–11.91

3.3.1.2 Efficiency and Output Voltage Regulation of TPS563210

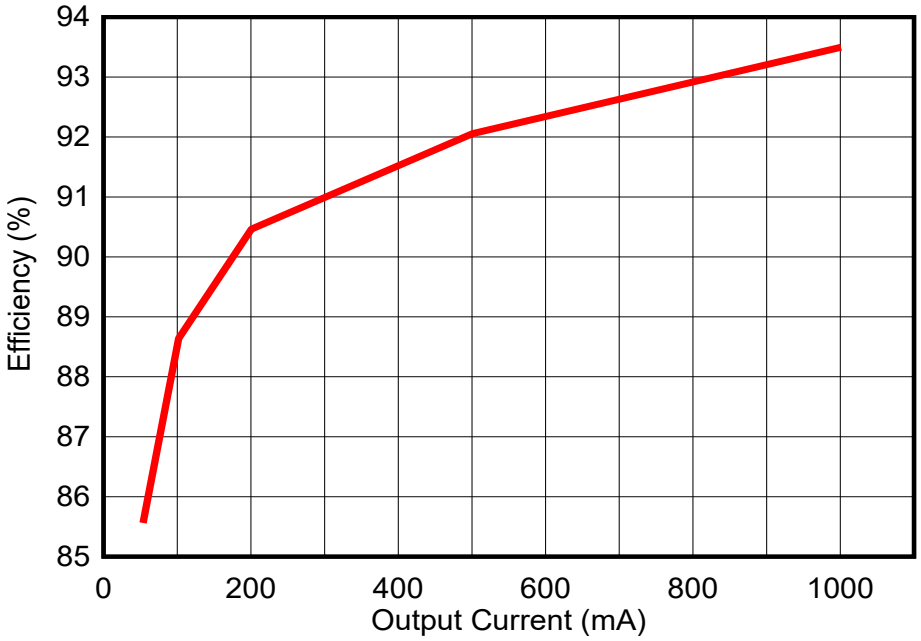


図 3-8. 5-V Output Current vs Efficiency

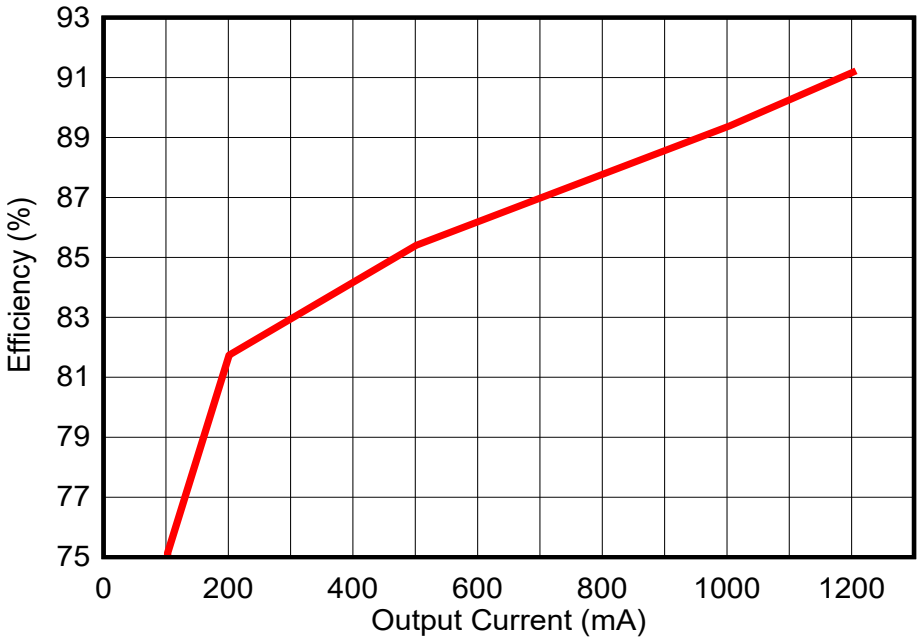


図 3-9. 3.3-V Output Current vs Efficiency

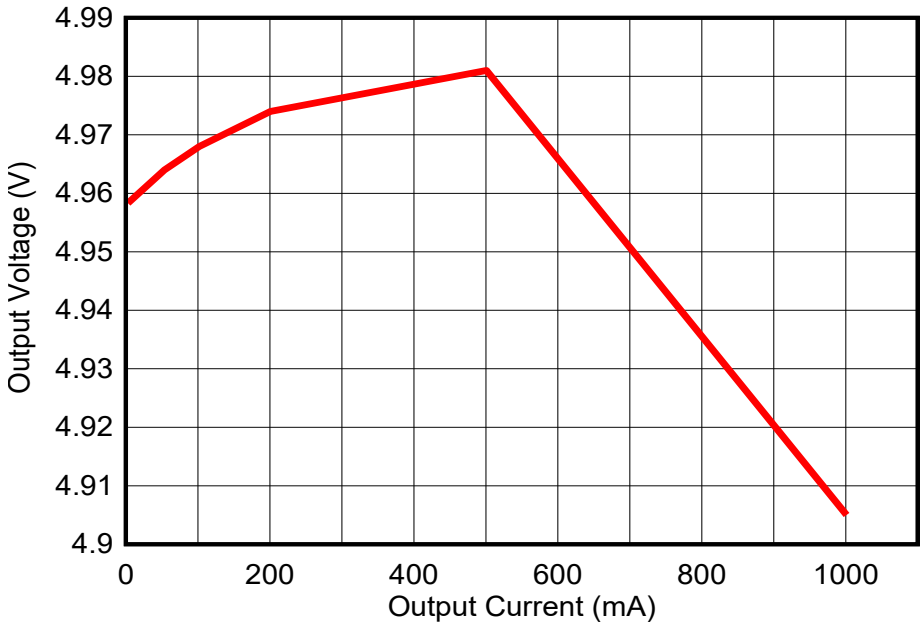


図 3-10. 5-V Output Current vs Voltage Regulation

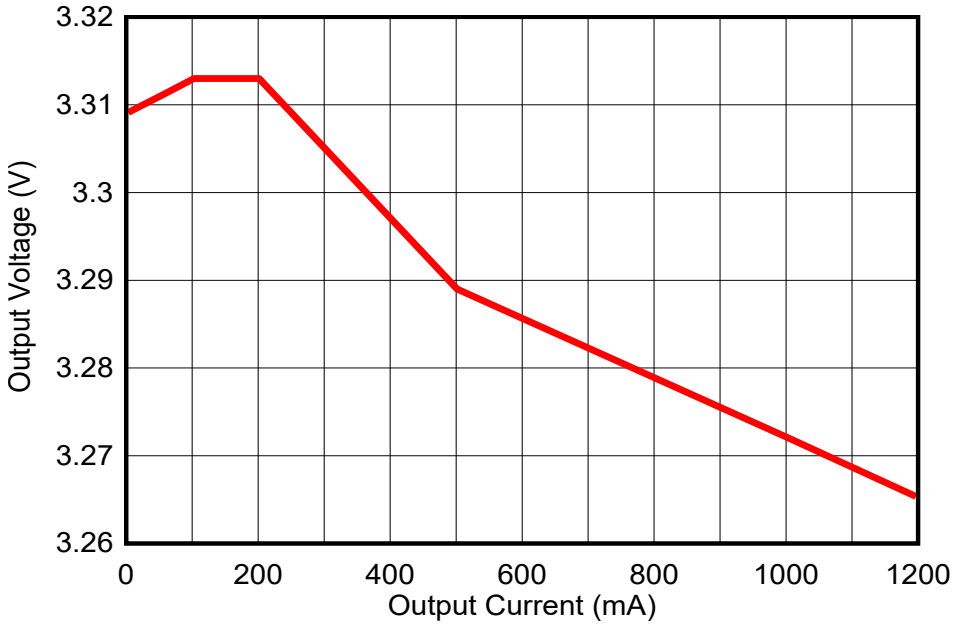
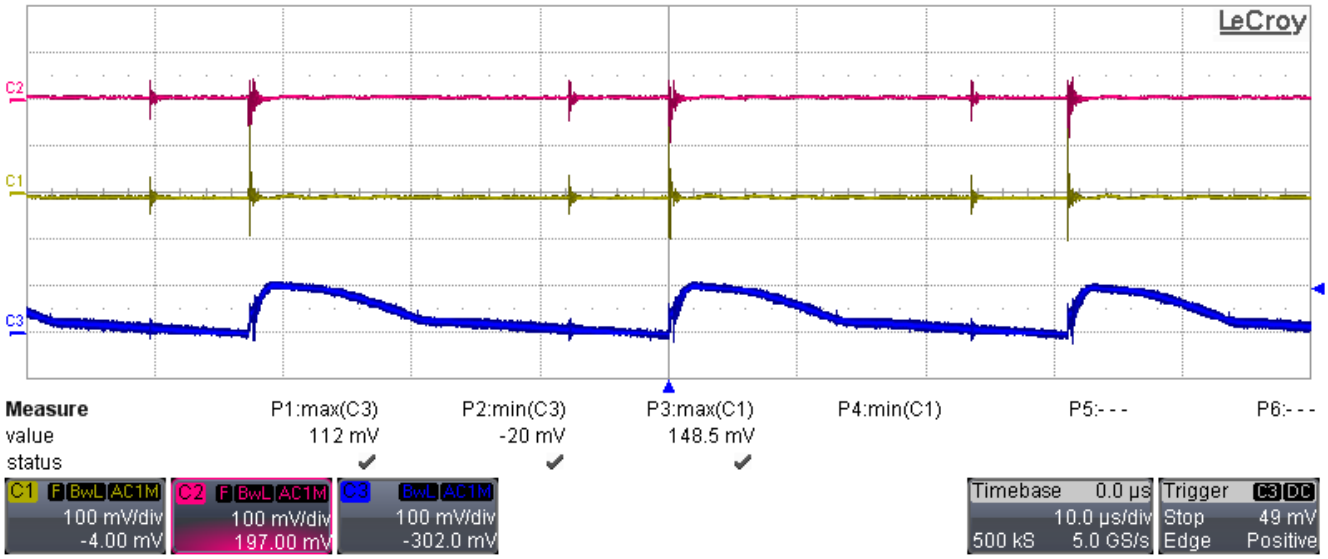


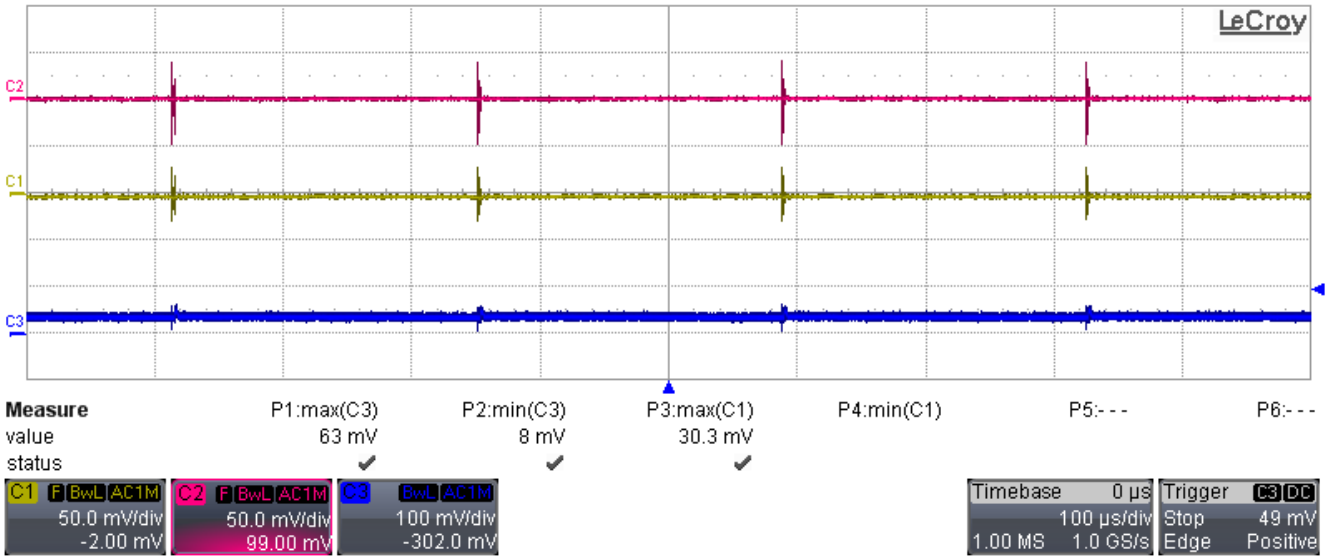
図 3-11. 3.3-V Output Current vs Voltage Regulation

3.3.1.3 Output Voltage Ripple Waveforms



In detail: C1 is –12-V output at 100 mA, C2 is +12-V output at 100 mA, C3 is +12 Vp at 2.2 A.

図 3-12. Voltage Ripple on –12 V, +12 V and +12 Vp at Full Load



In detail: C1 is –12-V output at 0 mA, C2 is +12-V output at 0 mA, C3 is +12 Vp at 0 A.

図 3-13. Voltage Ripple on –12 V, +12 V and +12 Vp at No Load

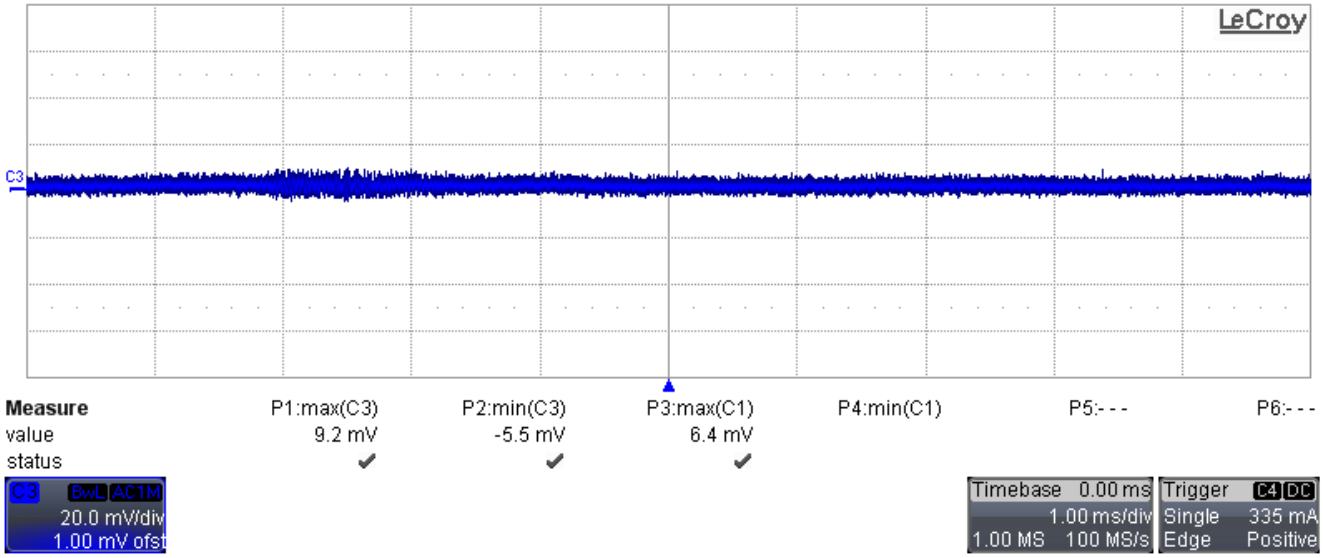


図 3-14. Voltage Ripple on 3.3 V_{OUT} at 1 A (1 ms/div)

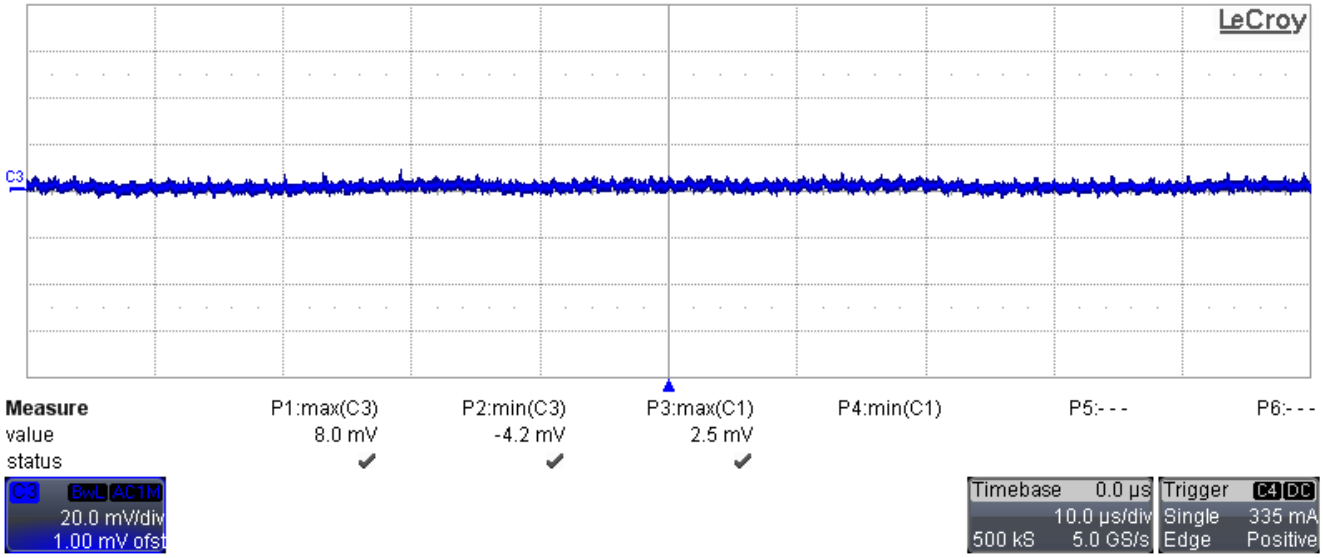


図 3-15. Voltage Ripple on 3.3 V_{OUT} at 1 A (10 µs/div)

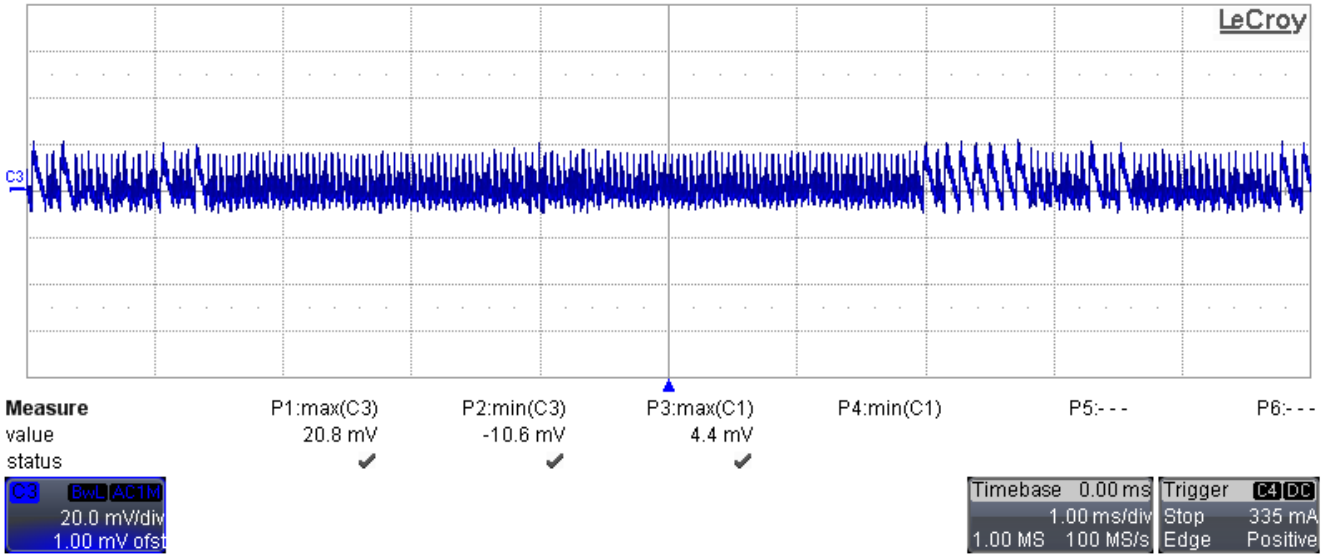


図 3-16. Voltage Ripple on 3.3 V_{OUT} at 5-mA Load Current

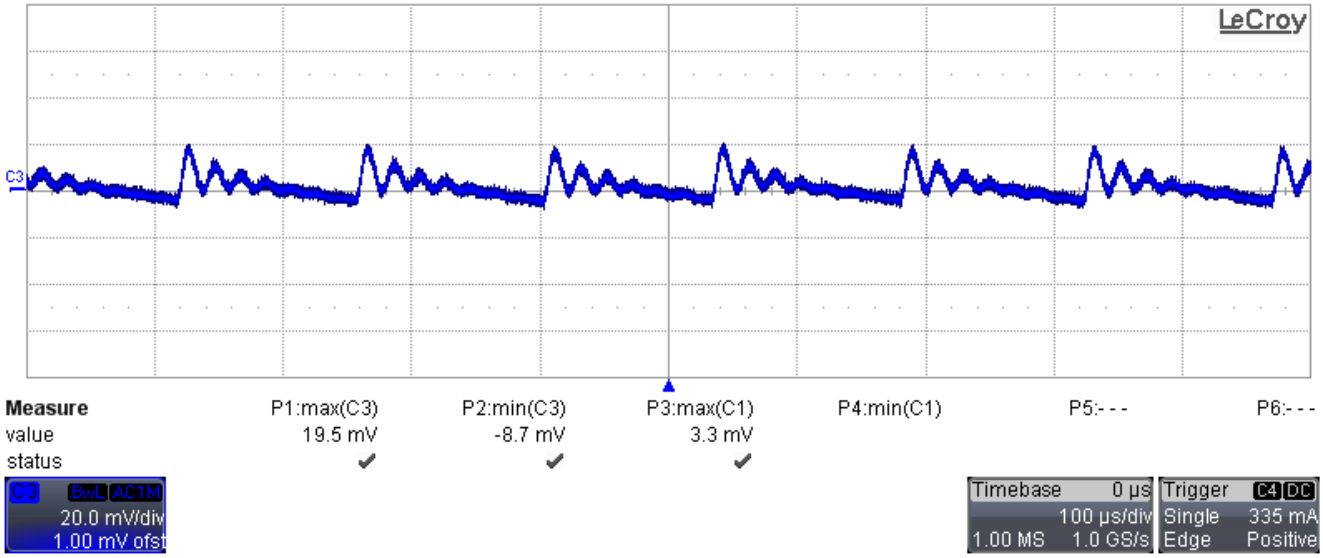


図 3-17. Voltage Ripple on 3.3 V_{OUT} at Zero Load Current

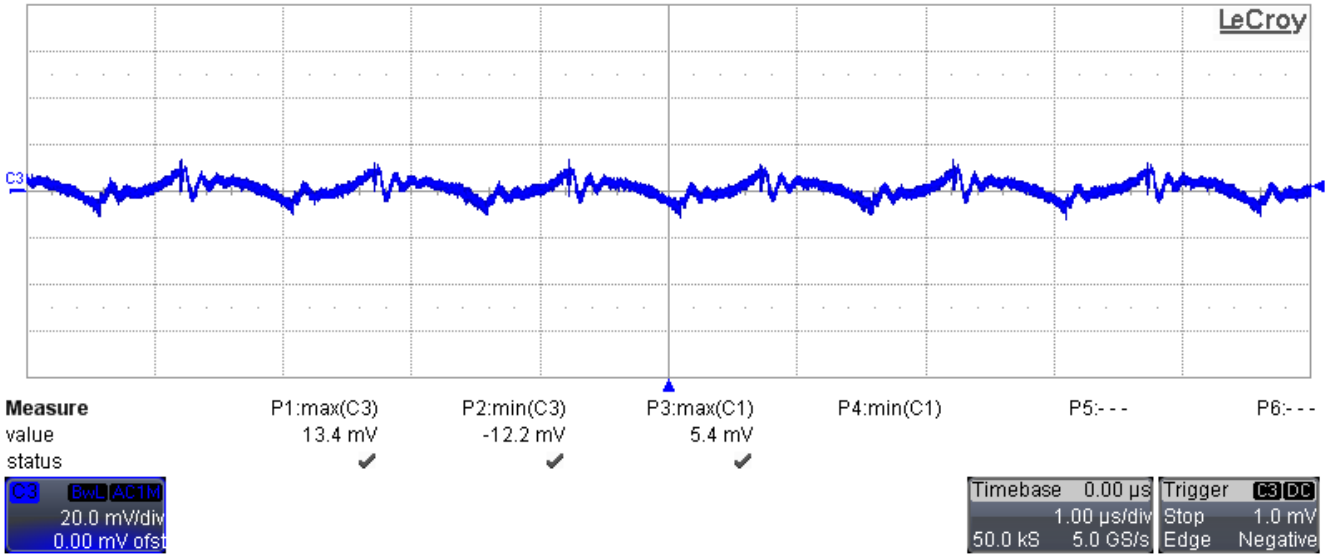


図 3-18. Voltage Ripple on 5 V_{OUT} at 1-A Load Current

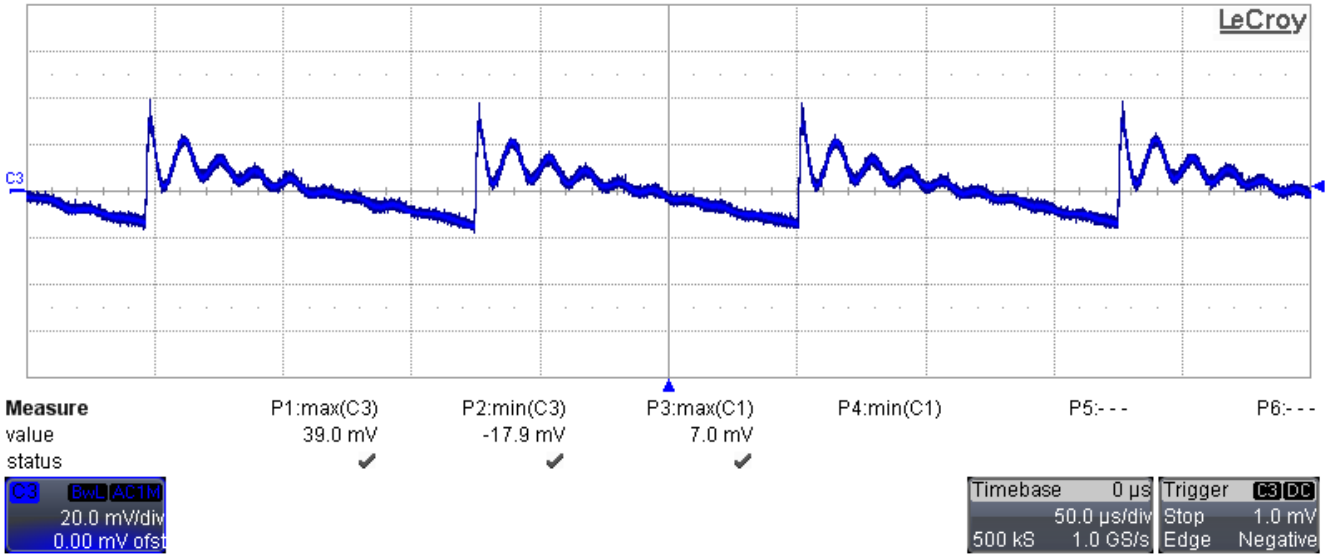


図 3-19. Voltage Ripple on 5 V_{OUT} at Zero Load Current

3.3.1.4 Start, Shutdown, Backup Power, and Transient Response Waveforms

図 3-20 shows the behavior of the converter during start-up (AC source turned on) with –12 V, +12 V and +12 Vp at full load. C1 is –12-V output at 100 mA, C2 is +12-V output at 100 mA, C3 is +12 Vp at 2.2 A.

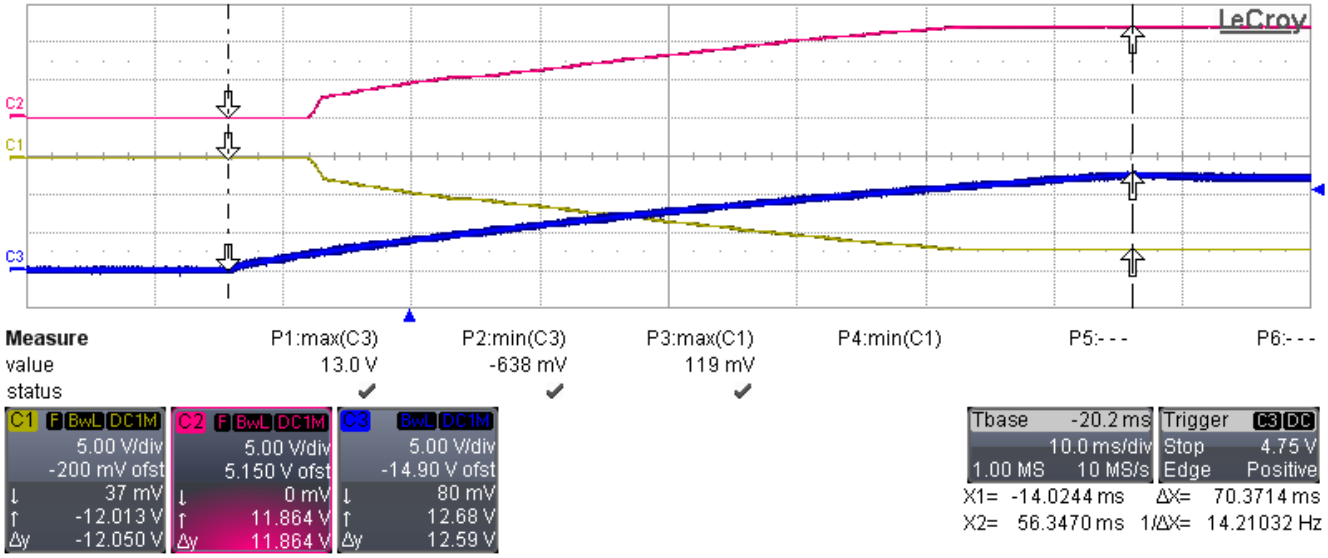


図 3-20. Behavior of the Converter During Start-Up

図 3-21 shows the behavior of the converter during shutdown (AC source disconnected) with –12 V, +12 V and +12 Vp at full load. C1 is –12-V output at 100 mA, C2 is +12-V output at 100 mA, C3 is +12 Vp at 2.2 A.

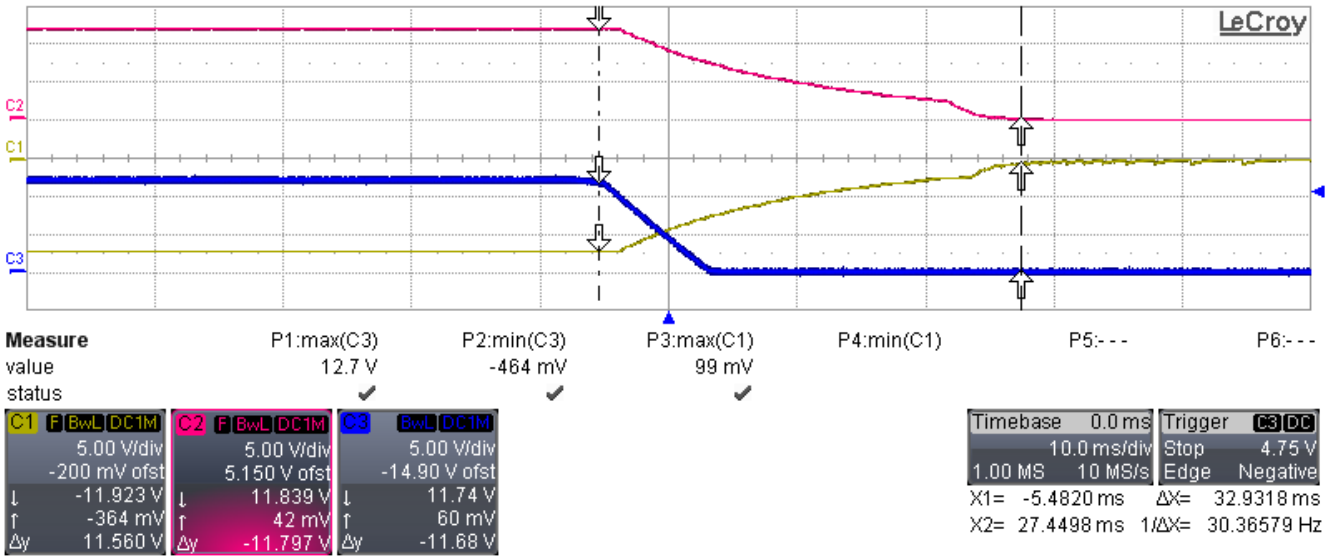


図 3-21. Behavior of the Converter During Shutdown

図 3-22 shows the behavior of the converter, loaded according to the specifications with 12 Vp at 0.44 A, and 5-V rail at 275 mA. Here the trace C2 is 12-Vp output (TP4_P), C1 is 5-V output and C4 is input VAC.

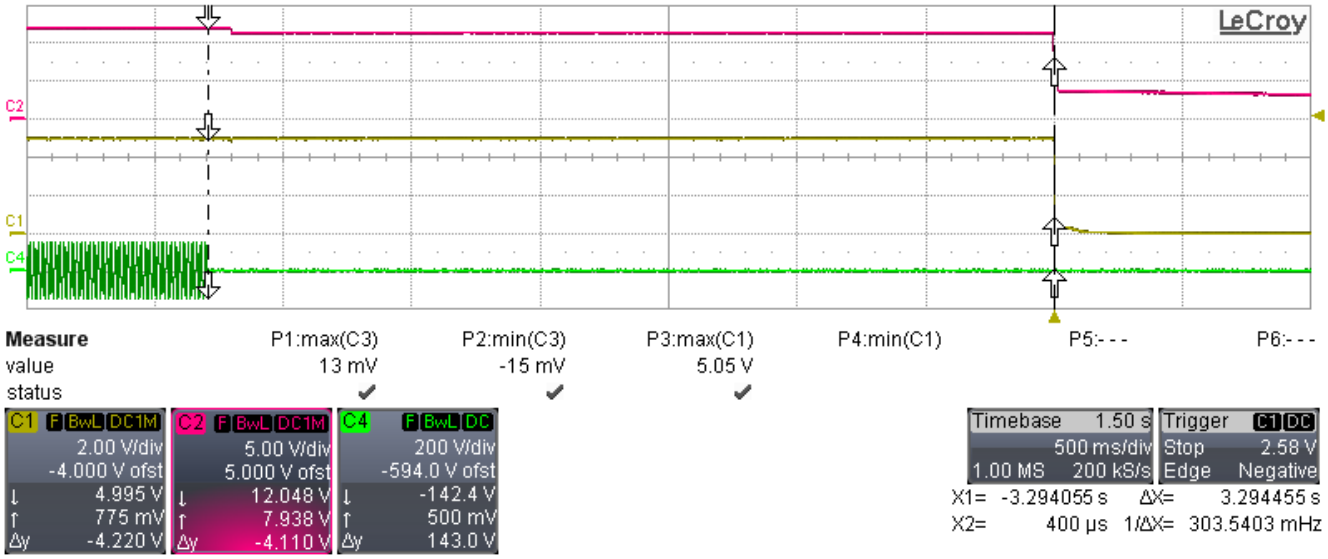


図 3-22. Backup Supply Behavior After AC Source is Disconnected

図 3-23 shows the transient response of the 5 V_{OUT} when switched between zero and 1 A load current.

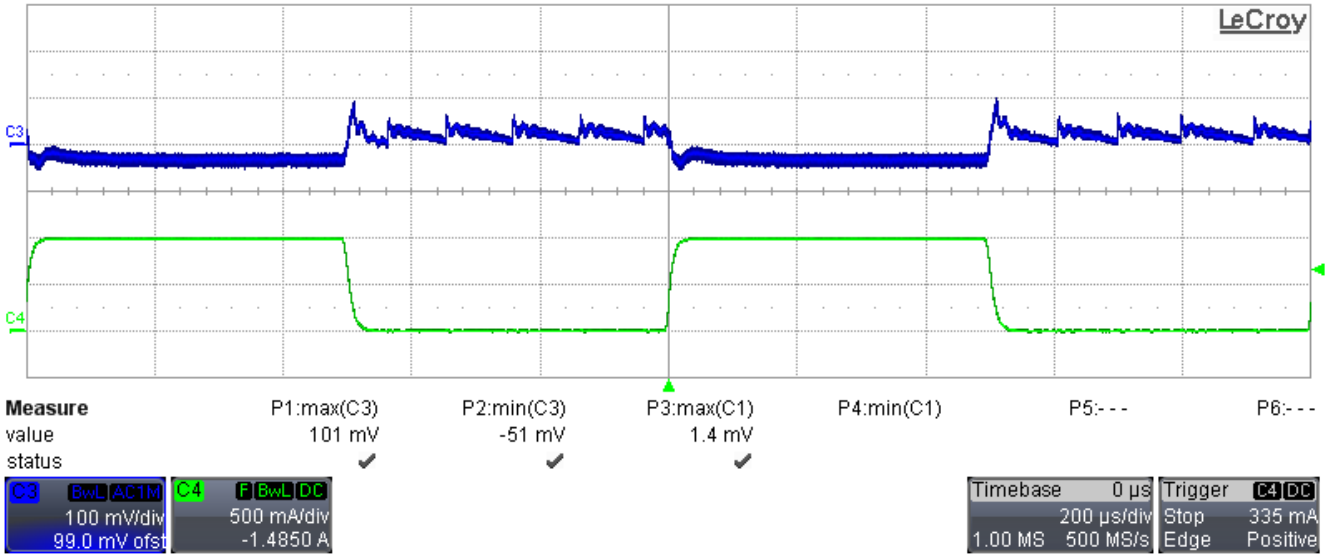


図 3-23. Transient on 5 V_{OUT} 0–1 A Load

図 3-24 shows the transient response of the 3.3 V_{OUT} when switched between zero and 1-A load current.

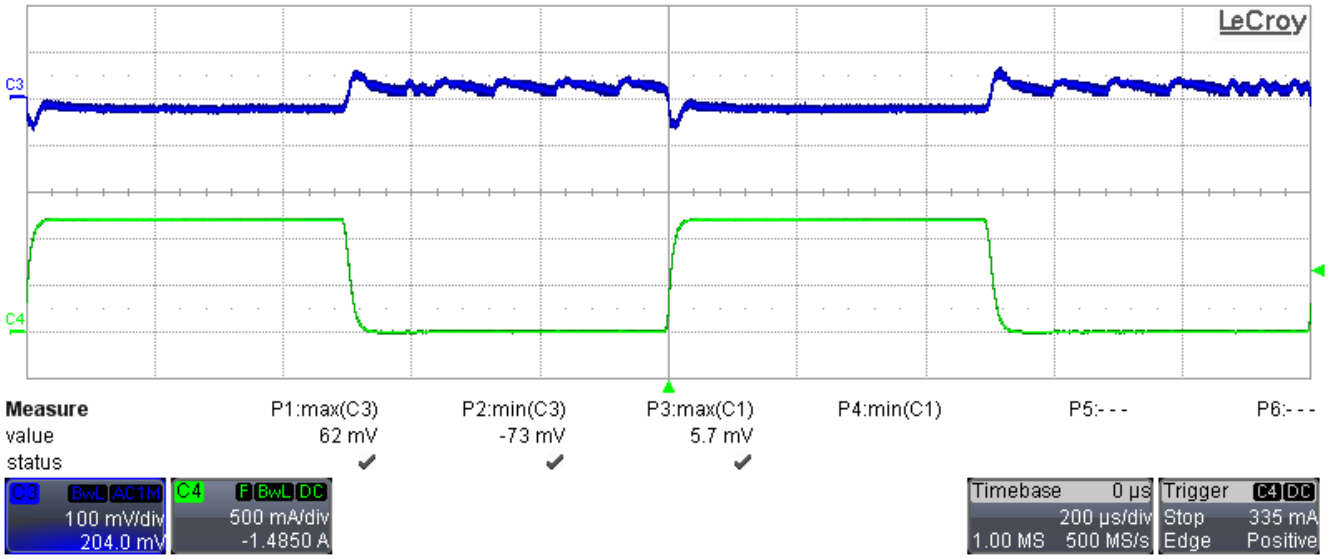


図 3-24. Transients on 3.3 V_{OUT} 0 A to 1 A

図 3-25 shows the transient response of the converter with zero to 2-A transients on 12 V_{OUT}, while 12 V and –12 V are loaded both at 100 mA. C1 is –12-V output at 100 mA, C2 is +12-V output at 100 mA, C3 is +12 Vp with switched load and C4 is the 12 Vp output current.

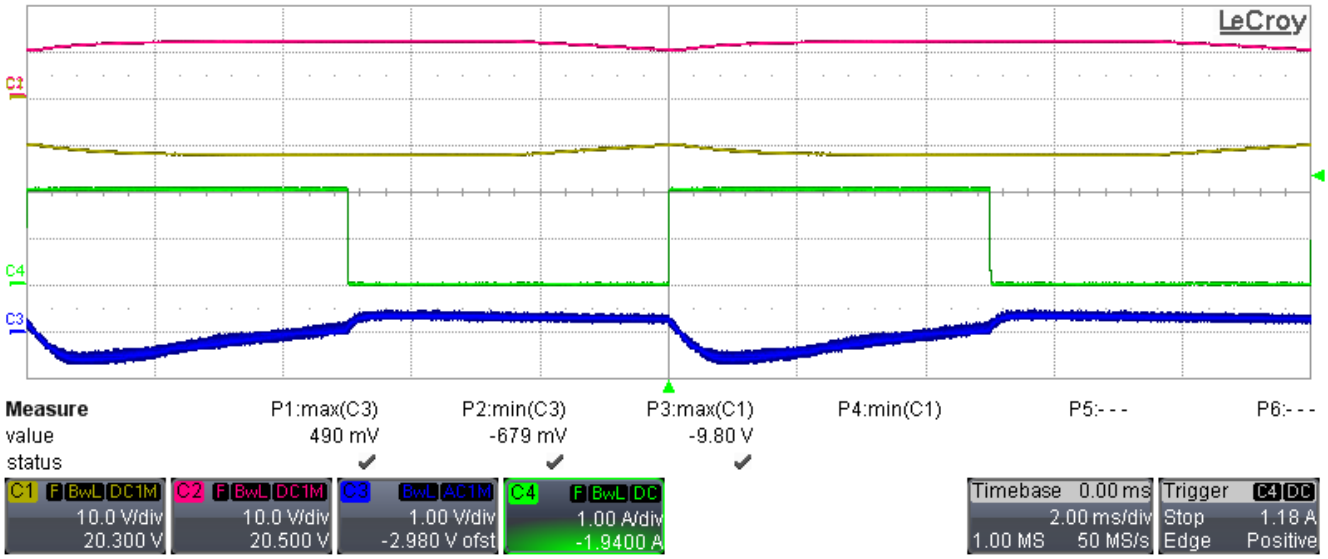


図 3-25. Transient Response of the Converter With Zero to 2-A Transients on 12 V_{OUT}

図 3-26 shows the transient response of the converter with zero to 2-A transients on 12 V_{OUT}, while 12 V and –12 V are both loaded at zero current. C1 is –12-V output at 0 mA, C2 is +12-V output at 0 mA, C3 is +12 Vp with switched load and C4 is the 12-Vp output current.

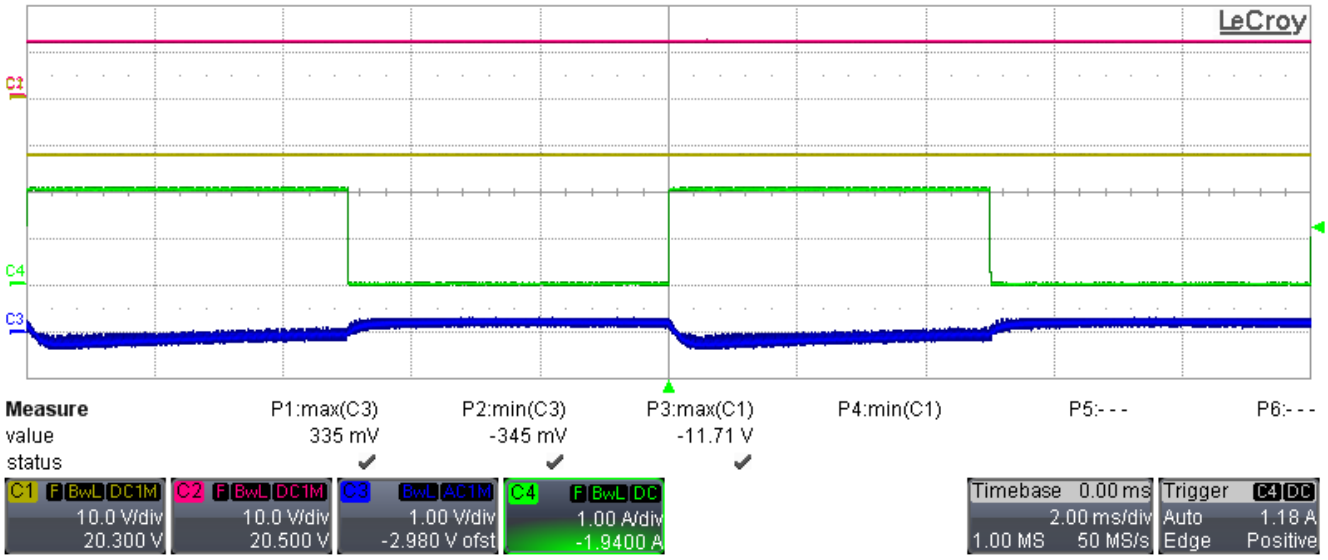


図 3-26. Transient Response of the Converter With Zero to 2-A Transients on 12 V_{OUT}

図 3-27 shows the transient response of –12-V output with 12 Vp fully loaded. C1 is –12-V output switched from 100 mA to zero and C4 is the –12-V output current.

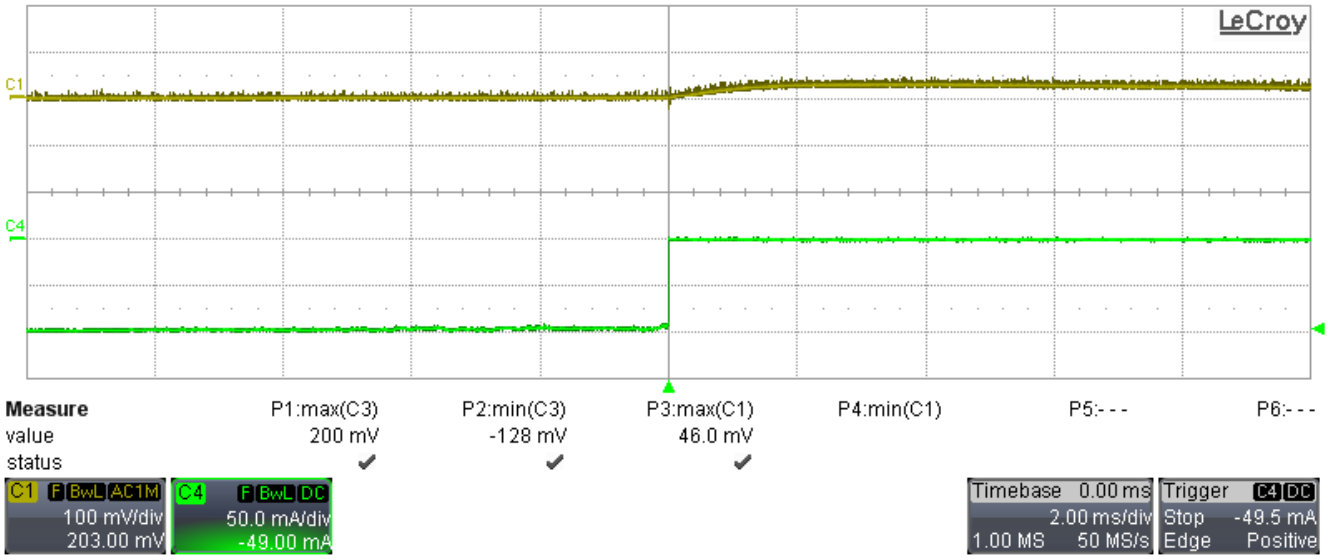


図 3-27. Transient Response of –12-V Output With 12 Vp Fully Loaded

図 3-28 shows the transient response of –12-V output with 12 Vp fully loaded. C1 is –12-V output switched from zero to 100 mA and C4 is the –12-V output current.

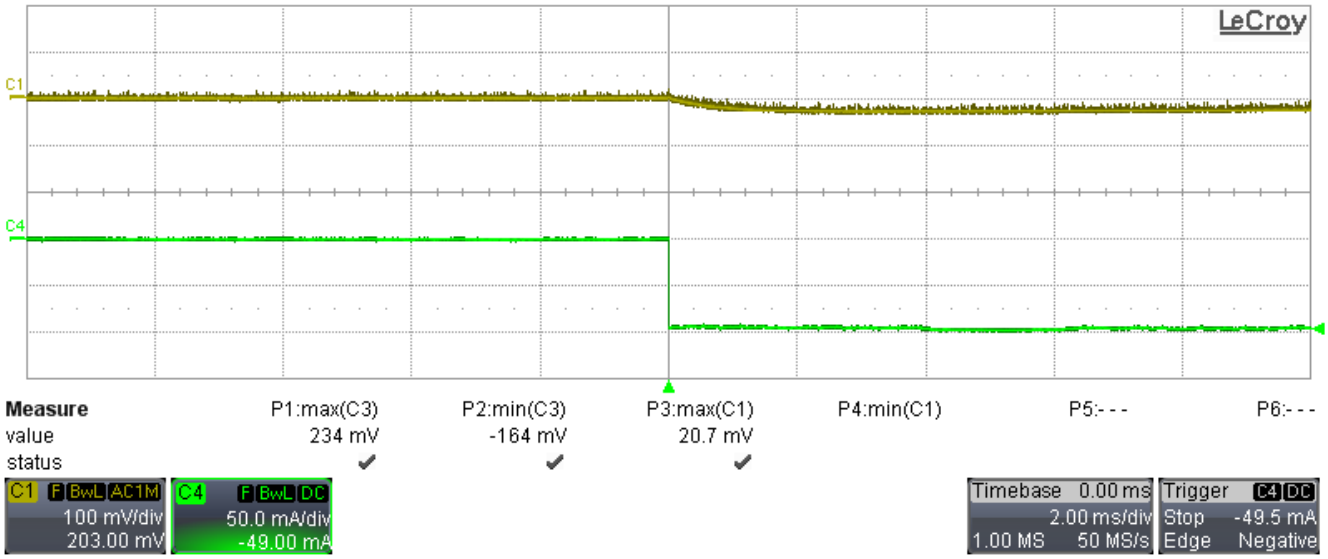


図 3-28. Transient Response of –12-V Output With 12 Vp Fully Loaded

図 3-29 shows the transient response of +12-V output with 12 Vp fully loaded. C2 is +12-V output switched from zero to 100 mA and C4 is the +12-V output current.

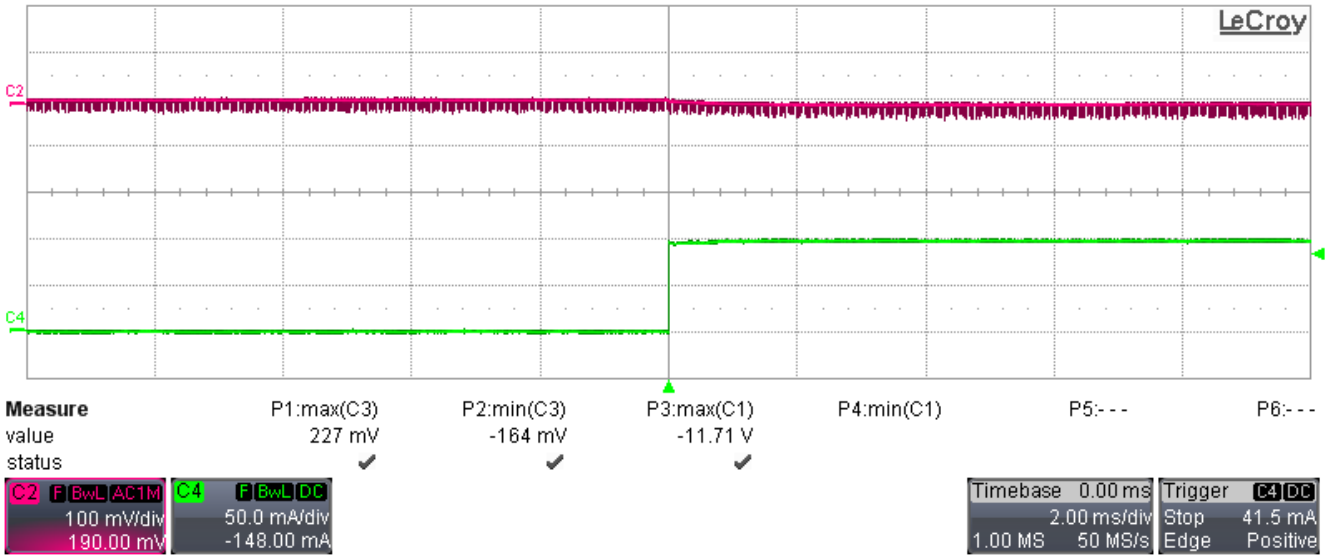


図 3-29. Transient Response of +12-V Output With 12 Vp Fully Loaded

図 3-30 shows the transient response of +12-V output with 12 Vp fully loaded. C2 is +12-V output switched from 100 mA to zero and C4 is the +12-V output current.

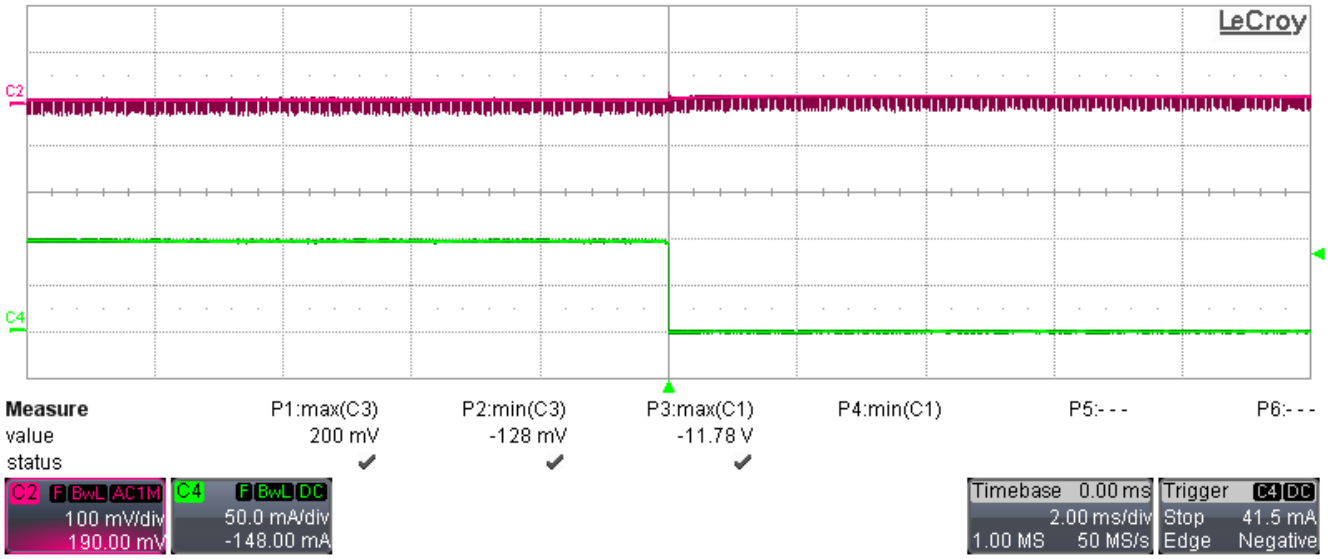


図 3-30. Transient Response of +12-V Output With 12 Vp Fully Loaded

3.3.1.5 Thermal Performance

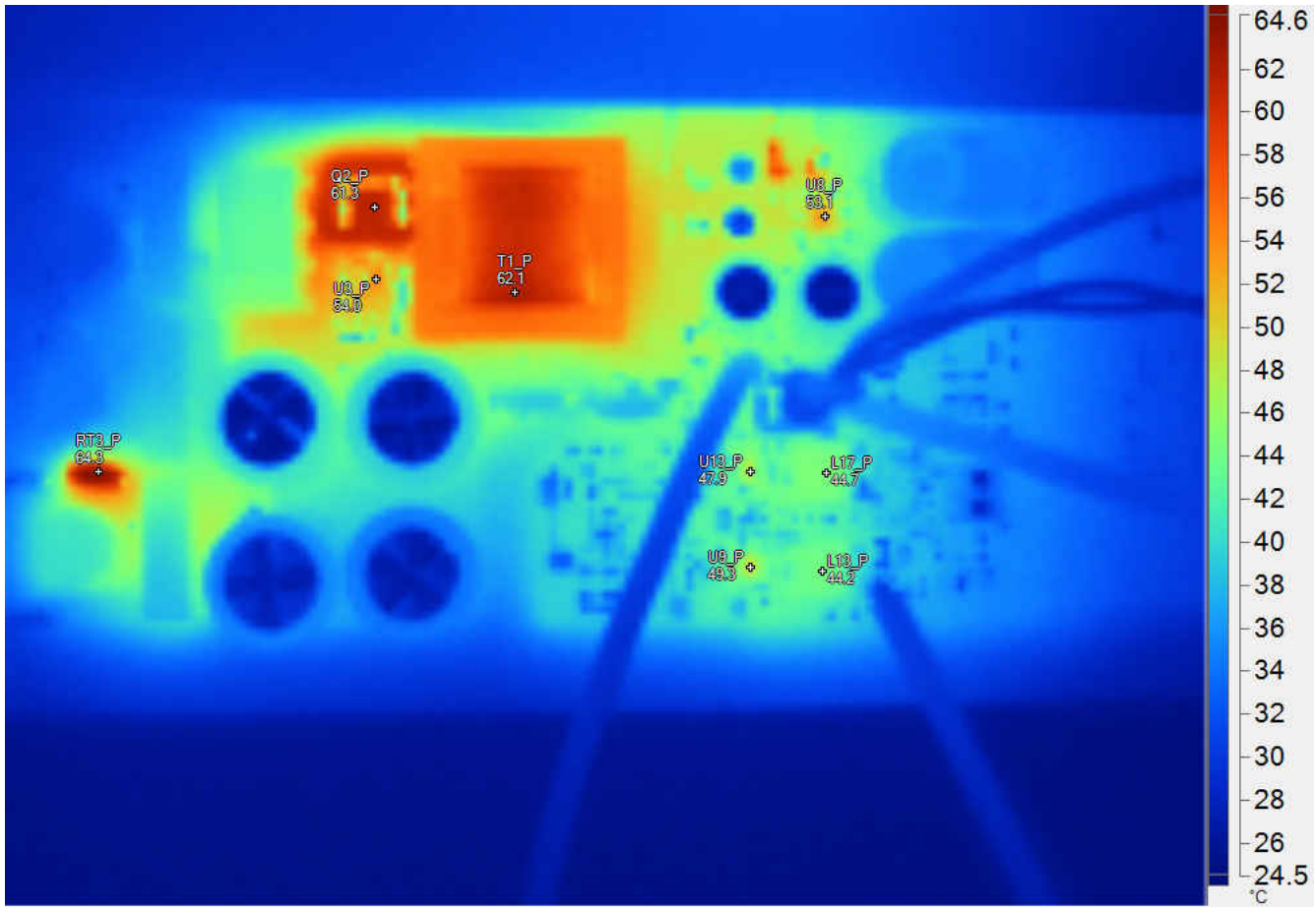


図 3-31. Top View of AC/DC Stage at 120-V AC, 60-Hz AC Input

表 3-6. Main Image Markers (Top Side)

NAME	TEMPERATURE	EMISSIVITY	BACKGROUND
RT3_P	64.3°C	0.96	25.5°C
Q2_P	61.3°C	0.96	25.5°C
T1_P	62.1°C	0.96	25.5°C
U8_P	53.1°C	0.96	25.5°C
U13_P	47.9°C	0.96	25.5°C
U9_P	49.3°C	0.96	25.5°C
L17_P	44.7°C	0.96	25.5°C
L13_P	44.2°C	0.96	25.5°C
U3_P	54.0°C	0.96	25.5°C

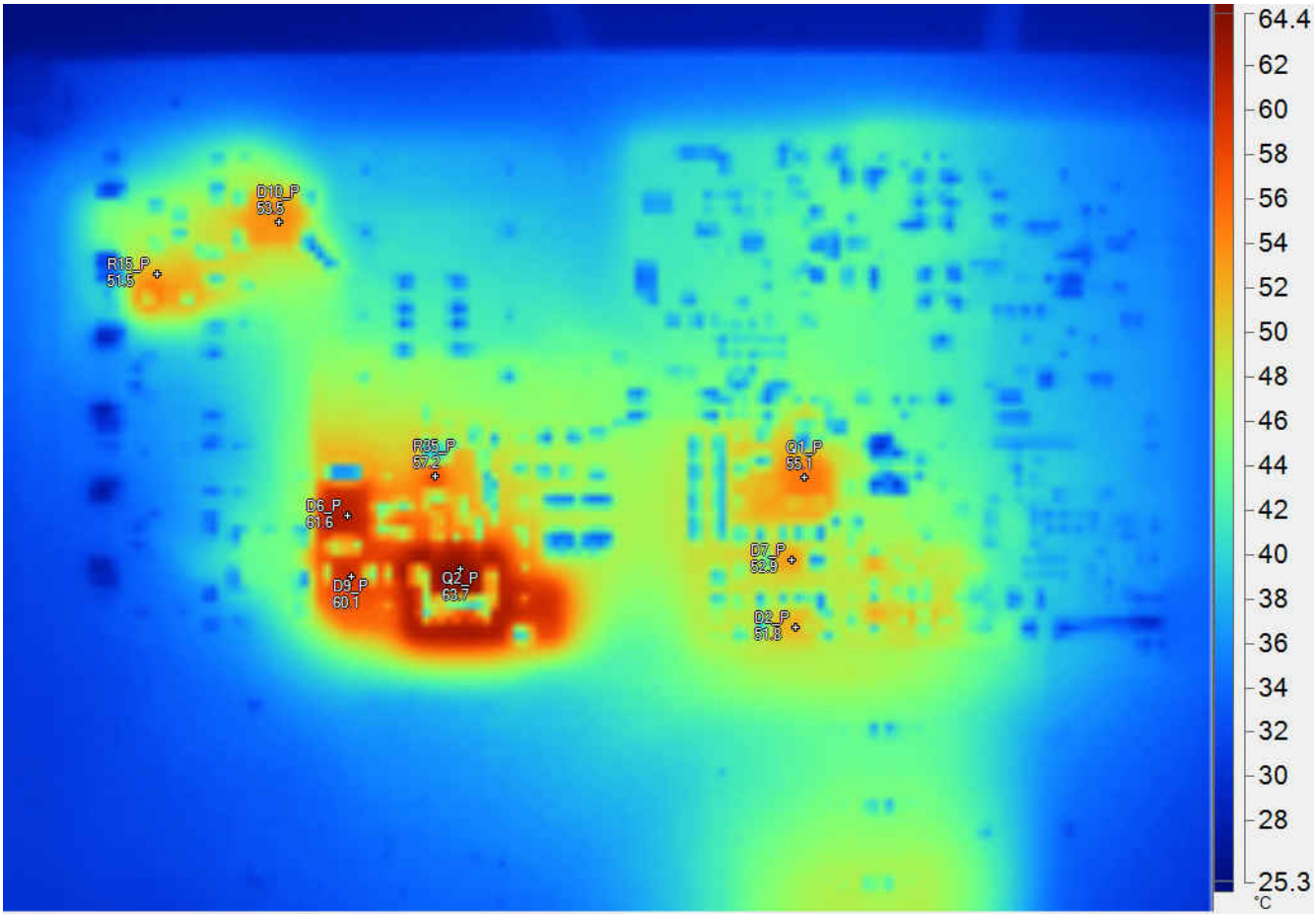


図 3-32. Bottom View of AC/DC Stage at 120-V AC, 60-Hz AC Input

表 3-7. Main Image Markers (Bottom Side)

NAME	TEMPERATURE	EMISSIVITY	BACKGROUND
D10_P	53.5°C	0.96	25.5°C
R15_P	51.5°C	0.96	25.5°C
D6_P	61.6°C	0.96	25.5°C
D9_P	60.1°C	0.96	25.5°C
Q2_P	63.7°C	0.96	25.5°C
R35_P	57.2°C	0.96	25.5°C
Q1_P	55.1°C	0.96	25.5°C
D7_P	52.9°C	0.96	25.5°C
D2_P	51.8°C	0.96	25.5°C

3.3.2 TLV1805-Based Control Pilot Interface

This section shows test data for control pilot signal logic high and low voltage, pulse width, and frequency.

3.3.2.1 TLV1805 Output Rise and Fall Time

図 3-33 and 図 3-34 show the rise and fall times of the TLV1805 control pilot signal generator.

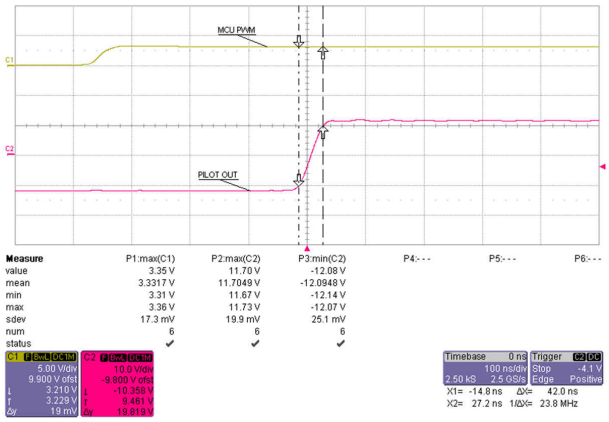


図 3-33. TLV1805 Control Pilot Signal Generator Rise Time

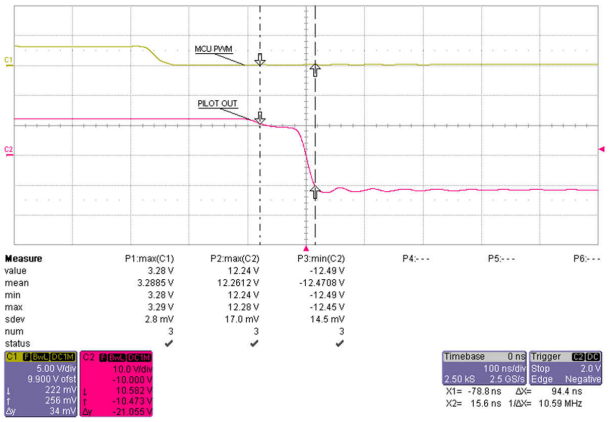


図 3-34. TLV1805 Control Pilot Signal Generator Fall Time

3.3.2.2 Control Pilot Signal Voltage Accuracy in Different States

図 3-35 through 図 3-38 show the control pilot signal voltage accuracy in different states.

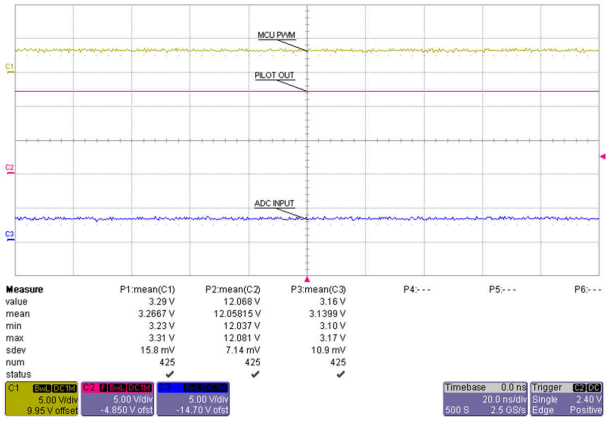


図 3-35. Control Pilot Signal Voltage Accuracy in State A

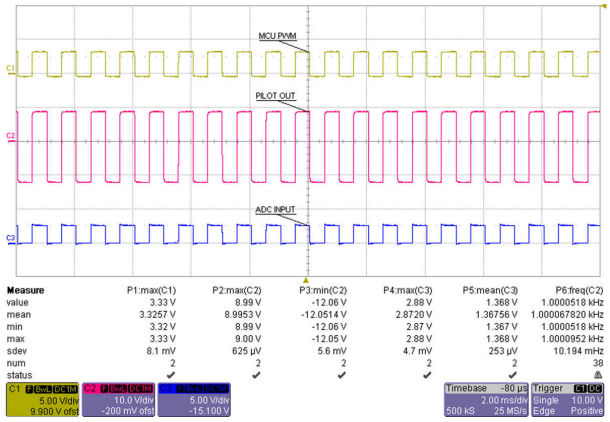


図 3-36. Control Pilot Signal Voltage Accuracy in State B

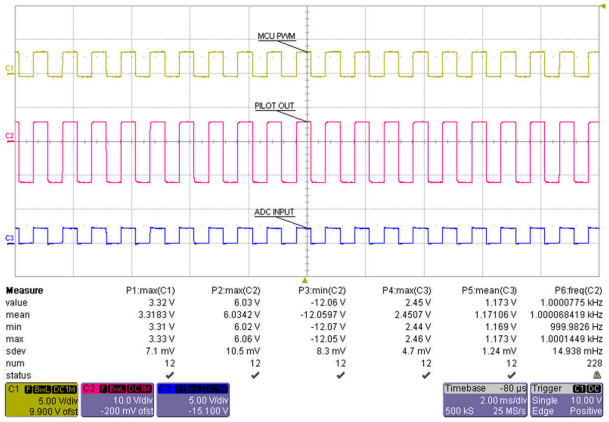


図 3-37. Control Pilot Signal Voltage Accuracy in State C

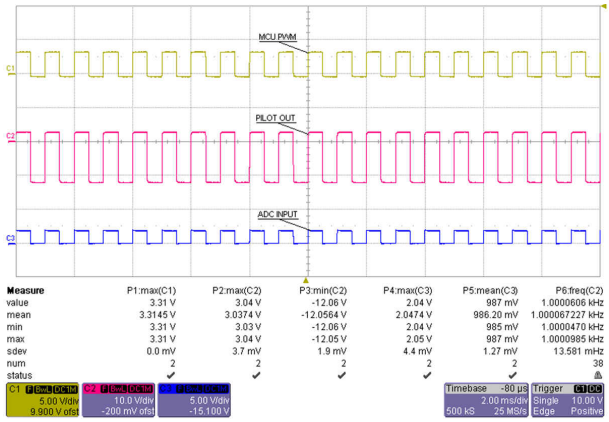


図 3-38. Control Pilot Signal Voltage Accuracy in State D

3.3.3 DRV8220-Based Relay and Plug Lock Drive

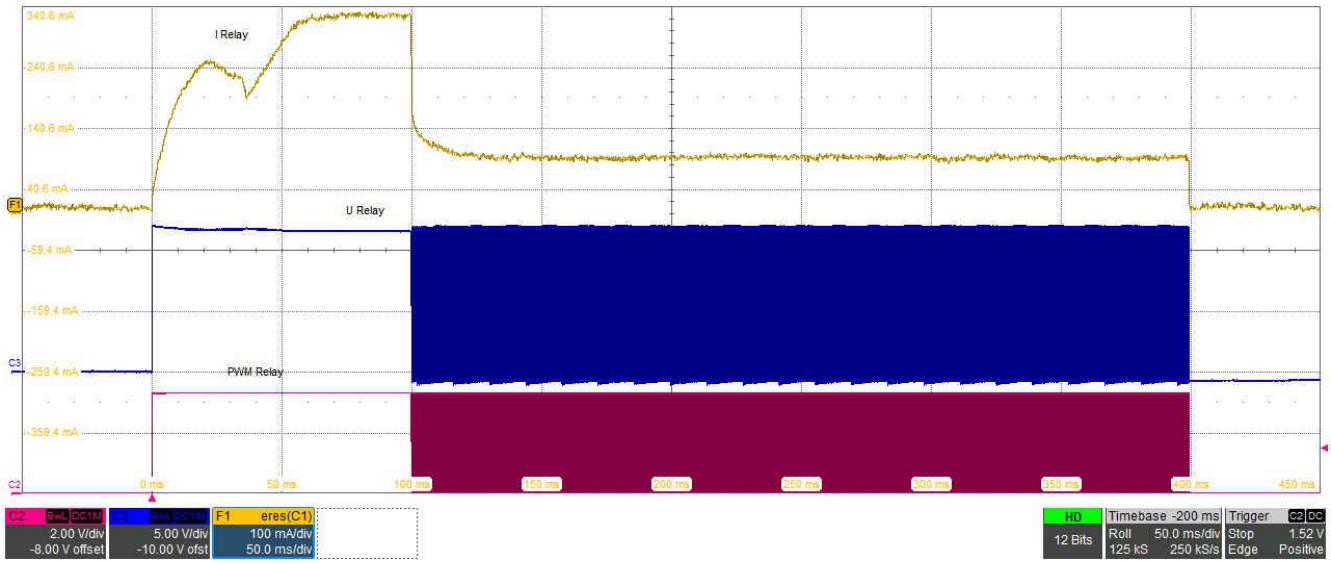


図 3-39. Relay Drive Waveforms

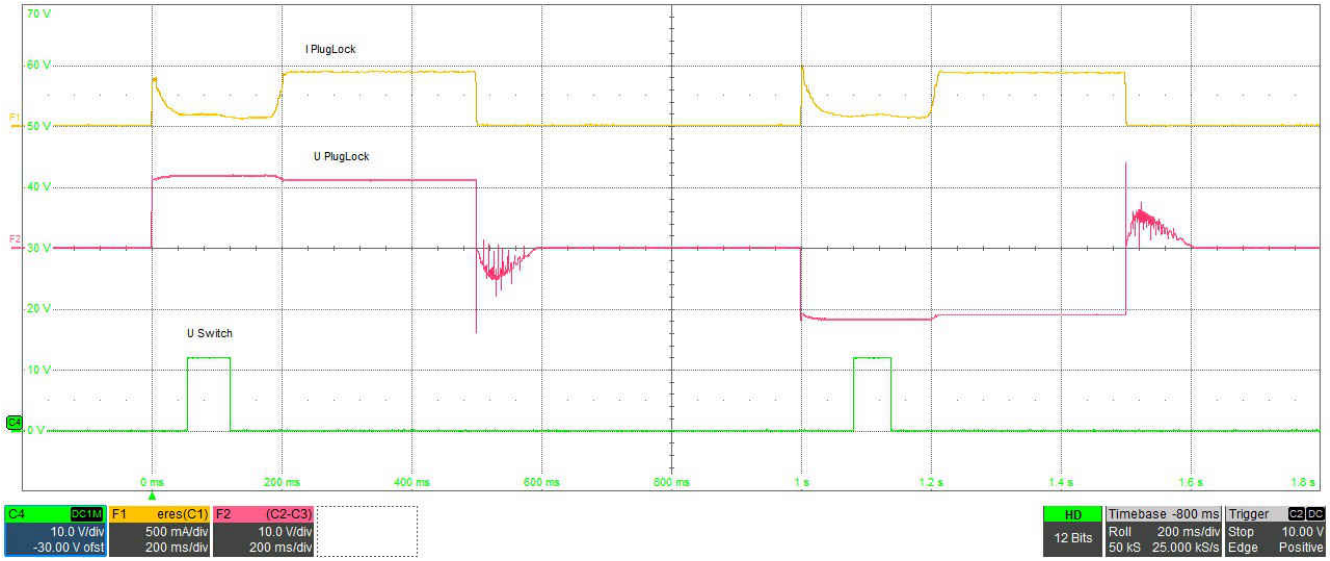


図 3-40. Plug Lock Drive Waveforms

3.3.4 ISO1212-Based Isolated Line Voltage Sensing

For this reference design, the high and low thresholds are set to 125 V_{RMS} and 121 V_{RMS}, respectively. The measured high and low thresholds are 178 V (126 V_{RMS}) and 170 V (120 V_{RMS}) as shown in 図 3-42.

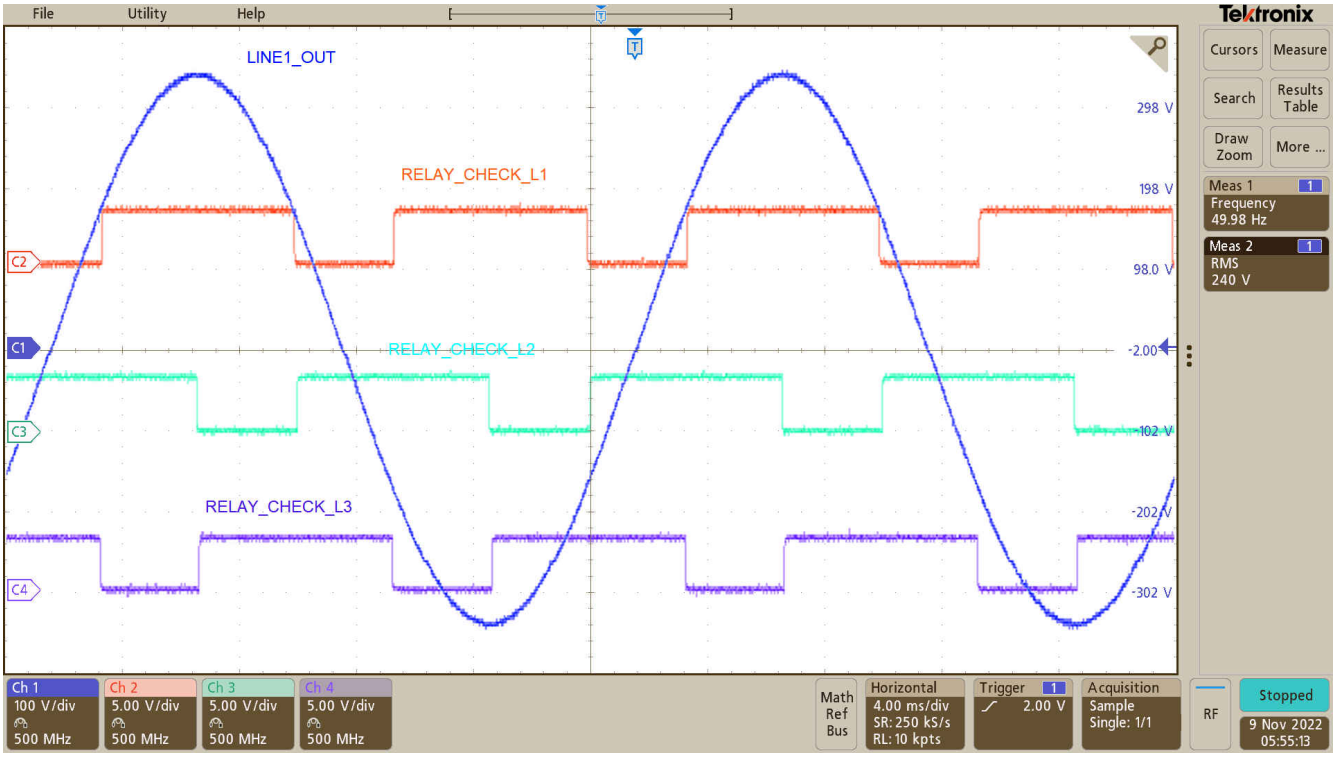


図 3-41. ISO1212 Digital Outputs and Input Line Voltage When Relay is Closed with Labels

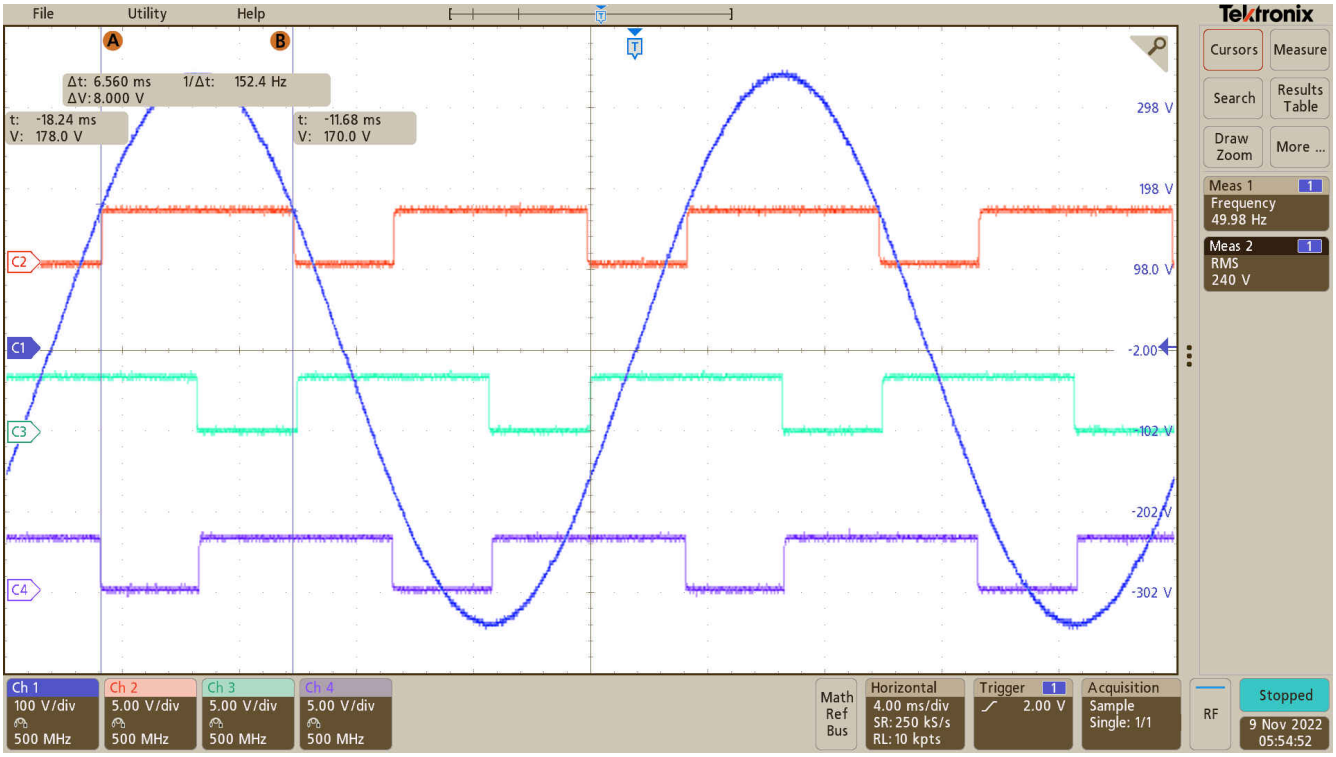


図 3-42. ISO1212 Digital Outputs and Input Line Voltage When Relay is Closed with Cursors

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010239.

4.1.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010239.

4.2 Documentation Support

1. Texas Instruments, *TIDA-00637: Level 1&2 Electric Vehicle Service Equipment Reference Design*
2. Texas Instruments, *TLV1805 40V, Rail-to-Rail Input, Push-Pull Output, High Voltage Comparator with Shutdown* data sheet
3. Texas Instruments, *ISO121x Isolated 24-V Digital Input Receivers for Digital Input Modules* data sheet

4.3 サポート・リソース

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4.4 Trademarks

5 About the Author

KELVIN LE is a systems engineer at Texas Instruments, where he is responsible for developing system solutions for the grid sector with a focus on EV charging. Kelvin has been with TI since 2015. Kelvin earned his Bachelor of Science in Biomedical Engineering from the University of Central Oklahoma and his Master of Science in Electrical and Computer Engineering from the University of Texas at Austin.

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