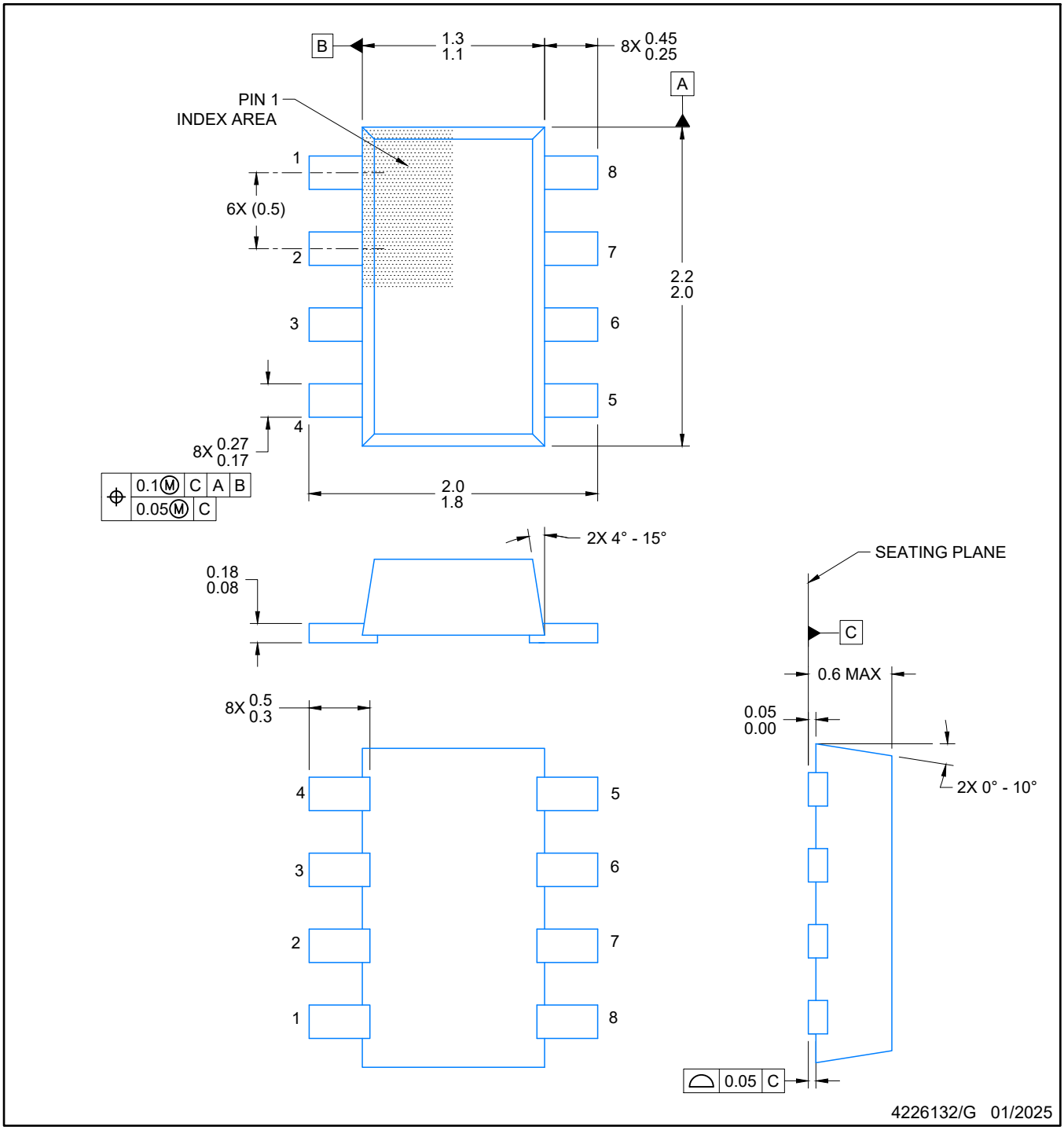
PACKAGE OUTLINE

DTS0008A

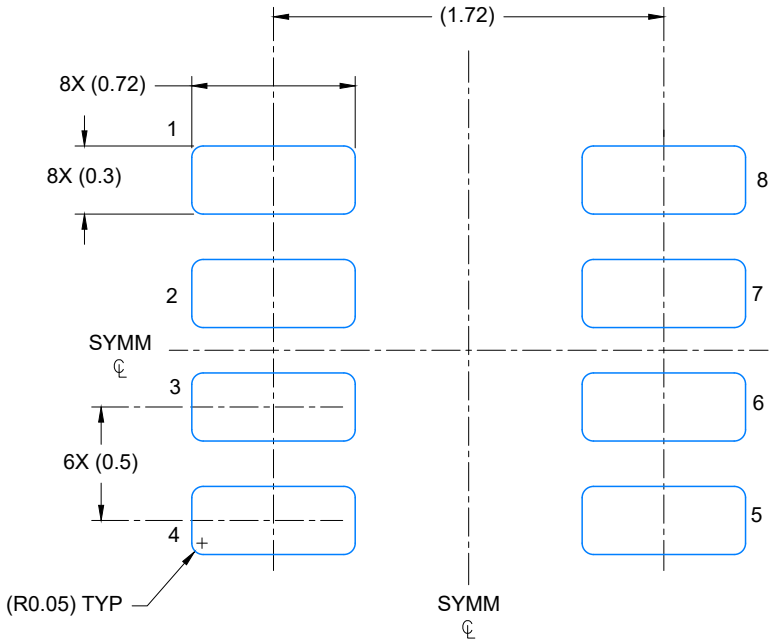
SOT - 0.6 mm max height

SMALL OUTLINE TRANSISTOR

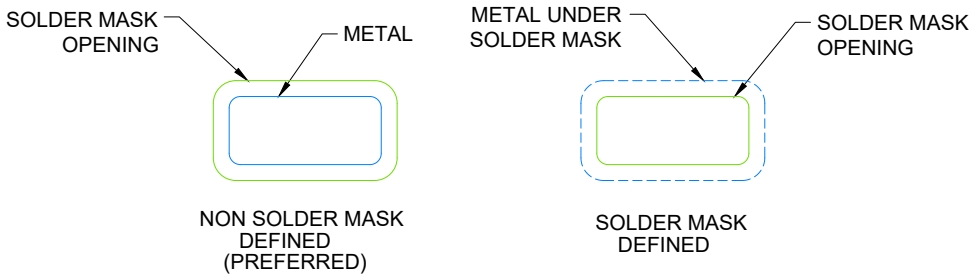


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not incude mold flash, protrusions or gate burrs. Mold flash, interlead flash, protrusions or gate burrs shall not exceed 0.171 per end or side.
4. The side flash along with the stub lead is allowed.
5. Any detached side flash from the stub lead is allowed unless it is touching the bottom side of the lead.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

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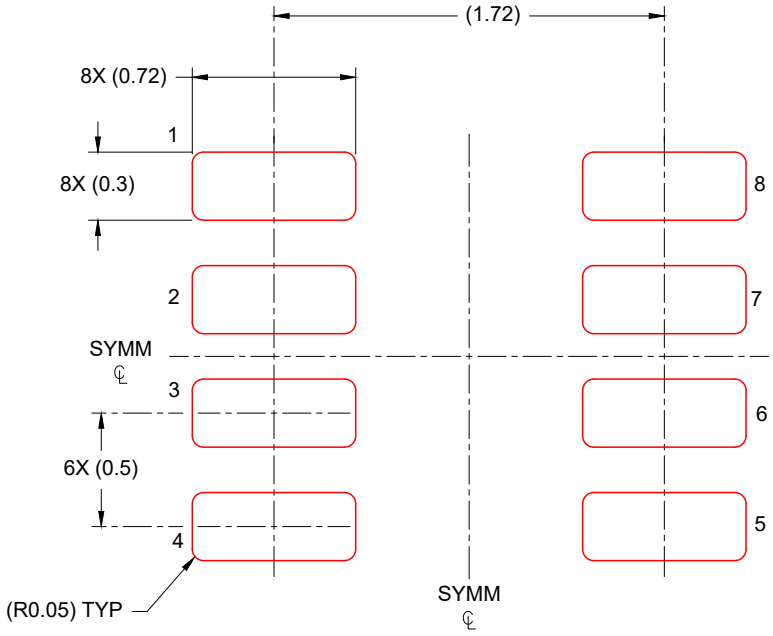
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Land pad design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 30X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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