Optimizing Data Transfer on High-Resolution, High-Throughput Data Converters

Many of today's data acquisition systems in industrial, medical and precision measurement applications incorporate high resolution and high throughput analog-to-digital converters (ADCs). Higher resolution data conversion requires more bits of data per sample, while higher throughput ADCs provide more samples per second. These attributes result in the demand for high data transfer rates between the ADC and the host, producing constraints that may be difficult to resolve. This article focuses on the Enhanced-SPI's Clock Re-Timer data transfer operation supported by some precision SAR ADCs.

The Serial Peripheral Interface (SPI) is a synchronous serial communication interface commonly used with ADCs where the device sends data in response to serial clock. Figure 1 illustrates the typical timing delays involved between the host and the ADC. The various delays encountered in the system can lead to a set of constraints that can make supporting high data rates difficult.

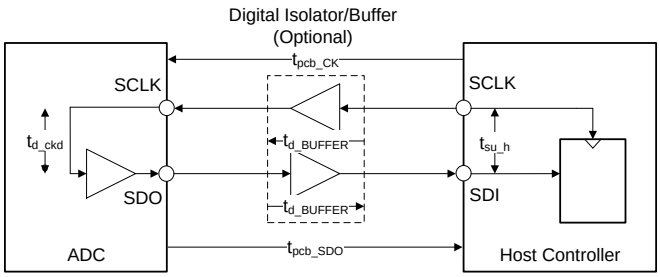

Figure 1. Typical Data Transfer Delays between Host and ADC

In this figure, the t_{pcb_CK} and t_{pcb_SDO} are the delays introduced by the printed circuit board (PCB) traces for the serial clock and SDO signals, t_{d_CKDO} is the clock-to-data delay of the device, t_{d_BUFFER} is the propagation delay introduced by any bus buffers, level translators or digital isolators, and t_{su_h} is the setup time specification of the host controller. The total delay in the path is given by,

$$t_{d\_total} = t_{pcb\_CK} + t_{d\_BUFFER} + t_{d\_CKDO} + t_{pcb\_SDO} + t_{su\_h}$$

A relation to calculate the maximum SCLK rate as a function of the total data transfer delay is given below:

$$f_{clk\_SPI} \leq 1 / t_{d\_total}$$

These equations stipulate that the maximum SCLK frequency cannot exceed the constraints imposed by the sum of the delays, limiting the application throughput.

Consider an application requiring communication between the ADS8920B and a host controller through a digital buffer over 1-ft distance of PCB microstrip. The ADS8900B is a 16-B, 1-MSPS, SAR ADC, where the data is available for read-out after the end of conversion. There is a minimum quiet time delay which must be allowed in order to settle the inputs of the ADC before start of next conversion. Figure 2 shows the typical read time interval.

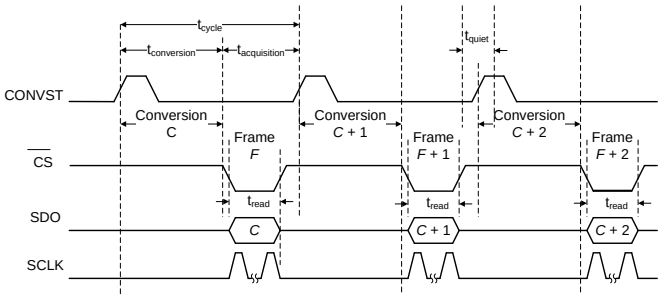

Figure 2. Standard 3-wire SPI Interface with ADS8920B

Hence the total time available for data read is:

$$t_{read} = t_{cycle} - t_{conversion} - t_{quiet}$$

The ADS8920B has 640-ns conversion time period and a 30-ns quiet time. In order to operate the ADC at 1-MSPS, 16-bits of data must be read in 330-ns. The minimum required SPI clock speed can be computed as:

$$f_{clk\_SPI} = N_{bits} / t_{read} = 16 \text{ bits} / 330 \text{ ns} = 48.5 \text{ MHz}$$

However, the maximum SCLK frequency for this system is constrained to 30.75-MHz due to the delays of the 1ft PCB traces and buffers as calculated in Table 1:

Table 1. Calculation of Total Transfer Delay

t_{pcb_CK}	t_{d_BUFFER}	t_{d_ckdo}	t_{pcb_SDO}	t_{su_h}	t_{d_total}
1.36 ns	6.9 ns (2x)	13 ns	1.36 ns	3 ns	32.52 ns

Therefore, the system is restricted to a maximum SCLK frequency of 30.75-MHz and is unable to support the SCLK frequency required to achieve 1-MSPS sample rate.

Enhanced-SPI's Clock Re-Timer Data Transfer

Some TI ADCs such as the ADS8920B and ADS9110 have a dedicated pin to provide a return clock back to the processor. This mode of operation is called the Clock Re-Timer. This Enhanced-SPI mode of operation solves the SCLK frequency limitation problem by moving the timing control of the data transfer from the host to the ADC. As illustrated in Figure 3, in Clock Re-Timer data transfer, the device provides a synchronous output clock on the RVS pin along with the output data on the SDO pin.

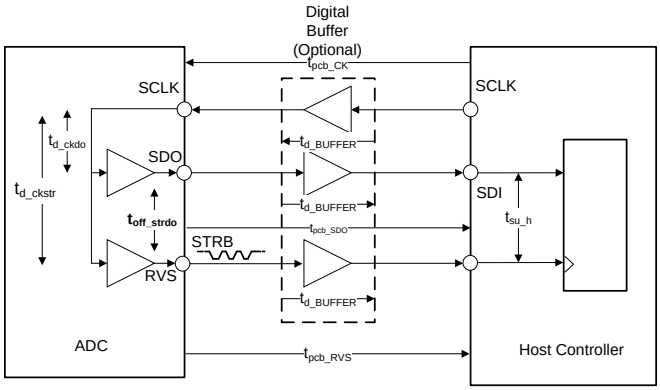

Figure 3. Signals Used for Clock Re-Timer Mode Data Transfer

The RVS pin of the ADC functions as a strobe (STRB) acting as an accompanying clock for the data. Each new data bit on the SDO pin is launched with a corresponding positive edge of the STRB. The host can use the STRB as a clock to capture the SDO data. The total delay in the path for a Clock Re-Timer data transfer is greatly reduced, allowing much higher SCLK frequencies:

$$t_{d\_total\_Timer} = t_{pcb\_RVS} - t_{pcb\_SDO} + t_{SU\_h}$$

The Clock Re-Timer data transfer completely eliminates the effect of buffer delays (t_{d_BUFFER}) and clock-to-data delays (t_{d_CKDO}); typically, the largest contributors in the overall delay computation. Furthermore, the actual values of t_{pcb_RVS} and t_{pcb_SDO} will get cancelled since they are routed through matched length traces. When using the Clock Re-Timer data transfer, the maximum SCLK frequency is limited by the ADC and the set up time (t_{SU_h}) of the host.

The waveform in Figure 4 illustrates the Clock Re-Timer data transfer. From the beginning, the SDO and STRB signals are aligned from the ADC even though they will have a delay with respect to the SCLK at the input of the ADC. As long as the SDO and the STRB are routed with matched traces, they will be aligned at the host. The STRB negative edge can be used reliably as the clock for capturing the SDO.

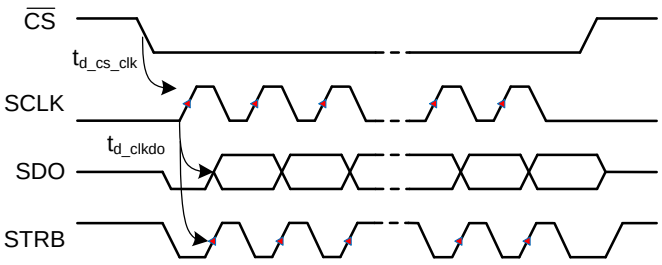

Figure 4. Clock Re-Timer Data Transfer

Clock Re-Timer can also be used to reflect SLCK and the following equation approximately shows the total time required for the overall data transfer, or the time for the CSn to be held active:

$$t_{data\_transfer} = N \cdot T_{clk} - t_{d\_ckdo} + t_{d\_CS\_clk}$$

Where N is the number of bits, T_{clk} is the SCLK period, and $t_{d\_cs\_clk}$ is the CS-to-SCLK delay. In the ADS8920B case, the STRB clock period is 15-ns, and $t_{d\_cs\_clk}$ is 12-ns, resulting on a required data transfer period of 239-ns; meeting the maximum 330-ns read time supporting maximum throughput of 1-MSPS.

In summary, the Enhanced-SPI's Clock Re-Timer eliminates the effect of buffer or isolation delays and eases board layout as there is no need to locate the controller and the ADC extremely close. The SCLK frequency can be as high as the rates supported by the ADC, the host and intermediate buffers, allowing full-throughput data transfer.

Table 2. SAR ADCs Supporting Enhanced SPI's Clock Re-Timer

Device	Resolution	Data Rate	Description
ADS8920B	16-Bit	1-MSPS	SAR ADC with integrated reference buffer and Enhanced-SPI
ADS8910B	18-Bit	1-MSPS	SAR ADC with integrated reference buffer and Enhanced-SPI
ADS8900B	20-Bit	1-MSPS	SAR ADC with integrated reference buffer and Enhanced-SPI
ADS9120	16-Bit	2.5-MSPS	SAR ADC with Enhanced-SPI
ADS9110	18-Bit	2-MSPS	SAR ADC with Enhanced-SPI

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