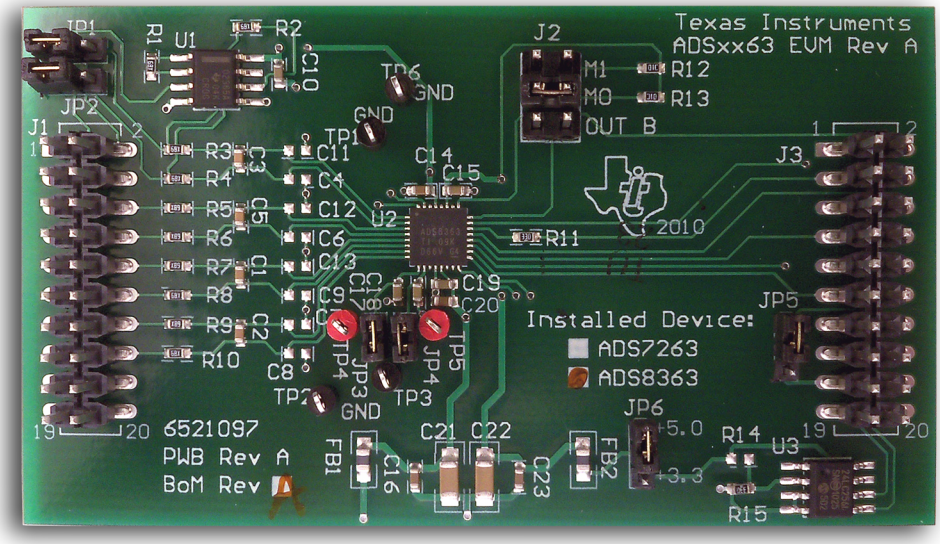
ADS7263/8363



ADS7263/8363EVM

This user's guide describes the characteristics, operation, and use of the ADS7263/8363EVM. This evaluation module (EVM) is an evaluation platform for the ADS7263, a 14-bit, dual, 500-kSPS, 2×2 channel, serial analog-to-digital converter (ADC), and the ADS8363, a 16-bit, 4×2 channel version of the ADS7263. The EVM allows evaluation of all aspects of the ADS7263 or ADS8363 device. A complete circuit description, schematic diagram, and bill of material are included in this document.

The following related documents are available through the Texas Instruments web site at http://www.ti.com.

Related Documentation

Device	Literature Number
ADS7263	SBAS523
ADS8363	SBAS523
Op Amps for Everyone Design Guide	SLOD006B

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1 EVM Overview

1.1 Features

ADS7263/8363EVM Features:

- Full-featured evaluation board for the ADS7263 and ADS8363, dual, 1-MSPS, 14-/16-bit, serial output, 4x2 or 2x2 analog input, simultaneous sampling ADCs
- Analog inputs can be configured as single-ended or differential
- Onboard reference
- High-speed serial interface

Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS7263/8363EVM. Unless otherwise noted, the term *ADS7263/8363* refers to the operation of either the ADS7263 or the ADS8363 converter.

1.2 Introduction

The ADS7263 and ADS8363 are high-speed, low-power, 14- and 16-bit ADCs that operate from independent +5-V AV_{DD} and DV_{DD} supplies.

The four, fully-differential analog inputs are divided into two pairs (A and B). The ADS7263 and ADS8363 each accept an analog input voltage in the range of –VREF to +VREF (5 V_{PP}), centered on the internal +2.5-V (typical) reference. The part also accepts bipolar input ranges when a level shift circuit is used in the analog front-end circuitry. Refer to Section 12 of the design guide, Op Amps for Everyone (SLOD006; available for download at www.ti.com) for further information on various circuit applications.

2 Analog Interface

For maximum flexibility, the ADS7263/8363EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient, 10-pin dual row header/socket combination at J1. This header/socket provides access to the analog input pins of the ADC. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. Use appropriate caution when handling these pins. Table 1 summarizes the pinouts for the analog interface J1.

Table 1. J1: Analog Interface Pinout

Pin Number	Signal	Description
J1.2	B1+	Noninverting input, Channel B1
J1.4	B1–	Inverting input, Channel B1
J1.6	B0+	Noninverting input, Channel B0
J1.8	B0–	Inverting input, Channel B0
J1.10	A1+	Noninverting input, Channel A1
J1.12	A1–	Inverting input, Channel A1
J1.14	A0+	Noninverting input, Channel A0
J1.16	A0–	Inverting input, Channel A0
J1.18	Unused	Pins are unused and should be left open for use with future amplifier and sensor input modules.
J1.20	REFIN	External reference source input (2.5 V nom, 2.525 V max)
J1.1 to J1.19 (odd)	AGND	Analog ground connections

3 Digital Interface

The ADS7263/8363EVM is designed for easy interfacing to multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient, 10-pin dual row header/socket combination at J3. This header/socket provides access to the digital control and serial data pins of the THS1218. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. Table 2 describes the J2 serial interface pins.

Table 2. J3: Serial Interface Pinout

Pin Number	Signal	Description
J3.1	$\overline{CS}$	Chip select; active low signal. Enables data transfer and device configuration.
J3.3	SCLK	Serial clock
J3.5	SCLK(R)	Serial clock return for DSP host
J3.7	FS	RD input
J3.9	FS(R)	Frame sync return for DSP host
J3.11	SDI	Serial data input
J3.13	SDO	Serial data output
J3.15	$\overline{INT}$	Busy output; provides an interrupt source to host processor
J3.17	$\overline{CSTART}$	Conversion start; provides alternate method of conversion initialization
J3.19	SPARE	—

3.1 Additional Control Options

Table 3 shows the pinout of J2. This dual row, four-position header provides additional control functionality to the ADS7263/8363EVM. Signals A0, M0, and M1 are configured with pull-up resistors by default. The jumper shunts supplied with the EVM can be used to set these signals to logic low. These signals can also be connected to control signals in your system.

Table 3. J2 Control Header Pinout

Pin Number	Signal	Description
J2.1	M1	Selects two-channel or four-channel mode
J2.3	M0	Selects between serial outputs A and B
J2.5	SDOB	*B channel* secondary output

4 Power Supplies

The ADS7263/8363EVM board requires +5 V_{DC} for the analog section and either +5V or +3.3V_{DC} for the digital section. While filters are provided for all power-supply inputs, optimal performance of the EVM requires a clean, well-regulated power source. +5-V_{DC} power is applied to J4 pin 3 referenced to pin 5. The digital supply of +3.3V or +5V is applied to J4 pin 9 or J4 pin 10 (respectively), referenced to J4 pin 6.

NOTE: The shunt jumper at location JP6 is placed across pins 1-2. This configuration is the factory default for both the ADS7263EVM and ADS8363EVM.

4.1 Reference Voltage

The ADS7263/8363 can be configured to use its internal reference, or external reference source through jumper JP3 and JP4 (see schematic for details). If an external reference is desired, a clean voltage source may be applied to TP4 or TP5 referenced to analog ground at TP3.

5 EVM Operation

This section provides information on the analog input, digital control, and general operating conditions of the ADS7263/8363EVM.

The analog input source can be applied directly to J1 (top or bottom side) or through optional amplifier and signal conditioning modules. The analog input level should not exceed 5.0 V_{PP}. The analog input range is from –VREF to +VREF (0 to 5 V_{DC}) centered at 2.5 V.

The digital control signals can be applied directly to J3 (top or bottom side). The ADS7263/8363EVM can also be connected directly to a DSP interface board. Refer to the ADS7263 and ADS8363 device product folders for a complete list of DSP interface cards and optional analog interface modules.

Jumper JP5 is provided to allow the separation of the convert start ($\overline{\text{CONVST}}$) and read (RD) signals. The factory default condition for the EVM is to have a shunt jumper placed between pins 1-2 of JP5. This configuration combines the RD and $\overline{\text{CONVST}}$ signals, which are applied to the ADC via J3.7. When JP5 is moved to pins 2-3, the RD signal is applied via J2.7 while $\overline{\text{CONVST}}$ is applied to J3.17.

J2 is provided as a means to access the M0 and M1 control lines as well as the OUTB serial data. Shunt jumpers are placed on J2 pins 3-4, which defaults M0 to a logic low state. Removing the jumpers allows these lines to go to logic high levels through the associated pull-up resistors R12 and R13.

6 Schematics and Layout

Schematics for the ADS7263/8363EVM are appended to this user's guide. The bill of materials is provided in Table 4.

6.1 Bill of Materials

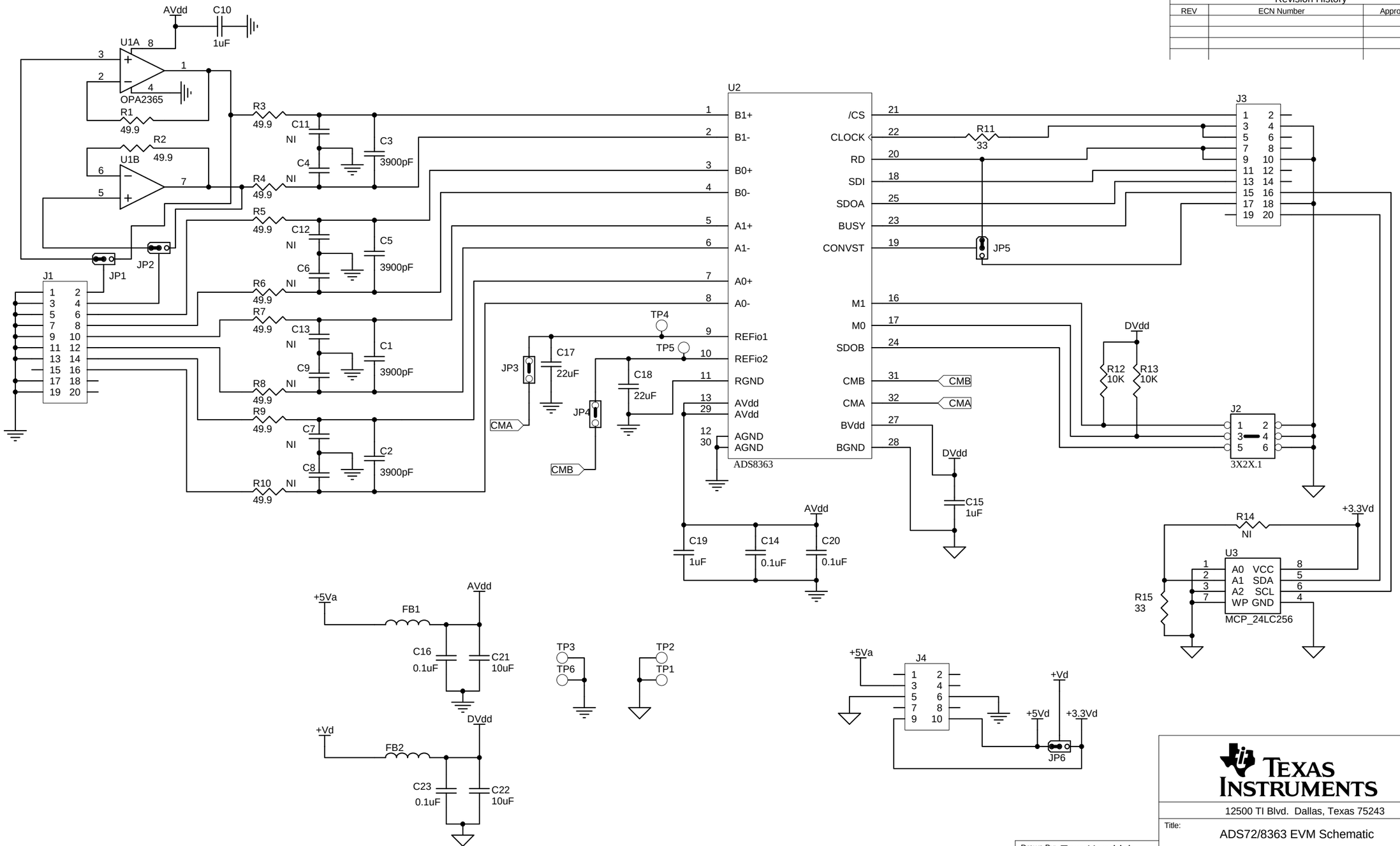
NOTE: All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, see the TI web site.)

Table 4. ADS7223/7263/8363EVM Bill of Materials

Item No.	Quantity	Ref Des	Description	Vendor	Part Number
1	4	C1, C2, C3, C5	Capacitor, ceramic 3900pF 50V 10% X7R 0603	Murata	GRM188R71H392KA01D
2	0	C4, C6, C7, C8, C9, C11, C12, C13	Not Installed		
3	3	C10, C15, C19	Capacitor, ceramic 1.0µF 25V X5R 0603	Murata	GRM188R61E105KA12D
4	4	C14, C16, C20, C23	Capacitor, ceramic 0.1µF 50V 10% X7R 0603	Murata	GRM188R71H104KA93D
5	2	C17, C18	Capacitor, ceramic 10µF 6.3V X5R 0603	Murata	GRM188R60J106ME47D
6	2	C21, C22	Capacitor, ceramic 10µF 25V X5R 1206	Murata	GRM31CR61E106KA12L
7	2	FB1, FB2	Ferrite chip 600Ω 500mA 0805	TDK	MMZ2012R601A
8	2	J1, J3 (Top)	10-pin, dual row, SM Header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
9	2	J1, J3 (Bottom)	10-pin, dual row, SM Header (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
10	1	J2	3x2x0.1, 3-pin dual row header	Samtec	TSW-103-07-T-D
11	1	J4 (Bottom)	5-pin, dual row, SM Header (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
12	4	JP1, JP2, JP5, JP6	3-position jumper, 2mm spacing	Samtec	TMM-103-01-T-S
13	2	JP3, JP4	2-position jumper, 2mm spacing	Samtec	TMM-102-01-T-S
14	10	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10	Resistor 49.9Ω 1/10W 1% 0603 SMD	Yageo	RC0603FR-0749R9L
15	2	R11, R15	Resistor 33.0Ω 1/10W 1% 0603 SMD	Yageo	RC0603FR-0733RL
16	2	R12, R13	Resistor 10.0kΩ 1/10W 1% 0603 SMD	Yageo	RC0603FR-0710KL
17	0	R14	Not installed		
18	4	TP1, TP2, TP3, TP6	Test point PC mini .040"D Black	Keystone	5001
19	2	TP4, TP5	Test point PC mini .040"D red	Keystone	5000
20	1	U1	IC Op Amp GP R-R 50MHz Dual 8-SOIC	TI	OPA2365AID
21	1	U2	Dual, 14-/16-bit 4x2/2x2 1MSPS Simultaneous SAR ADC with two internal references and FIFO (1)	TI	ADS7263SRHBT or ADS8363SRHBT
22	1	U3	IC EEPROM 256Kbit, 400kHz 8-SOIC	Microchip	24LC256T-I/SN
23	6	N/A	2mm Shunt, Black	Samtec	2SN-BK-G
24	2	N/A	Shunt jumper 0.1" Black Gold	3M	969102-0000-DA

(1) The device installed at location U2 depends on the EVM purchased. The installed device is reflected in the EVM orderable part number. This device is soldered to the board for best performance.

Revision History		
REV	ECN Number	Approved



TEXAS INSTRUMENTS

12500 TI Blvd. Dallas, Texas 75243

Title: ADS72/8363 EVM Schematic

Drawn By: Tom Hendrick			
Engineer: Tom Hendrick	SIZE: C	DATE: 1-Dec-2010	REV: A
FILE: 6443174_B.DDB			SHEET: 1 OF: 1

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 3.3 V_{DC} to 5 V_{DC} and the output voltage range of 0 V_{DC} to 5 V_{DC}.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +30°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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