Functional Safety Information

INA227-Q1/INA228-Q1/INA238-Q1 Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for INA227-Q1/INA228-Q1/INA238-Q1 (VSSOP-10 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

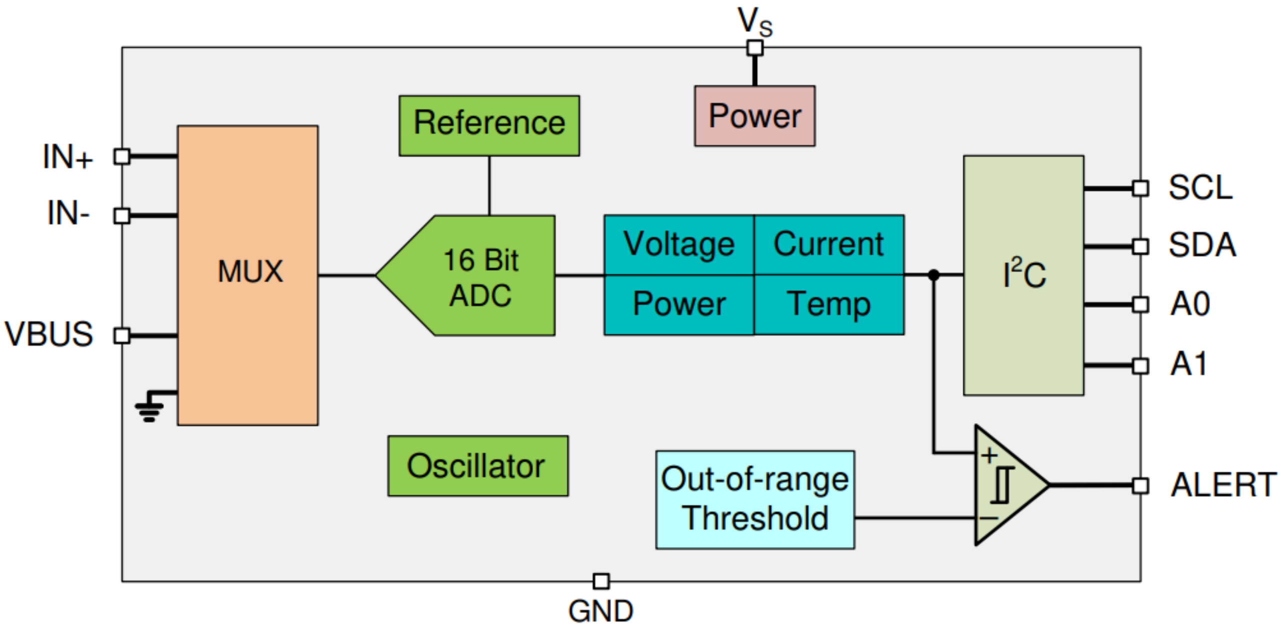

Figure 1-1. Functional Block Diagram

INA227-Q1/INA228-Q1/INA238-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VSSOP-10 Package

This section provides Functional Safety Failure In Time (FIT) rates for VSSOP-10 package of INA227-Q1/INA228-Q1/INA238-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	2
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 25 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs, Analog & Mixed ≤ 50V supply	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA227-Q1/INA228-Q1/INA238-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
ADC output bit error	20%
ADC gain out of specification	20%
ADC offset out of specification	20%
Communication error	15%
Register bit error	10%
ADC mux select error	5%
ALERT - false trip or failure to trip	5%
Pin to pin short, any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INA227-Q1/INA228-Q1/INA238-Q1 (VSSOP-10 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VS (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_S = 3.3 V
- $V_{CM} = V_{IN-}$ = 48 V

4.1 VSSOP-10 Package

Figure 4-1 shows the INA227-Q1/INA228-Q1/INA238-Q1 pin diagram for the VSSOP-10 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA227-Q1/INA228-Q1/INA238-Q1 data sheet.

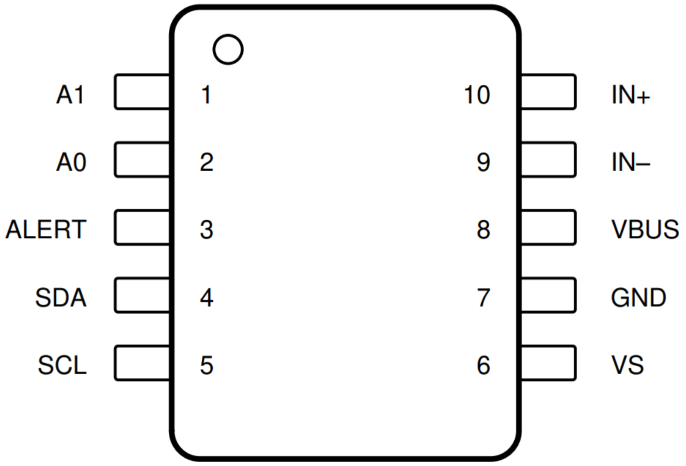

Figure 4-1. Pin Diagram (VSSOP-10) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A1	1	A1 shorted to GND. No change if initially grounded. Loss of I2C communication if tied to SDA or SCL. Power supply shorted to GND if tied to VS.	D for A1=GND; B otherwise

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A0	2	A0 shorted to GND. No change if initially grounded. Loss of I2C communication if tied to SDA or SCL. Power supply shorted to GND if tied to VS.	D for A1=GND; B otherwise
ALERT	3	ALERT forced to active mode. Loss of ALERT functionality.	B
SDA	4	SDA shorted to GND. Loss of communication.	B
SCL	5	SCL shorted to GND. Loss of communication.	B
VS	6	Power supply shorted to GND. No power to the device.	B
GND	7	Normal operation.	D
VBUS	8	VBUS shorted to GND. High current will flow from bus supply to GND.	B
IN-	9	In high-side configuration, a short from the bus supply to GND will occur resulting in high current flow. In low-side configuration, normal operation.	B for high-side; D for low-side
IN+	10	In high-side configuration, a short from the bus supply to GND will occur resulting in high current flow. In low-side configuration, input pins are shorted.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A1	1	A1 pin is open. Undefined device address.	B
A0	2	A0 pin is open. Undefined device address.	B
ALERT	3	ALERT pin is open. Loss of ALERT functionality.	B
SDA	4	SDA pin is open. Loss of communication.	B
SCL	5	SCL pin is open. Loss of communication.	B
VS	6	No power to the device.	B
GND	7	No power to the device.	B
VBUS	8	VBUS pin will float to an unknown voltage. Any measurements and calculations which depend on VBUS will be invalid.	B
IN-	9	Cannot measure sense voltage.	B
IN+	10	Cannot measure sense voltage.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
A1	1	2 - A0	A1 shorted to A0. No change if A1 and A0 are initially the same. Loss of I2C communication for any short combination between GND, SDA, and SCL, or if SCL is tied to VS. Power supply shorted to ground if one pin is Vs and the other is GND. If SDA is shorted to VS, then the device could be damaged when SDA is driven low by the device if input current is > 10 mA.	A for SDA to VS; D for A1=A0; B otherwise
A0	2	3 - ALERT	A0 shorted to ALERT. Address changes with ALERT signal. Loss of I2C communication if A0 is SDA or SCL. If A0 is tied to VS, then the device could be damaged when ALERT is driven low by the device if input current is > 10 mA.	A for ALERT to VS; B otherwise
ALERT	3	4 - SDA	ALERT shorted to SDA. Loss of communication.	B
SDA	4	5 - SCL	SDA shorted to SCL. Loss of communication.	B
SCL	5	6 - VS	SCL shorted to VS. Loss of communication.	B
VS	6	7 - GND	Power supply shorted to GND. No power to the device.	B
GND	7	8 - VBUS	VBUS shorted to GND. High current will flow from bus supply to GND.	B
VBUS	8	9 - IN-	In high-side configuration, input pins are shorted and applied sense voltage is 0 V. In low-side configuration, a short from the bus supply to GND will occur resulting in high current flow.	B
IN-	9	10 - IN+	Input pins shorted together. Applied sense voltage is 0 V.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN+	10	1 - A1	In high-side configuration, a short from the bus supply to A1 will occur. If A1 is driven to voltage > VS + 0.3 V, device could be damaged. In low-side configuration, A1 shorted to GND. No change if initially grounded. Loss of I2C communication if tied to SDA or SCL. Power supply shorted to GND if tied to VS.	A for high-side; D for low-side for A1=GND; B for low-side otherwise

Table 4-5. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A1	1	A1 shorted to VS. No change if initially set to VS. Loss of I2C communication if SCL is tied to VS. Power supply shorted to ground if A1 is GND. If A1 is SDA then the device could be damaged when SDA is driven low by the device if input current is > 10 mA.	A for A1=SDA; D for A1=VS; B otherwise
A0	2	A0 shorted to VS. No change if initially set to VS. Loss of I2C communication if SCL is tied to VS. Power supply shorted to ground if A1 is GND. If A1 is SDA then the device could be damaged when SDA is driven low by the device if input current is > 10 mA.	A for A0=SDA; D for A0=VS; B otherwise
ALERT	3	ALERT shorted to VS. When ALERT is driven low, device could be damaged if input current is > 10 mA.	A
SDA	4	SDA shorted to VS. When SDA is driven low, device could be damaged if input current is > 10 mA.	A
SCL	5	SCL shorted to VS. Loss of communication.	B
VS	6	Normal operation.	D
GND	7	Power supply shorted to GND. No power to the device.	B
VBUS	8	VBUS shorted to VS. The device could be damaged if VS is driven to a voltage > 6 V.	A
IN-	9	In high-side configuration, VBUS shorted to VS. The device could be damaged if VS is driven to a voltage > 6 V. In low-side configuration, power supply shorted to GND. No power to the device.	A for high-side; B for low-side
IN+	10	In high-side configuration, VBUS shorted to VS. The device could be damaged if VS is driven to a voltage > 6 V. In low-side configuration, power supply shorted to GND. No power to the device.	A for high-side; B for low-side

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