PGA308

User's Guide

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This user's guide describes the function and operation of the PGA308, a single-supply, auto-zero sensor amplifier with programmable gain and offset.

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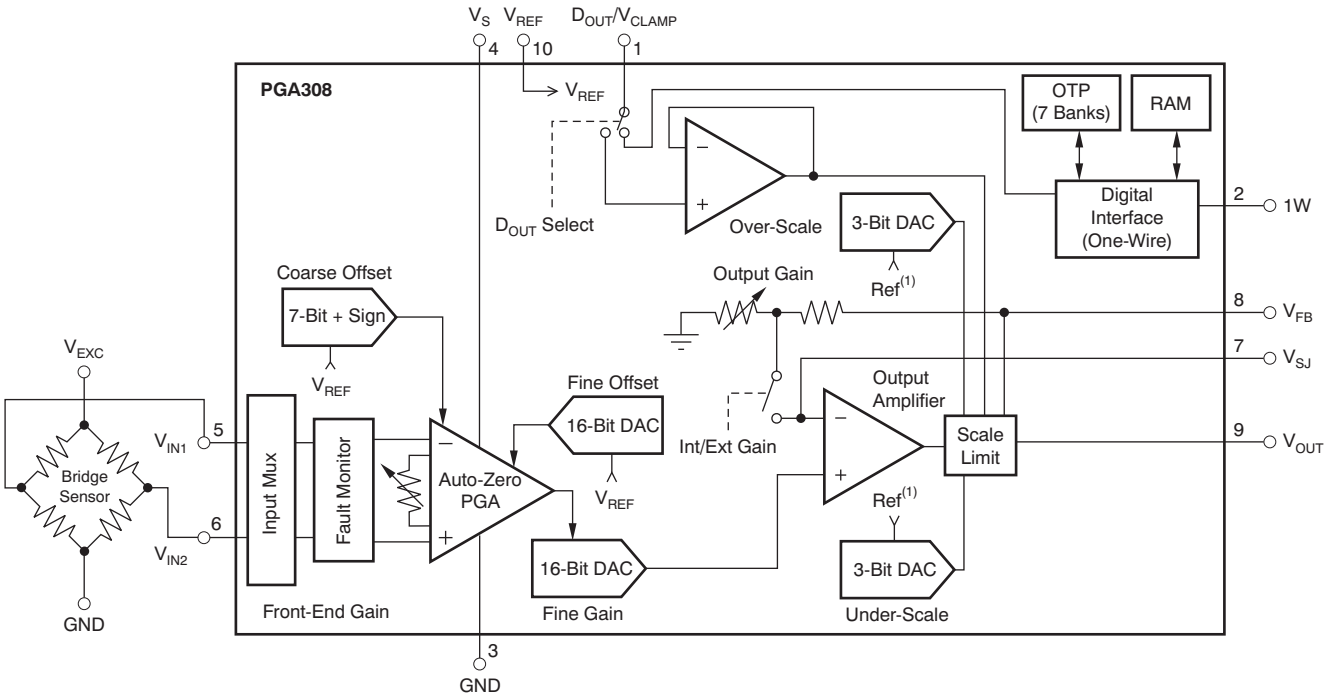
1.1 Overview

The PGA308 is an ideal building block for resistive bridge sensor conditioning and general data acquisition. Digitally-programmable coarse offset, fine offset, and gain may be controlled in real-time or permanently programmed into the PGA308. Figure 1-1 shows the PGA308 in a typical bridge sensor application.



(1) Ref = V_{REF} or V_S selectable.

Figure 1-1. PGA308 in a Typical Bridge Sensor Application

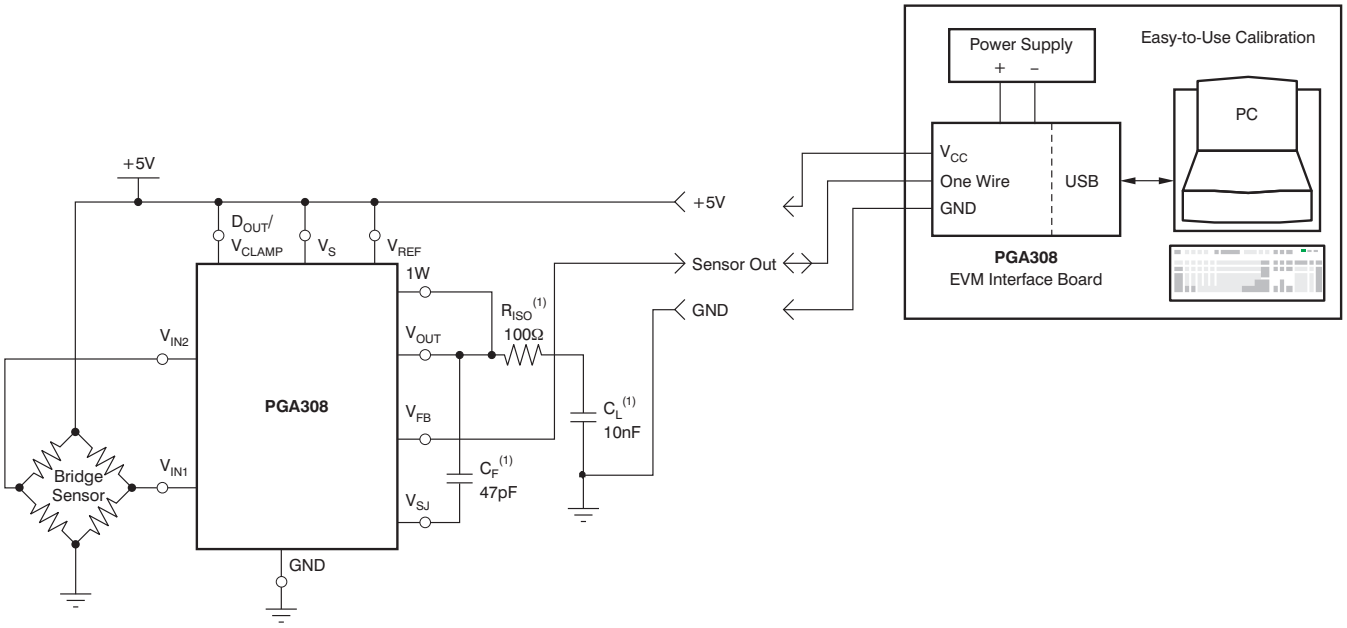
1.1.1 Sensor Error Adjustment Range

The PGA308 is designed to readily accommodate the following sensors:

- $Span_{25C}$: 0.08mV/V to 296mV/V
- Initial Offset: 20mV/V

Span and Offset are based on a bridge sensor excitation voltage of +5V, a PGA308 output voltage span of 4V (+0.5V to +4.5V), V_{REF} of +5V, and a V_{OUT}/V_{IN} upper gain of 9600. Individual applications must consider noise, small signal bandwidth, V_{OUT}/V_{IN} gain, and required system error to assess whether or not the PGA308 will work for a given sensor sensitivity.

The PGA308EVM provides easy-to-use setup and calibration of the PGA308 through a personal computer and PGA308EVM software. Figure 1-2 shows the typical PGA308 device, EVM, and bridge connections.



(1) Although not needed in all applications:

- R_{ISO} provides the PGA308 with overvoltage protection on Sensor Out.
- C_L provides EMI/RFI filtering.
- C_F provides the PGA308 with stability for the capacitive load of C_L.

Figure 1-2. PGA308, Evaluation Module, and Bridge Sensor Connections

1.2 Related Documentation from Texas Instruments

Current versions of all documentation can be obtained from the TI website at http://www.ti.com/, or by calling the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify the document by both title and literature number (shown in parentheses).

Data Sheets:

PGA308 (SBOS440)

User's Guides:

PGA308EVM User's Guide (SBOU060)
Sensor-Emulator-EVM Reference Guide (SBOA102)
USB DAQ Platform User's Guide (SBOU056)
Universal Serial Bus General-Purpose Device Controller (SLLS466)

Tools:

PGA308EVM Source Code (SBOC256)
PGA308EVM Software (SBOC257)
PGA308EVM Evaluation Module

1.3 If You Need Assistance

If you have questions about the PGA308 evaluation module, join the discussion with the Linear Amplifiers Applications Team in the e2e™ forum at e2e.ti.com. Include ***PGA308*** as the subject heading of your posting.

1.4 Information About Cautions and Warnings

This document contains caution statements.

CAUTION

This is an example of a caution statement. A caution statement describes a situation that could potentially damage your software or equipment.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

1.5 FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense is required to take whatever measures may be required to correct this interference.

Functional Description

This chapter describes the functions of the PGA308.

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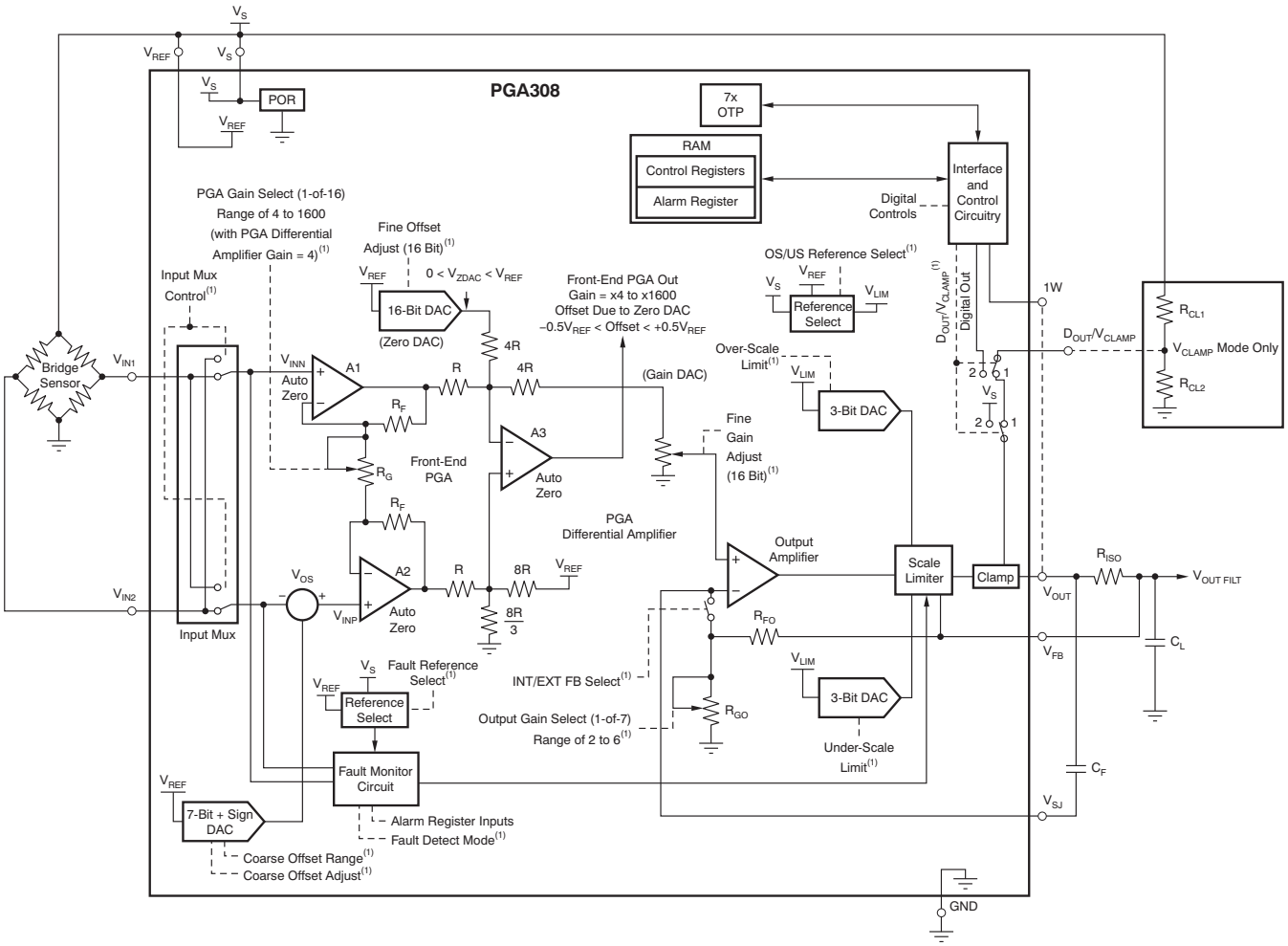
2.1 Block Diagram

Figure 2-1 shows a detailed block diagram of the PGA308 and can be used as a reference figure for the subsections in this section.



(1) User-adjustable feature.

Figure 2-1. Detailed Block Diagram

2.2 Amplification Signal Path

The PGA308 core consists of the precision, low-drift, low-noise, front-end programmable gain amplifier (PGA). This Front-End PGA has gain capabilities from x4 to x1600. The Output Amplifier has a gain range from x2 to x6. A fine gain adjust in front of the Output Amplifier offers a selectable x0.33 to x1.0 attenuation factor. Theoretically, this architecture yields a V_{OUT}/V_{IN} gain range of x2.66 to x9600 for the PGA308. Many applications use overall gains of x1600 or less. Although capable of up to x9600 overall gain, the selection of gains in the Front-End PGA and Output Amplifier are designed to allow for gain distribution throughout the PGA308 that enables optimum span and offset scaling from input to output. The Input Mux allows the polarity of the inputs to be switched in order to accommodate sensors with unknown polarity output. Higher gains reduce bandwidth and require more analog filtering and/or system analog-to-digital converter (ADC) averaging to reject noise.

2.3 Coarse and Fine Offset Adjustment

The sensor offset adjustment is performed in two stages. The input-referred Coarse Offset Adjust Digital-to-Analog Converter (DAC) has a ±100mV offset adjustment range for a selected V_{REF} of +5V. Any residual input sensor offset and any desired V_{OUT} offset pedestal for zero-applied sensor strain input are provided by a fine offset adjust through the 16-bit Zero DAC that combines with the signal from the output of the Front-End PGA.

2.4 Voltage Reference

The PGA308 V_{REF} pin is an input voltage reference pin. The reference voltage is used in the Coarse Offset Adjust and Zero DACs. The Fault Monitor circuitry trip points, as well as the Over- and Under-Scale limits, can be configured so that they are referenced to either V_S or V_{REF}. This flexibility permits both absolute and ratiometric mode designs.

2.5 Fault Monitor Circuit: Sensor Fault Detection (also see Figure 3-12 and Figure 3-16)

To detect sensor burnout and/or short circuits, a set of four comparators (external fault comparators) are connected to the inputs of the Front-End PGA. There are two fault detect modes of operation for these comparators.

The first fault detect mode is Common-Mode Fault. If either input is taken to less than 100mV or greater than V_S – 1.2V, then the corresponding comparator sets a sensor fault flag that can be programmed to cause the PGA308 V_{OUT} to be driven to within 100mV (I_{OUT} < 4mA) of either V_S (or V_{CLAMP}, if V_{CLAMP} is used) or ground. This level will be well above the set Over-Scale Limit level or well below the set Under-Scale Limit level. The state of the fault condition can be read in digital form in the ALRM Register. If Over-Scale/Under-Scale limiting is disabled, the PGA308 output voltage will continue to be driven to within 100mV (I_{OUT} < 4mA) of either V_S (or V_{CLAMP}, if V_{CLAMP} is used) or ground, depending on the selected fault polarity, high or low.

The second fault detect mode is Bridge Fault. In Bridge Fault Mode, either V_S or V_{REF} (whichever is used for bridge excitation) can be chosen as the fault voltage, V_{FLT}. If either of the inputs are taken to less than the larger of either 100mV or 0.35V_{FLT}, then a fault is signaled. Also, if either of the inputs are taken to greater than the smaller of V_S – 1.2V or 0.65V_{FLT}, then a fault is signaled. This design allows for bridge differential voltages of up to 30% of the bridge excitation voltage. The corresponding comparator sets a sensor fault flag that can be programmed to cause the PGA308 V_{OUT} to be driven within 100mV (I_{OUT} < 4mA) of either V_S (or V_{CLAMP}, if V_{CLAMP} is used) or ground. This level will be well above the set Over-Scale Limit level or well below the set Under-Scale Limit level. The state of the fault condition can be read in digital form in the Fault Status Register. If Over-Scale/Under-Scale limiting is disabled, the PGA308 output voltage will continue to be driven within 100mV (I_{OUT} < 4mA) of either V_S or ground, depending on the selected fault polarity, high or low.

In addition, there are five other fault detect comparators (internal fault comparators) that help detect subtle PGA308 front-end violations that could result in linear voltages at V_{OUT} and be interpreted as valid states. These fault detect comparators are especially useful during factory calibration and setup. Section 3.6, *Fault Monitor Circuitry*, provides details about the PGA308 fault monitoring capabilities.

2.6 Over-Scale and Under-Scale Limits

The Over-Scale and Under-Scale Limit circuitry provides programmable upper and lower clip limits for the PGA308 output voltage. Combining the fault monitor circuitry functions with system diagnostics allows the user to determine when a conditioned sensor is defective or the process being monitored by the sensor is out of range. The selected PGA308 V_{LIM} is divided down by a precision resistor string to form the Over- and Under-Scale Limit trip points. These resistor ratios are extremely accurate and produce no significant initial or temperature errors. As shown in the Over-Scale/Under-Scale Limit Circuit (Figure 3-11), there are two separate amplifiers, the Over-Scale and Under-Scale amplifiers, that use the Over-Scale or Under-Scale threshold, respectively, and determine where the PGA308 output, V_{OUT}, is clipped. The reference for the trip points, V_{LIM}, is register-selectable for either V_{REF} or V_S.

2.7 V_{CLAMP} Pin

The V_{CLAMP} pin is a dual-use pin. It can be used for either a V_{OUT} clamp function or as a digital output function. The voltage clamp function provides an output voltage clamp that is external-resistor programmable. In mixed-voltage systems, when powering the PGA308 from +5V with the output scaled for 0.1V to 2.9V, V_{CLAMP} can be set to 3.0V to prevent an overvoltage lock-up/latch-up condition on a 3V system ADC or microcontroller input. The digital output function allows for configuration of a sensor module. The value can either be pre-programmed in one-time programmable (OTP) memory or controlled through the One-Wire interface (1W pin).

2.8 Digital Interface: One-Wire Program Protocol

The PGA308 is configurable through a single wire universal asynchronous receiver/transmitter (UART)-compatible interface (1W pin). It is possible to connect this single wire communication pin to the V_{OUT} pin in true three-wire sensor modules (V_S, GND, and Sensor Out) and continue to allow for calibration and configuration programming. Refer to Section 4.4, *Digital Interface*, and the One-Wire Protocol timing diagram (Figure 4-2).

Each transaction consists of several bytes of data transfer. Each byte consists of 10-bit periods. The first bit is the start bit, which is always zero. The 1W pin must always be high when no communication is in progress. The '1' to '0' (high to low) transition signals the start of a byte transfer with all timing information for the current byte referenced to this transition.

The second through ninth bits are the eight data bits for the byte and are transferred LSB first. The 10th bit is the stop bit, which is always '1'. The recommended circuit implementation uses a pull-up resistor and/or current source with an open drain (or open collector) output connected to the 1W pin, which is also an open drain output. The single wire may be driven high by the controller during transmission from the controller, but some form of pull-up is required to allow the signal to go high during reception because the PGA308 1W pin can only pull the output low.

All communication transactions start with an initialization byte that is transmitted by the controller. This byte (55h) senses the baud rate used for the communication transaction. The baud rate is sensed during the initialization byte of every transaction. This baud rate is used for the entire transaction. Each transaction may use a different baud rate, if desired. Baud rates of 4.8k to 114k bits/second are supported.

The second byte is a command/address byte. The last bit in this byte indicates either a read or write at the address selected by the address pointer portion of the byte. Additional data transfer occurs after the command/address byte. The number of bytes and direction of data transfer depend on the command byte. For a read sequence, the PGA308 waits for a two-bit delay (unless programmed otherwise) after the completion of the command/address byte before beginning to transmit. This wait period allows time for the controller to ensure that the PGA308 is able to control the One-Wire interface. The least significant byte of the register is transmitted first; the second byte is the most significant byte of the register.

2.9 Timeout on the One-Wire Interface

A timeout mechanism is implemented to allow for resynchronization of the One-Wire interface if

synchronization between the controller and the PGA308 is lost for any reason. The timeout period is set to approximately 28ms (typical). If the timeout period expires between the initialization byte and the command byte, between the command byte and any data byte, or between any data bytes, the PGA308 resets the One-Wire interface circuitry to a state that expects an initialization byte. Every time a byte is transmitted on the One-Wire interface, this timeout period is reset.

2.10 Power-On Sequence of the PGA308

The PGA308 has circuitry to detect when the power supply is applied to the PGA308 and reset the internal registers to a known power-on reset (POR) state. This reset also occurs when the power supply is detected as invalid, so that the PGA308 is in a known state when the supply returns to a valid level. The threshold for this circuit is approximately 1.5V to 2.5 V. When the power supply becomes valid, the PGA308 waits for approximately 25ms, during which time V_{OUT} is disabled, and then attempts to read the data from the last valid OTP memory bank. If the memory bank has the proper checksum, the PGA308 registers are loaded with the OTP data and V_{OUT} is enabled. If the checksum is invalid, V_{OUT} is disabled.

The One-Wire Interface can always communicate with the PGA308 and override the contents of the current OTP bank in use, unless this function is disabled by the OWD bit in the CFG2 Register (Configuration Register 2). Overriding the contents of the current OTP bank is accomplished by setting the appropriate SWL[2:0] bits in the SFTC Register (Software Control Register). For applications that require an *instant-on* for V_{OUT}, the NOW bit in the CFG2 Register must be set to '1', which eliminates the 25ms disable of V_{OUT} on power-up.

2.11 One-Wire Operation with 1W Connected to V_{OUT}

Some sensor applications prefer a sensor module with three pins: V_S, GND, and Sensor Out. These applications also prefer digital calibration of the sensor module after the final assembly of the sensor and electronics. The PGA308 has a mode that allows the One-Wire interface pin, 1W, to be connected directly to the PGA308 output pin, V_{OUT}.

To calibrate the PGA308 + Sensor, first configure the internal registers on the PGA308, then measure the analog voltage on V_{OUT} as a result of these register value settings. Repeat the configuration and measurement process until the correct voltage is obtained. Because V_{OUT} is connected to 1W, the ability to enable and disable V_{OUT} is required to allow a multiplexing operation between 1W (using the connection as a bidirectional digital interface) and V_{OUT} (driving the connection as a conditioned sensor output voltage.)

The PGA308 also offers a mode in which the output amplifier can be enabled for a set time period and then disabled to allow sharing of the 1W pin with the V_{OUT} connection. The enable/disable of the output amplifier is accomplished by writing a value to bits OEN[7:0] in the One-Wire Enable Control register (OENC). Any non-zero value enables the output. This non-zero value is decremented every 10ms until it becomes zero. When this value becomes zero, V_{OUT} is disabled and a 1s timeout begins waiting for bus activity on the digital interface (1W pin). As long as there is activity on the 1W pin, the 1s timeout is continually reset.

After 1s of no bus activity, the PGA308 checks for a correct checksum. If the checksum is correct, the PGA308 runs with the values that currently exist in RAM. If the checksum is not valid, the PGA308 checks for written bank select registers in OTP in the order of BANK SEL4, BANK SEL3, BANK SEL2, then BANK SEL1. The highest bank select register that contains valid programmed data is read. The value read from this register points to one of the seven OTP banks, which is then loaded into RAM.

2.12 OTP Memory Banks

There are four one-time programmable (OTP) bank selection registers: BANK SEL1, BANK SEL2, BANK SEL3, and BANK SEL4. Bank selection can be set four times by programming the BANK SEL*x* registers in sequence (1, 2, 3, 4). The default OTP bank used on POR is the location stored in the last programmed BANK SEL*x* register. Therefore, if programmed, BANK SEL4 always has priority over the other bank select registers.

The PGA308 contains seven OTP user memory banks. All seven of these banks can be independently programmed. However, the default bank at POR can be set only four times. The seven possible OTP user memory banks allow an end product with a microcontroller interface between the end user and the PGA308 to select from up to seven factory pre-programmed configurations. It also provides total user flexibility for any other configuration through software communication over the One-Wire interface. This flexibility allows no-scrap recovery from miscalibration situations.

Analog Architecture

This chapter provides a detailed description of the PGA308 analog circuitry.

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3.1 Gain Scaling

The PGA308 contains three primary gain blocks for scaling differential input bridge sensor signals, as shown in Figure 3-1. The Front-End PGA contains the highest gain selection to allow for the highest signal-to-noise ratio by applying the largest gain at the front of the signal chain before the addition of other noise sources. The Front-End PGA gain select has 16 gain settings (4, 8, 16, 32, 64, 100, 200, 400, 480, 600, 800, 960, 1200, and 1600) and is set by bits GI[4:0] (CFG0 Register [D12:D8]). GI4 selects the polarity of the input mux. The input mux allows electronic lead swapping of the bridge inputs for proper polarity selection of the differential input voltage after a module (that is, a sensor and the associated electronics) is built.

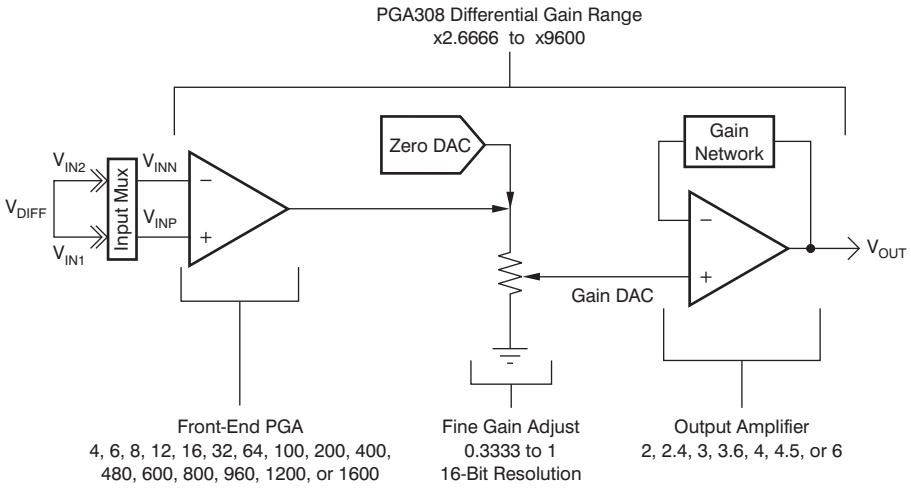


Figure 3-1. PGA308 Gain Blocks

The Front-End PGA is followed by the Gain DAC. The fine gain adjust is controlled by the 16-bit Gain DAC and is adjustable from 0.3333 to 1. The GDAC Register is used only for the Gain DAC setting. Final signal gain is applied through the Output Amplifier, which has an internal select of seven gain settings (2, 2.4, 3, 3.6, 4.0, 4.5, and 6). The Output Amplifier has a selection to disable the internal gain and allow user-supplied external resistors to set the Output Amplifier gain. Bits GO[2:0] (CFG0 Register [D15:13]) select the internal Output Amplifier gains, except when programmed with '111', which disables the internal feedback.

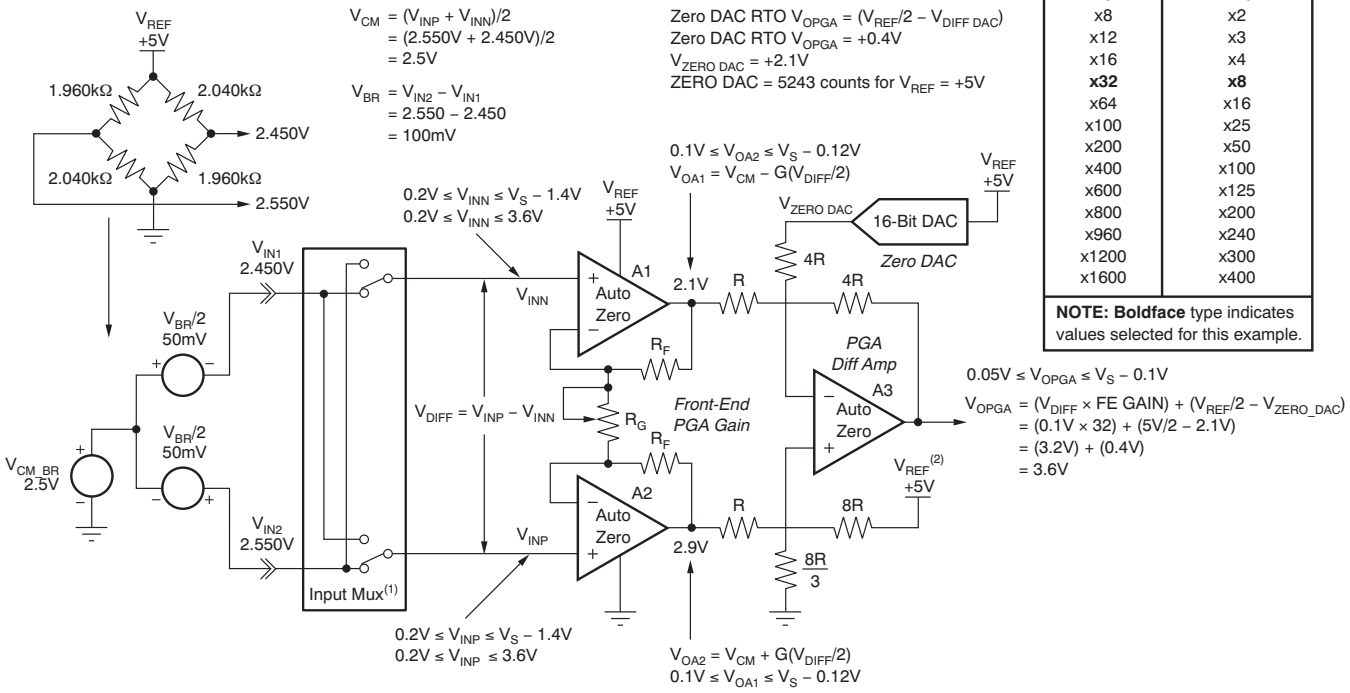
The combined gain blocks allow for a V_{OUT}/V_{DIFF} signal gain of 2.666 (1MHz bandwidth) to 9600 (10kHz bandwidth). Higher gains result in higher noise at V_{OUT} and can require additional post-filtering, depending upon the desired signal-to-noise ratio.

The wide selection of gains in various combinations is provided to optimize sensor input signal scaling for almost any sensor application. The Front-End PGA of the PGA308 is a three op amp instrumentation amplifier configuration for optimum rejection of common-mode voltages and high input impedance to avoid loading of sensor signal sources. This instrumentation amplifier is constructed using op amps with Auto-Zero front-ends to virtually eliminate 1/f noise.

As with any instrumentation amplifier, there are limitations on the output voltage swing and input common-mode voltage range. The circuit shown in Figure 3-2 is representative of the Front-End PGA within the PGA308, and is used to evaluate critical internal node voltages to ensure that output voltage swing and common-mode limits are not violated. It is possible to violate the limits of these internal nodes and continue to have apparently valid output voltages at V_{OUT} of the PGA308. As a result, there are internal comparators that can be set to monitor these internal nodes to indicate an out-of-limit condition during sensor calibration (see Section 3.6, *Fault Monitor Circuitry*).

FRONT-END PGA GAINS	
FE GAIN (V_{OPGA}/V_{DIFF})	**A1, A2 GAIN ($G = 1 + 2\ R_F/R_G$)**
x4	x1
x6	x1.5
x8	x2
x12	x3
x16	x4
x32	**x8**
x64	x16
x100	x25
x200	x50
x400	x100
x600	x125
x800	x200
x960	x240
x1200	x300
x1600	x400

NOTE: Boldface type indicates values selected for this example.



NOTE: Coarse offset is zero; therefore: $V_{IN2} = V_{INP}$, $V_{IN1} = V_{INN}$, $V_{DIFF} = V_{BR}$, $V_{CM} = V_{CM\_BR}$.

(1) Input mux allows for sensor output polarity reversal.

(2) PGA Diff Amp gain of x4 allows full range out of Zero DAC and full voltage swing out of A1 and A2 without common-mode violation on A3 input.

Figure 3-2. Front-End PGA Gain: Internal Node Calculations

After choosing appropriate scaling for the PGA308 gain blocks, a simple hand analysis can check for internal node limit violations. It is important to convert the PGA308 input voltages (V_{IN1}, V_{IN2}) to common-mode and differential components for the maximum sensor output. The model for this conversion is illustrated in Figure 3-2.

The Front-End PGA has a gain of 4 in difference amplifier A3. To analyze important internal nodes V_{OA1} and V_{OA2}, it is necessary to assign the proper gain factor (G) to op amps A1 and A2. This process is detailed in Figure 3-2 with the respective equations for the output voltages shown at the appropriate nodes. For maximum V_{DIFF} into the Front-End PGA, V_{OA1} and V_{OA2} are within the allowed voltage swing of:

$0.1V < (V_{OA1}$ or $V_{OA2}) < V_S - 0.12V$.

Or, for this example:

$0.1V < (V_{OA1}$ or $V_{OA2}) < 4.88V$.

Other applications may yield different results that require different gain scaling or a resistor in the positive or negative leg of the sensor excitation path to adjust the common-mode input voltage of the PGA308.

The maximum allowable input voltage range (IVR) of the PGA308 is specified as 0.2V < IVR < V_S − 1.4V, which for this application translates to 0.2V < IVR < 3.6V. As shown in Figure 3-2 , V_{INP} = 2.550V and V_{INN} = 2.450V, which is within the acceptable IVR specification. The output voltage (V_{OPGA}) of difference amplifier A3 has a gain of 4 in it for voltages out of A2 and A1, but a scaling of (V_{REF}/2 – $V_{ZERO\ DAC}$) for voltages out of the Zero DAC. This arrangement allows for Zero DAC offset scaling of +V_{REF}/2 to –V_{REF}/2 referred-to-output (RTO) of A3, V_{OPGA}. This bipolar offset capability eases offset scaling for many sensor applications. V_{OPGA} is shown with the contribution from V_{DIFF} multiplied by the Front-End PGA gain (FE GAIN), plus the Zero DAC output voltage. The V_{OPGA} signal is further processed through the Gain DAC and Output Amplifier gain blocks. Figure 3-3 depicts the Gain DAC and Output Amplifier gain blocks within the PGA308. For this example, the Gain DAC was set to 0.625 and the Output Amplifier to a gain of 2. As shown in Figure 3-3, the net output voltage (V_{OUT}) is 4.5V for the maximum V_{DIFF} output of the sensor.

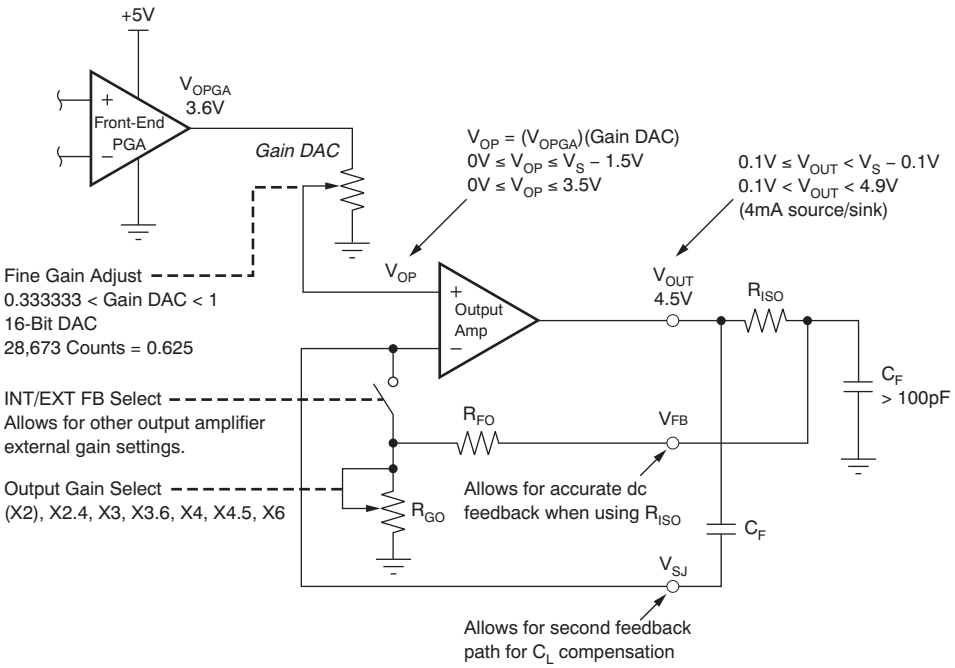


Figure 3-3. Fine Gain Adjust and Output Gain Select

For $V_{OUT\ MIN}$, the sensor output of 0V:

$$V_{OUT\ MIN} = \text{Zero DAC} \times [(\text{Gain DAC})(\text{Output Amplifier Gain})] \quad (1)$$

Where:

Zero DAC = $V_{ZERO\ DAC}$ RTO V_{OPGA}

For this example, then: $V_{OUT\ MIN}$ = 0.4V [(0.625)(2)] = 0.5V

The Output Amplifier has external connections that allow the end-user to have maximum flexibility in output amplifier configurations for a variety of applications. Use of the V_{FB} and V_{SJ} pins is described in Section 3.4, *Output Amplifier*.

3.1.1 PGA308 Transfer Function

Equation 2 shows the mathematical expression that is used to compute the output voltage, V_{OUT}. This equation can also be rearranged algebraically to solve for different terms. For example, during calibration, this equation is rearranged to solve for V_{IN}.

$$V_{OUT} = \left[\left(\text{mux\_sign} \bullet V_{IN} + V_{Coarse\_Offset}\right) \bullet GI + V_{Zero\_DAC}\right] \bullet GD \bullet GO \quad (2)$$

Where:

mux_sign: This term changes the polarity of the input signal; value is ±1. See Table 7-28.

V_{IN}: The input signal for the PGA308; $V_{IN}1 = V_{INP}$, $V_{IN}2 = V_{INN}$.

V_{Coarse_Offset}: The coarse offset DAC output voltage. See Table 7-30.

GI: Input stage gain. Refer to Table 7-29.

V_{Zero_DAC}: Zero DAC output voltage. See Table 7-23.

GD: Gain DAC. Refer to Table 7-25.

GO: Output stage gain. See Table 7-27.

3.2 Offset Scaling

The coarse offset adjust is implemented after the input mux and before the Front-End PGA gain to allow for maximum dynamic range. Many bridge sensors have initial offsets comparable to the respective full-scale outputs. The coarse offset adjust can be applied as positive or negative. The coarse offset adjust polarity is defined in Figure 3-4. Assuming proper input common-mode voltage in the linear input voltage range of the device and a zero differential input voltage into the PGA308, coarse offset adjust polarity is shown as V_{INP} with respect to V_{INN}. A positive polarity for coarse offset adjust causes an increase in V_{OUT} and a negative polarity causes a decrease in V_{OUT}. Coarse offset adjust is implemented in a 7-bit DAC + sign and contains 100 positive selections, 100 negative selections, and '0'.

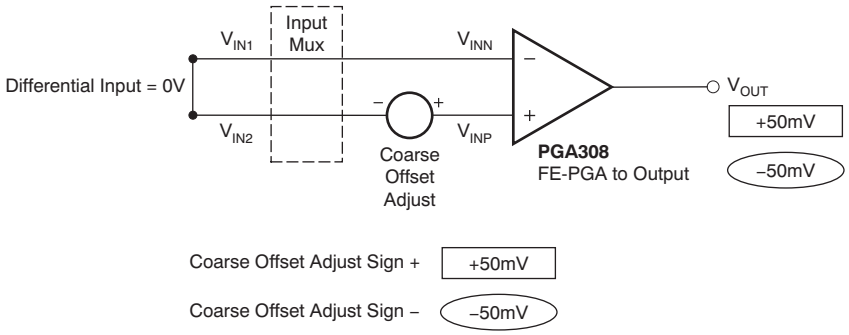


Figure 3-4. Coarse Offset Adjust Polarity

To optimize the range and resolution of the coarse offset adjust for different values of V_{REF}, there is also a coarse offset range selection feature in the PGA308. For COS VR1 = 1 and COS VR0 = 1 (CFG2 Register [D11:D10]) the 4.5V to 5.5V coarse offset reference range is selected. For this range, the resolution in either the positive or negative range is (1/128)(V_{REF})(0.0256). For a +5V reference, this resolution translates to 1mV steps, with a ±100mV range.

Figure 3-5 depicts the PGA308 with the gain settings used for the example bridge sensor application detailed in Figure 3-2 and Figure 3-3. The conversion of the bridge initial differential offset (plus its common-mode) to the differential plus common-mode voltage source model is shown in Figure 3-5, for an initial bridge sensor offset of 34mV (V_{INP} – V_{INN}). Conceptually, this model divides into two 17mV offset voltages with polarities as shown. If the coarse offset adjust is set for –34mV offset (V_{INP} – V_{INN}), then the initial bridge offset is cancelled exactly. Any residual initial bridge offset that has not been cancelled by the coarse offset adjust will be gained up by the Front-End PGA gain and must be accounted for when setting the fine offset adjust by using the Zero DAC. The coarse offset adjust is set by bits OS[7:0] (CFG0 Register [D7:D0], with bit OS7 determining the coarse offset polarity as negative for a '1' and positive for a '0'. The internal architecture of the coarse offset adjust does yield duplicate digital codes for 0V or a (–0 × V_{REF}) and a (+0 × V_{REF}). In addition, digital codes beyond the 100 positive and 100 negative selections result in the maximum positive or maximum negative output, respectively. See Table 7-26 (CFG0 Register) and Table 7-36 (CFG2 Register) in the *Detailed Register Descriptions* section, for a complete mapping of the coarse offset adjust settings.

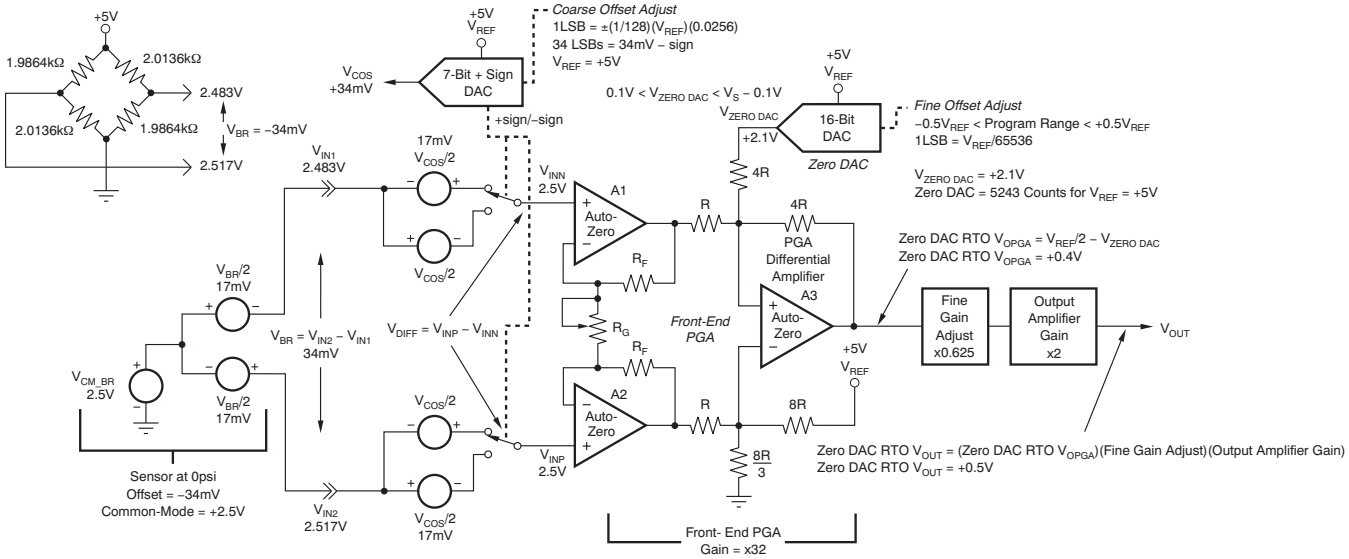
The PGA308 Coarse Offset Adjust DAC circuitry is optimized for a given reference input by programming the PGA308 for the voltage on the V_{REF} pin. The COS VR[1:0] (CFG2 Register [D11:10]) bits select the V_{REF} range to be as close as possible to the voltage on the V_{REF} pin. Table 3-1 shows the coarse offset V_{REF} range selection versus COS VR[1:0] bits along with the coarse offset adjust resolution and range.

Table 3-1. Coarse Offset Reference Voltage Range

COS VR1	COS VR0	Coarse Offset V_{REF} Range (V)	Coarse Offset Resolution (V)	Coarse Offset Range (V)
0	0	1.6 to 2.4	(1/128)(V_{REF})(0.064)	(±100mV)(V_{REF}/2)
0	1	2.4 to 3.6	(1/128)(V_{REF})(0.0427)	(±100mV)(V_{REF}/3)
1	0	3.6 to 4.5	(1/128)(V_{REF})(0.0320)	(±100mV)(V_{REF}/4)
1	1	4.5 to 5.5	(1/128)(V_{REF})(0.0256)	(±100mV)(V_{REF}/5)

The fine offset adjust is set by the Zero DAC. The Zero DAC output voltage, $V_{ZERO\ DAC}$, is scaled through summation with V_{REF} into A3, the difference amplifier of the Front-End PGA, to create an architecture that allows for positive and negative offsets to be summed with (V_{DIFF})(FE GAIN) at the output of A3, V_{OPGA}. The fine offset adjust allows for more flexible scaling when the Coarse Offset Adjust cannot entirely remove the offset voltage of the sensor.

The programmable voltage range at V_{OPGA} as a result of the Zero DAC is $\pm(V_{REF}/2)$, referred-to-output (RTO) of the Front-End PGA. The achievable voltage range out of the Zero DAC is limited to $0.1V < V_{ZERO\ DAC} < V_S - 0.1$ because of its internal output stage. Zero DAC RTO V_{OPGA} is also subjected to the Fine Gain Adjust and Output Amplifier Gain before its effect is seen on V_{OUT}. Zero DAC is used in single-supply systems that are set to a known low-end voltage when the input differential voltage to the PGA308 is zero (V_{DIFF} = 0V). A typical 5V single-supply sensor signal conditioning system can use 0.5V to 4.5V for its linear output range and the range from 0V to 0.5V and 4.5V to 5V for system diagnostic information, such as Over-Scale, Under-Scale, and Fault Detect information. All of these additional features are in the PGA308 (see Section 3.5, *Over-Scale and Under-Scale Limits* and Section 3.6, *Fault Monitor Circuitry*). The 16-bit Zero DAC setting is contained in the ZDAC Register.



Key Front-End PGA Equations

$V_{INP} = V_{CM\_BR} + V_{BR}/2 + V_{COS}/2$
$V_{INN} = V_{CM\_BR} - V_{BR}/2 - V_{COS}/2$

$V_{CM} = (V_{INP} + V_{INN})/2$
$V_{CM} = V_{CM\_BR}$

$V_{DIFF} = V_{INP} - V_{INN}$
$V_{DIFF} = V_{BR} + V_{COS}$

Figure 3-5. Coarse and Fine Offset Adjust

3.3 Zero DAC Circuit Range

The fine offset adjust set by the Zero DAC has a programmable range from $-V_{REF}/2$ to $+V_{REF}/2$, as Figure 3-6 illustrates. The output of the Zero DAC has a buffer op amp with a positive and negative saturation voltage that limits how closely it can swing to ground or to V_S. For a +5V reference, the programmable range of the Zero DAC is –2.5V to +2.5V for Zero DAC RTO V_{OPGA}.

Because of the limitations on the voltage swing (+0.1V to +4.9V) of the Zero DAC output (ideally, 0V to +5V) the usable range of the Zero DAC RTO V_{OPGA} is –2.4V to +2.4V for a reference voltage of +5V. For a reference less than (V_S – 0.1V), this range is skewed to yield full range on the negative side. For example, with V_S= +5V and V_{REF} = +2.5V, the Zero DAC RTO V_{OPGA} range is –1.25V to +1.15V (that is, the programmable range for Zero DAC RTO V_{OPGA} is –1.25V to +1.25V).

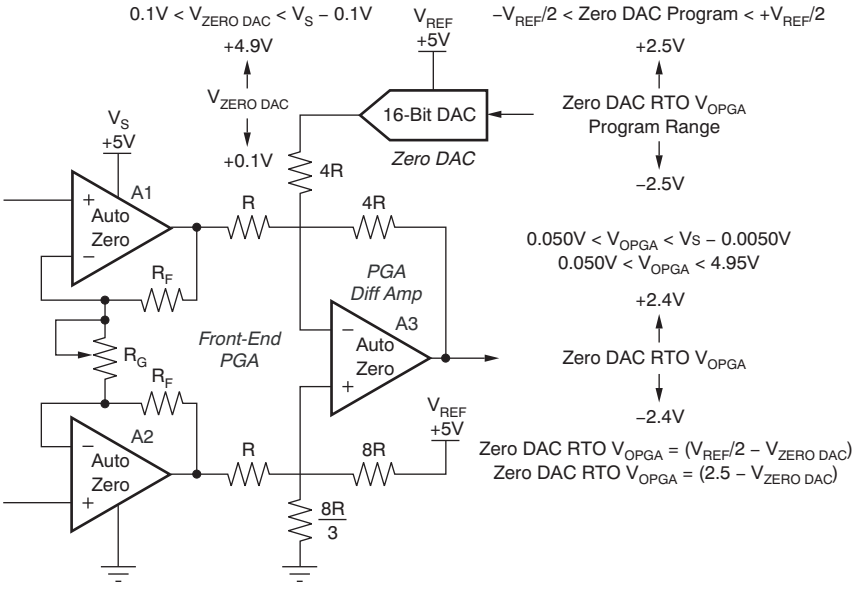


Figure 3-6. Zero DAC Circuit Range

3.3.1 Complete Scaling Example

The following complete scaling example uses the circuit shown in Figure 3-7.

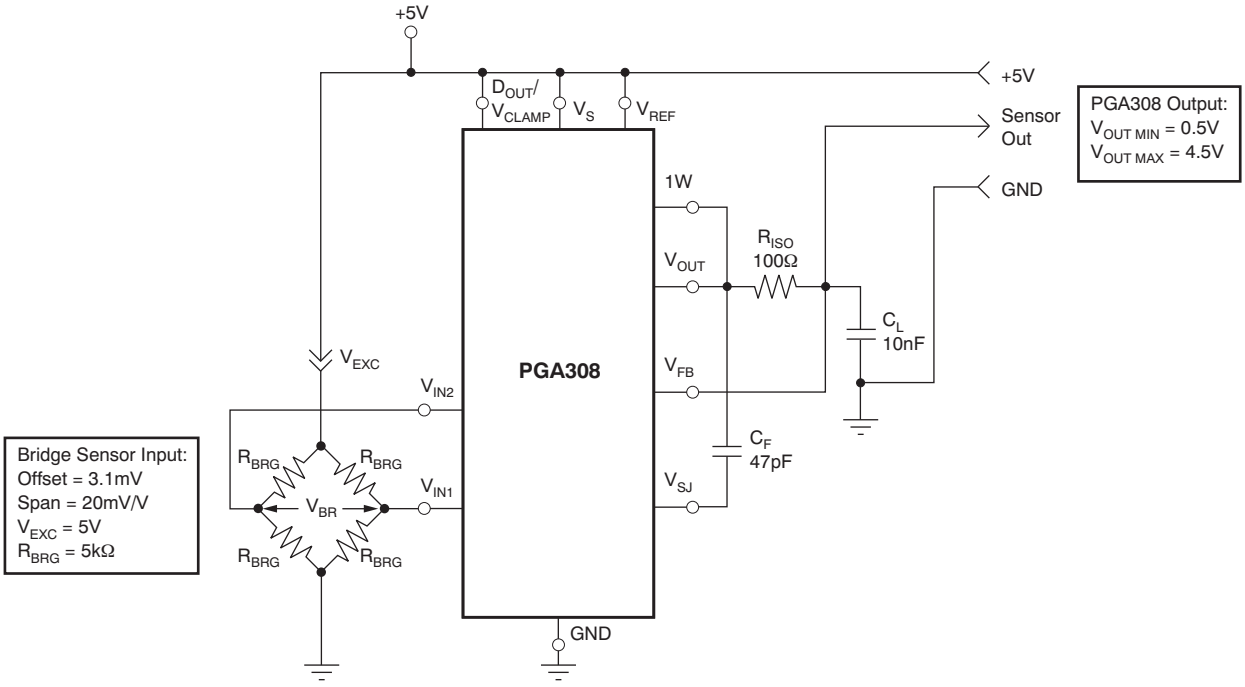


Figure 3-7. Complete Scaling Example Application Circuit

Given system parameters:

V_S := 5V

V_{REF} := 5V

Given bridge sensor input:

Bridge_Offset := 3.1mV/V (V_{BR} offset factor for zero input strain)

Bridge_Span := 20mV/V (V_{BR} offset factor for maximum input strain)

V_{EXC} := 5V

R_{BRG} := 5kΩ

Given desired PGA308 output:

V_{OUT_MIN} := 0.5V

V_{OUT_MAX} := 4.5V

Find PGA308 gain and offset settings:

Coarse Offset DAC

Front-End PGA Gain

Gain DAC

Zero DAC

Output Amplifier

Overview:

Both the voltage reference and bridge excitation voltage are external to the PGA308. Therefore, there are no load considerations on the PGA308 for these voltages. Be sure to use supplies with adequate current drive for V_{REF} and bridge V_{EXC}.

Step 1. Calculate Zero and Full-Scale Bridge Sensor Input:

V_{BR_MIN} := Bridge_Offset × V_{EXC}

V_{BR_MIN} = 0.0155V

V_{BR_MAX} := Bridge_Span × V_{EXC} + Bridge_Offset × V_{EXC}

$V_{BR\_MAX} = (20 \times 10^{-3})(5) + (1.55 \times 10^{-2})(5)$

V_{BR_MAX} = 0.1155V

Step 2. Calculate Total Desired Gain:

G_total := $(V_{OUT\_MAX} - V_{OUT\_MIN})/(V_{BR\_MAX} - V_{BR\_MIN})$

G_total = (4.5V – 0.5V) / (0.1155V – 0.0155V)

G_total = 40

Step 3. Partition Total Desired Gain:

Use Table 3-2 to choose the closest GT to G_total. Table 3-2 is based on setting Gain DAC = midscale (0.6667) for maximum allowance for adjustment at final calibration. GT = V_{OUT} / (V_{IN2} – V_{IN1}).

Choose GT with the largest front-end gain possible for best signal-to-noise ratio. For example, choose GT = 42.6688 → Front-End Gain = 32, Gain DAC = 0.6667, Output Amplifier = 2.

FE_Gain = 32 (Front-End PGA)

Out_Gain = 2 (Output Amplifier)

Table 3-2. PGA308 Total Gain Combinations with Gain DAC = 0.6667

GT	Front-End PGA	Gain DAC	Output Amplifier		GT	Front-End PGA	Gain DAC	Output Amplifier
5.3336	4	0.6667	2		320.0160	200	0.6667	2.4
6.4003	4	0.6667	2.4		400.0200	200	0.6667	3
8.0004	6	0.6667	2		400.0200	100	0.6667	6
8.0004	4	0.6667	3		480.0240	200	0.6667	3.6
9.6005	6	0.6667	2.4		533.3600	400	0.6667	2
9.6005	4	0.6667	3.6		533.3600	200	0.6667	4
10.6672	8	0.6667	2		600.0300	200	0.6667	4.5
10.6672	4	0.6667	4		640.0320	480	0.6667	2
12.0006	6	0.6667	3		640.0320	400	0.6667	2.4
12.0006	4	0.6667	4.5		768.0384	480	0.6667	2.4
12.8006	8	0.6667	2.4		800.0400	600	0.6667	2
14.4007	6	0.6667	3.6		800.0400	400	0.6667	3
16.0008	12	0.6667	2		800.0400	200	0.6667	6
16.0008	8	0.6667	3		960.0480	600	0.6667	2.4
16.0008	6	0.6667	4		960.0480	480	0.6667	3
16.0008	4	0.6667	6		960.0480	400	0.6667	3.6
18.0009	6	0.6667	4.5		1066.7200	800	0.6667	2
19.2010	12	0.6667	2.4		1066.7200	400	0.6667	4
19.2010	8	0.6667	3.6		1152.0576	480	0.6667	3.6
21.3344	16	0.6667	2		1200.0600	600	0.6667	3
21.3344	8	0.6667	4		1200.0600	400	0.6667	4.5
24.0012	12	0.6667	3		1280.0640	960	0.6667	2
24.0012	8	0.6667	4.5		1280.0640	800	0.6667	2.4
24.0012	6	0.6667	6		1280.0640	480	0.6667	4
25.6013	16	0.6667	2.4		1440.0720	600	0.6667	3.6
28.8014	12	0.6667	3.6		1440.0720	480	0.6667	4.5
32.0016	16	0.6667	3		1536.0768	960	0.6667	2.4

Table 3-2. PGA308 Total Gain Combinations with Gain DAC = 0.6667 (continued)

32.0016	12	0.6667	4		1600.0800	1200	0.6667	2
32.0016	8	0.6667	6		1600.0800	800	0.6667	3
36.0018	12	0.6667	4.5		1600.0800	600	0.6667	4
38.4019	16	0.6667	3.6		1600.0800	400	0.6667	6
42.6688	**32**	**0.6667**	**2**		1800.0900	600	0.6667	4.5
42.6688	16	0.6667	4		1920.0960	1200	0.6667	2.4
48.0024	16	0.6667	4.5		1920.0960	960	0.6667	3
48.0024	12	0.6667	6		1920.0960	800	0.6667	3.6
51.2026	32	0.6667	2.4		1920.0960	480	0.6667	6
64.0032	32	0.6667	3		2133.4400	1600	0.6667	2
64.0032	16	0.6667	6		2133.4400	800	0.6667	4
76.8038	32	0.6667	3.6		2304.1152	960	0.6667	3.6
85.3376	64	0.6667	2		2400.1200	1200	0.6667	3
85.3376	32	0.6667	4		2400.1200	800	0.6667	4.5
96.0048	32	0.6667	4.5		2400.1200	600	0.6667	6
102.4051	64	0.6667	2.4		2560.1280	1600	0.6667	2.4
128.0064	64	0.6667	3		2560.1280	960	0.6667	4
128.0064	32	0.6667	6		2880.1440	1200	0.6667	3.6
133.3400	100	0.6667	2		2880.1440	960	0.6667	4.5
153.6077	64	0.6667	3.6		3200.1600	1600	0.6667	3
160.0080	100	0.6667	2.4		3200.1600	1200	0.6667	4
170.6752	64	0.6667	4		3200.1600	800	0.6667	6
192.0096	64	0.6667	4.5		3600.1800	1200	0.6667	4.5
200.0100	100	0.6667	3		3840.1920	1600	0.6667	3.6
240.0120	100	0.6667	3.6		3840.1920	960	0.6667	6
256.0128	64	0.6667	6		4266.8800	1600	0.6667	4
266.6800	200	0.6667	2		4800.2400	1600	0.6667	4.5
266.6800	100	0.6667	4		4800.2400	1200	0.6667	6
300.0150	100	0.6667	4.5		6400.3200	1600	0.6667	6

Step 4. Calculate Gain DAC Value:

Gain_DAC := G_total / [(FE_Gain)(Out_Gain)]

Gain_DAC = 40 / [(32)(2)]

Gain_DAC = 0.625

Step 5. Calculate Coarse Offset:

Bridge_offset = 15.5mV

Coarse Offset Adjust is 1mV with a range of ±100mV for V_{REF} = 5V

(see Table 7-36, *CFG2 Register* and Table 7-37, *Coarse Offset V_{REF} Range Select Register* for details)

Set Coarse Offset as close as possible to V_{BR_MIN}

Coarse_Offset = –15mV → residual error on V_{BR_MIN} = 0.5mV

Coarse_Offset = –15mV

Step 6. Calculate Zero DAC:

V_{OUT_MIN} := [(V_{BR_MIN} + Coarse_Offset)(FE_Gain) + Zero_DACx)](Gain_DAC)(Out_Gain)

Where:

Zero_DACx = Zero DAC RTO V_{OPGA}

Zero_DACx := [V_{OUT_MIN} / (Gain_DAC)(Out_Gain)] – (V_{BR_MIN} + Coarse_Offset)(FE_Gain)

Zero_DACx = [0.5V / (0.625)(2)] – [15.5mV + (–15mV)](32)

Zero_DACx = 0.384V

Step 7. Computed Values Check:

For V_{BR_MIN}, check V_{OUT_MIN} using computed values:

$V_{OUT\_MIN\_compute}$:= [(V_{BR_MIN} + Coarse_Offset)(FE_Gain) + Zero_DACx](Gain_DAC)(Out_Gain)

$V_{OUT\_MIN\_compute}$ = [(15.5mV + {–15mV})(32) + 0.384](0.625)(2)

$V_{OUT\_MIN\_compute}$ = 0.5V

For V_{BR_MAX}, check V_{OUT_MAX} using computed values:

$V_{OUT\_MAX\_compute}$:= [(V_{BR_MAX} + Coarse_Offset)(FE_Gain) + Zero_DACx](Gain_DAC)(Out_Gain)

$V_{OUT\_MAX\_compute}$ = [(115.5mV + {–15mV})(32) + 0.384] (0.625)(2)

$V_{OUT\_MAX\_compute}$ = 4.5V

Step 8. Measured Values:

Program the PGA308 with computed values and take real-world measurements for V_{OUT_MIN} at V_{BR_MIN} and V_{OUT_MAX} at V_{BR_MAX}

$V_{OUT\_MIN\_measure}$:= 0.505315V

$V_{OUT\_MAX\_measure}$:= 4.585756V

These real-world measurements are a result of gain and offset tolerances internal to the PGA308.

Step 9. Adjusted V_{BR} inputs:

Refer all errors between the ideal V_{OUT} and measured V_{OUT} to the input for a final calibration of Gain DAC and Zero DAC

$V_{OUT\_measure}$ = [($V_{BR\_measure}$ + Coarse_Offset)(FE_Gain) + Zero_DAC](Gain_DAC)(Out_Gain)

$V_{BR\_MIN\_measure}$:= [[$V_{OUT\_MIN\_measure}$ / (Gain_DAC)(Out_Gain)] – Zero_DACx] / (FE_Gain) – Coarse_Offset

$V_{BR\_MIN\_measure}$ = [[0.505315V/(0.625)(2)] – 0.384]/(32) – (–15mV)

$V_{BR\_MIN\_measure}$ = 0.015633V

$V_{BR\_MAX\_measure}$ = [[$V_{OUT\_MAX\_MEASURE}$ / (Gain_DAC)(Out_Gain)] - Zero_DACx] / (FE_Gain) – Coarse_Offset

$V_{BR\_MAX\_measure}$ = [[4.585756V / (0.625)(2)] - 0.384] / (32) - (-15mV)

$V_{BR\_MAX\_measure}$ = 0.117644V

Step 10. Calibrated Gain DAC Values:

G_total_measure := (V_{OUT_MAX} – V_{OUT_MIN})/($V_{BR\_MAX\_measure}$ – $V_{BR\_MIN\_measure}$)

G_total_measure = (4.5V – 0.5V) / (0.117644V – 0.015633)

G_total_measure = 39.211448

Gain_DAC_calibrate := (G_total_measure / G_total) × Gain_DAC

Gain_DAC_calibrate = (39.211448 / 40) (0.625)

Gain_DAC_calibrate = 0.612679

Step 11. Calibrated Zero DAC Values:

V_{OUT_MIN} = [($V_{BR\_MIN\_measure}$ + Coarse_Offset)(FE_Gain) + Zero_DAC_calibrate](Gain_DAC_calibrate)(Out_Gain)

Zero_DACx_calibrate := [V_{OUT_MIN} / (Gain_DAC_calibrate × Out_Gain)] – ($V_{BR\_MIN\_measure}$ + Coarse_Offset)(FE_Gain)

Zero_DACx_calibrate = [0.5V / (0.612679)(2)] – [0.015633 + (–15mV)](32)

Zero_DACx_calibrate = 0.387792V

Step 12. Final Calibrated PGA308 Settings:

$V_{BR\_MIN\_measure}$ = 0.015633V, V_{OUT_MIN} = 0.5V
$V_{BR\_MAX\_measure}$ = 0.117644V, V_{OUT_MAX} = 4.5V
V_{EXC} = 5V
Coarse_Offset = –15mV
FE_Gain = 32
Zero_DACx_calibrate = 0.387792V
Gain_DAC_calibrate = 0.612679
Out_Gain = 2

Step 13. For final calibrated settings, check the internal PGA308 nodes for design margin:

(a) Front-End PGA Inputs (refer to Figure 3-5):

V_{INP_MIN}:= (V_{EXC} / 2) + ($V_{BR\_MIN\_measure}$ / 2) + (Coarse_Offset / 2)
V_{INP_MIN} = 2.500316V
V_{INP_MAX}:= (V_{EXC} / 2) + ($V_{BR\_MAX\_measure}$ / 2) + (Coarse_Offset / 2)
V_{INP_MAX} = 2.551322V
V_{INN_MIN}:= (V_{EXC} / 2) – ($V_{BR\_MIN\_measure}$ / 2) – (Coarse_Offset / 2)
V_{INN_MIN} = 2.499684V
V_{INN_MAX}:= (V_{EXC} / 2) – ($V_{BR\_MAX\_measure}$ / 2) – (Coarse)Offset / 2)
V_{INN_MAX} = 2.448678V
For V_S = +5V:
0.2 ≤ Linear Input Voltage Range ≤ V_S – 1.4V
0.2 ≤ Linear Input Voltage Range ≤ 3.6V

V_{INP_MIN}, V_{INP_MAX}, V_{INN_MIN}, and V_{INN_MAX} are all within the allowed Linear Input Voltage Range. The Linear Input Voltage Range specification is at the $V_{IN\ 1}$ and V_{IN2} pins and already includes any coarse adjust effects.

(b) A1, A2 Outputs (refer to Figure 3-2):

FE_Gain = 32 → G = 8
V_{CM_MAX}:= (V_{INP_MAX} + V_{INN_MAX}) / 2
V_{CM_MAX} = 2.5V
V_{DIFF_MAX}:= V_{INP_MAX} – V_{INN_MAX}
V_{DIFF_MAX} = 0.102644V
V_{CM_MIN}:= (V_{INP_MIN} + V_{INN_MIN}) / 2
V_{CM_MIN} = 2.5V
V_{DIFF_MIN}:= V_{INP_MIN} + V_{INN_MIN}
V_{DIFF_MIN} = 0.000633V
V_{OA1_MIN}:= V_{CM_MIN} + G × (V_{DIFF_MIN} / 2)
V_{OA1_MIN} = 2.502531V
V_{OA2_MIN}:= V_{CM_MIN} – G × (V_{DIFF_MIN} / 2)
V_{OA2_MIN} = 2.497469V
V_{OA1_MAX}:= V_{CM_MAX} + G × (V_{DIFF_MAX} / 2)
V_{OA1_MAX} = 2.910576V
V_{OA2_MAX}:= V_{CM_MAX} – G × (V_{DIFF_MAX} / 2)
V_{OA2_MAX} = 2.089424V
For V_S = +5V:
0.1V ≤ V_{OA1}, V_{OA2} ≤ V_S – 0.12V
0.1V ≤ V_{OA1}, V_{OA2} ≤ 4.88V

V_{OA1_MIN}, V_{OA2_MIN}, V_{OA1_MAX}, and V_{OA2_MAX} are all within the allowed V_{OA1}, V_{OA2} output range.

(c) A3 Outputs (refer to Figure 3-2):

FE_Gain = 32, Zero_DACx_calibrate = 0.387792V

V_{OPA_MIN} := (FE_Gain × V_{DIFF_MIN}) + Zero_DACx_calibrate

V_{OPA_MIN} = 0.408V

V_{OPA_MAX} := (FE_Gain × V_{DIFF_MAX}) + Zero_DACx_calibrate

V_{OPA_MAX} = 3.672V

For V_S = +5V:

0.05V ≤ V_{OPGA} ≤ V_S – 0.1V

0.05V ≤ V_{OPGA} ≤ 4.9V

V_{OPA_MIN} and V_{OPA_MAX} are both within the allowed V_{OPGA} output range.

(d) Output Amplifier Input (refer to Figure 3-3):

Gain_DAC_calibrate = 0.612679

V_{OP_MIN} := (V_{OPGA_MIN}) × (Gain_DAC_calibrate)

V_{OP_MIN} = 0.25V

V_{OP_MAX} := (V_{OPGA_MAX}) × (Gain_DAC_calibrate)

V_{OP_MAX} = 2.25V

For V_S = +5V:

0V ≤ V_{OP} ≤ V_S – 1.5V

0V ≤ V_{OP} ≤ 3.5V

V_{OP_MIN} and V_{OP_MAX} are both within the allowed V_{OP} input range.

(e) Output Amplifier V_{OUT} (refer to Figure 3-3):

From our desired PGA308 output:

V_{OUT_MIN} = 0.5V

V_{OUT_MAX} = 4.5V

For V_S = +5V:

0.1V ≤ V_{OUT} ≤ V_S – 0.1V (for 4mA source/sink)

0.1V ≤ V_{OUT} ≤ 4.9V

V_{OUT_MIN} and V_{OUT_MAX} are both within the allowed V_{OUT} output range.

3.4 Output Amplifier

The Output Amplifier portion of the PGA308 is configured to allow maximum flexibility and accuracy in the end application. Figure 3-8 depicts the Output Amplifier in a common three-terminal sensor application. In this application, it is desired to provide overvoltage protection as a result of mis-wires on the output of the PGA308, as well as electromagnetic interference (EMI) and radio frequency interference (RFI) filtering through a 10nF capacitor on the sensor module output. In this configuration, R_{ISO} provides overvoltage protection on $V_{OUT\ FILT}$ to 16V by limiting the current into V_{OUT} to about 150mA [(16V − 0.7V) / 100Ω]. The internal ESD diodes, D_{ESD+} to V_S and D_{ESD-} to GND, cause the 0.7V drop and are sized to accommodate up to ±180mA maximum fault currents. In addition, R_{ISO} serves to isolate the 10nF, RFI/EMI filter, capacitive load from V_{OUT}.

D_Z, a zener diode or unipolar transient suppressor, provides a path for fault current flow because the low-dropout regulator (LDO) cannot sink current. Furthermore, it is undesirable to have V_S on the PGA308 rise above its maximum voltage rating of 5.5V for positive fault currents. For negative fault currents, D_Z will forward-bias to limit negative voltages across the PGA308 from V_S to GND to –0.7V.

Note that the point of feedback around the Output Amplifier, V_{FB}, is taken from $V_{OUT\ FILT}$. Provided there is adequate voltage swing headroom, the Output Amplifier will accurately scale $V_{OUT\ FILT}$ to match the desired conditioned sensor voltage. The V_{FB} pin is protected internally for overvoltages up to ±30V to protect the PGA308 under miswire conditions. If voltages exceed ±30V, then the current into the V_{FB} pin must be current-limited to ±10mA. C_F provides a second feedback path around the Output Amplifier for stability. With the configuration shown, the Output Amplifier is stable for internal Output Amplifier gains from 2 (125kHz bandwidth, 63° loop gain phase margin, CMP SEL = 1) to 6 (64kHz bandwidth, 86° loop gain phase margin, CMP SEL = 1).

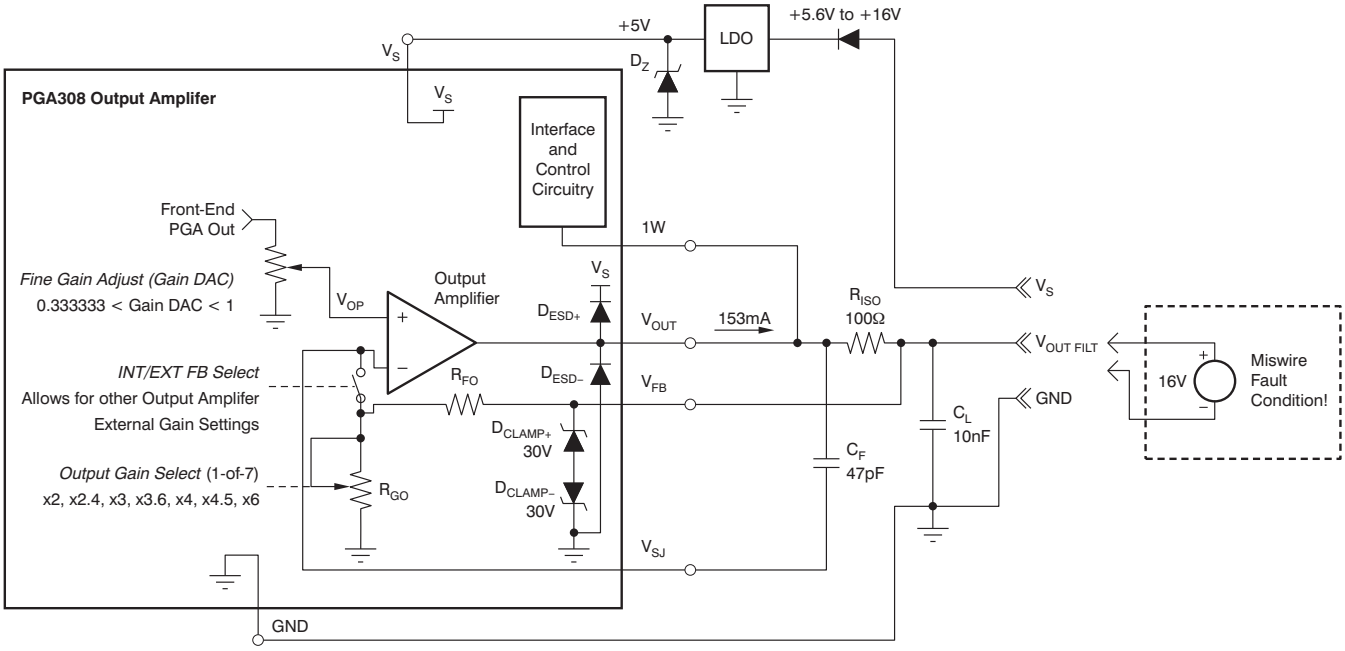


Figure 3-8. Output Amplifier in a Common Three-Terminal Sensor Application

Table 3-3 details the typical Output Amplifier resistor values for R_{FO} and R_{GO} for a selected gain. The Typical Characteristics section of the PGA308 data sheet contains an Open-Loop Output Impedance curve for the Output Amplifier. These values, combined with the typical Output Amplifier Open-Loop Gain curve and standard op amp stability techniques, allow the Output Amplifier to be tailored and configured for a specific sensor application. When using the Over-Scale and Under-Scale Limit circuitry, the Output Amplifier has small signal bandwidth and slew rate differences depending on the CMP SEL bit (CFG1 Register [D11]) setting. See *Section 3.5, Over-Scale and Under-Scale Limits*, for more details.

Table 3-3. Output Amplifier: Gain Select and CFG0 Register Select Bits

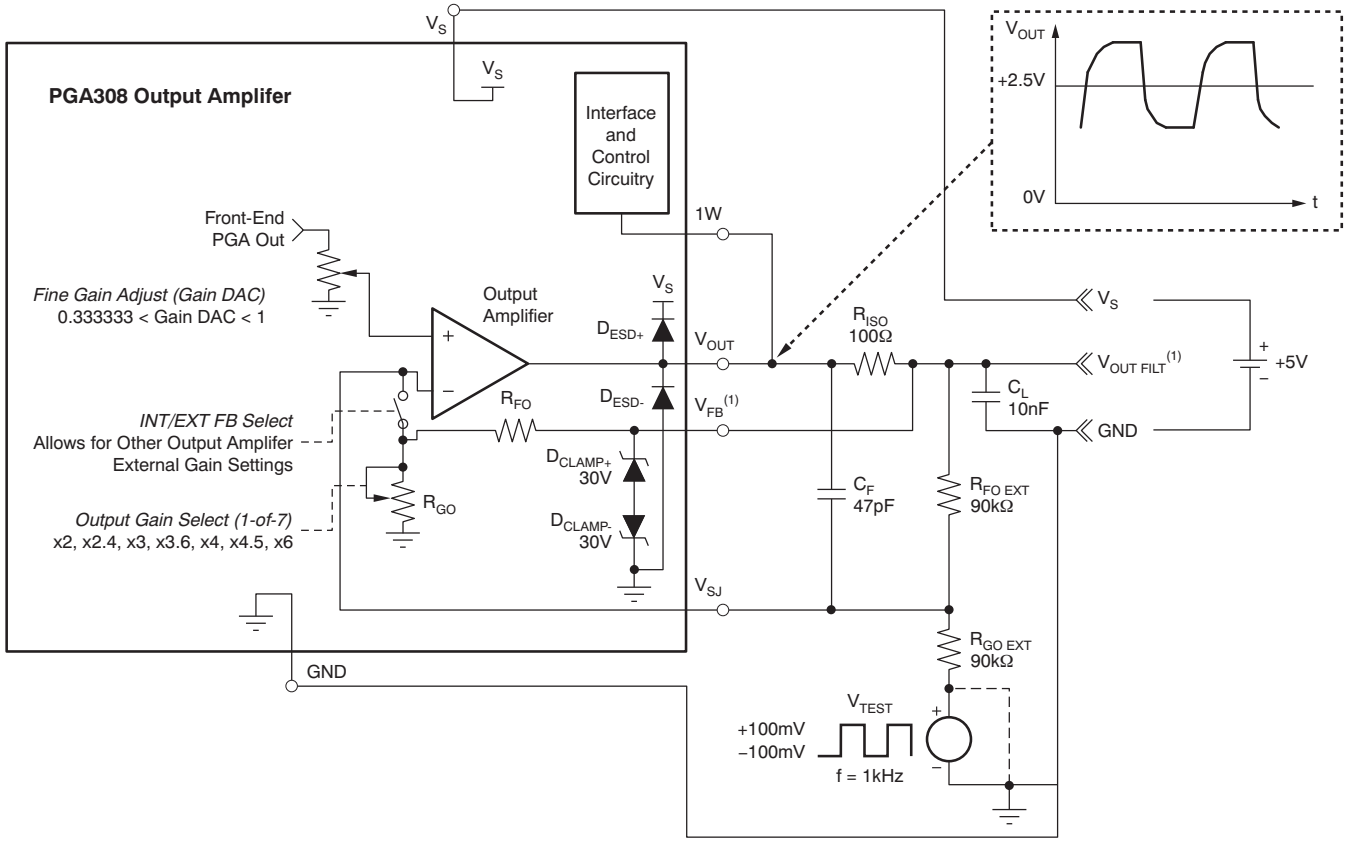
GO2 [D15]	GO1 [D14]	GO0 [D13]	Output Amplifier Gain	R_{FO} (Feedback Resistor) (1)	R_{GO} (Input Resistor) (1)
0	0	0	2	90kΩ	90kΩ
0	0	1	2.4	105kΩ	75kΩ
0	1	0	3	120kΩ	60kΩ
0	1	1	3.6	130kΩ	50kΩ
1	0	0	4.0	135kΩ	45kΩ
1	0	1	4.5	140kΩ	40kΩ
1	1	0	6	150kΩ	30kΩ
1	1	1	Disable Internal Feedback	See note (2)	See note (2)

(1) Refer to the detailed block diagram shown in *Figure 2-1* .

(2) Disable Internal Feedback still leaves 180kΩ between V_{FB} and GND. V_{FB} must be connected to V_{OUT} or $V_{OUT\ FILT}$ for the Over-Scale and Under-Scale circuitry to work properly. See the detailed block diagram shown in *Figure 2-1* .

In addition to using its own internal gain setting resistors, R_{FO} and R_{GO}, the Output Amplifier may use external feedback resistors $R_{FO\ EXT}$ and $R_{GO\ EXT}$, as shown in Figure 3-9. Table 3-3 details the bits used in the CFG0 Register for the desired Output Amplifier gain configurations. To use the external feedback resistors, set GO2, GO1, and GO0 to all '1's.

In addition to allowing external feedback resistors to be used, this configuration provides a convenient mechanism for testing the Output Amplifier stability, even if internal gain settings are to be used. As shown in Figure 3-9, external feedback resistors $R_{FO\ EXT}$ and $R_{GO\ EXT}$ are both set to 90kΩ, equivalent to the typical resistor values used for an internal gain setting of 2. A small-signal transient response for the Output Amplifier can be measured at V_{OUT} by biasing V_{OUT} to midscale (+2.5V for V_S = +5V) through the Zero DAC, setting V_{DIFF} = 0V, and using a signal generator to inject a 200mV_{PP} square wave (1kHz) into the end of $R_{GO\ EXT}$. Standard stability transient response criteria for a dominant two-pole system can then be used to determine suitable phase margin based on the measured overshoot and ringing on V_{OUT}. Note that despite the fact that the internal gain-setting resistors ®$_{FO}$ and R_{GO}) are not being used the V_{FB} pin must be connected to $V_{OUT\ FILT}$ as shown in Figure 3-9 to use the Over-Scale and Under-Scale amplifiers.



(1) V_{FB} must be connected to $V_{OUT\ FILT}$ in order to use the Over-Scale and Under-Scale amplifiers.

Figure 3-9. Output Amplifier Using External Feedback Resistors $R_{FO\ EXT}$ and $R_{GO\ EXT}$

For low-supply applications, the minimum gain for the Output Amplifier is related to its common-mode input range and output voltage swing. In Figure 3-10, the power supply is lowered to +2.7V. The tested common-mode input range of the Output Amplifier is 0V to V_S − 1.5V, as indicated in Figure 3-10. The output voltage swing is tested to be 0.1V to +2.6V for a 4mA load, as shown. This tested result calculates to a minimum gain of 2.08 (ΔV_{OUT} / ΔV_{IN}). For best performance, the Output Amplifier should be scaled for a minimum gain of 2.4 for this application. Usually, this common-mode input range is only a factor at lower voltages but is easily checked for each individual application. At higher supplies, the common-mode input range is not an issue unless external feedback is selected and the Output Amplifier is connected in unity gain. Because the minimum internal feedback of the Output Amplifier only allows a minimum gain of 2, the common-mode input range is not an issue at supply voltages greater than 2.8V.

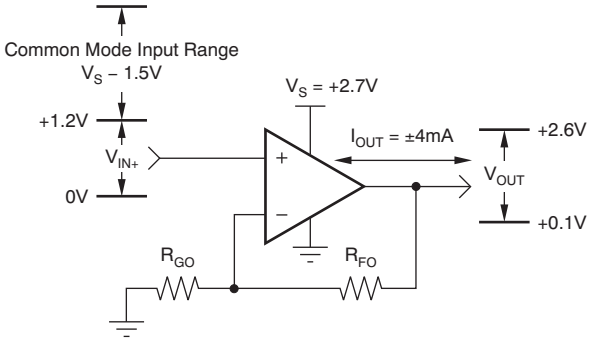
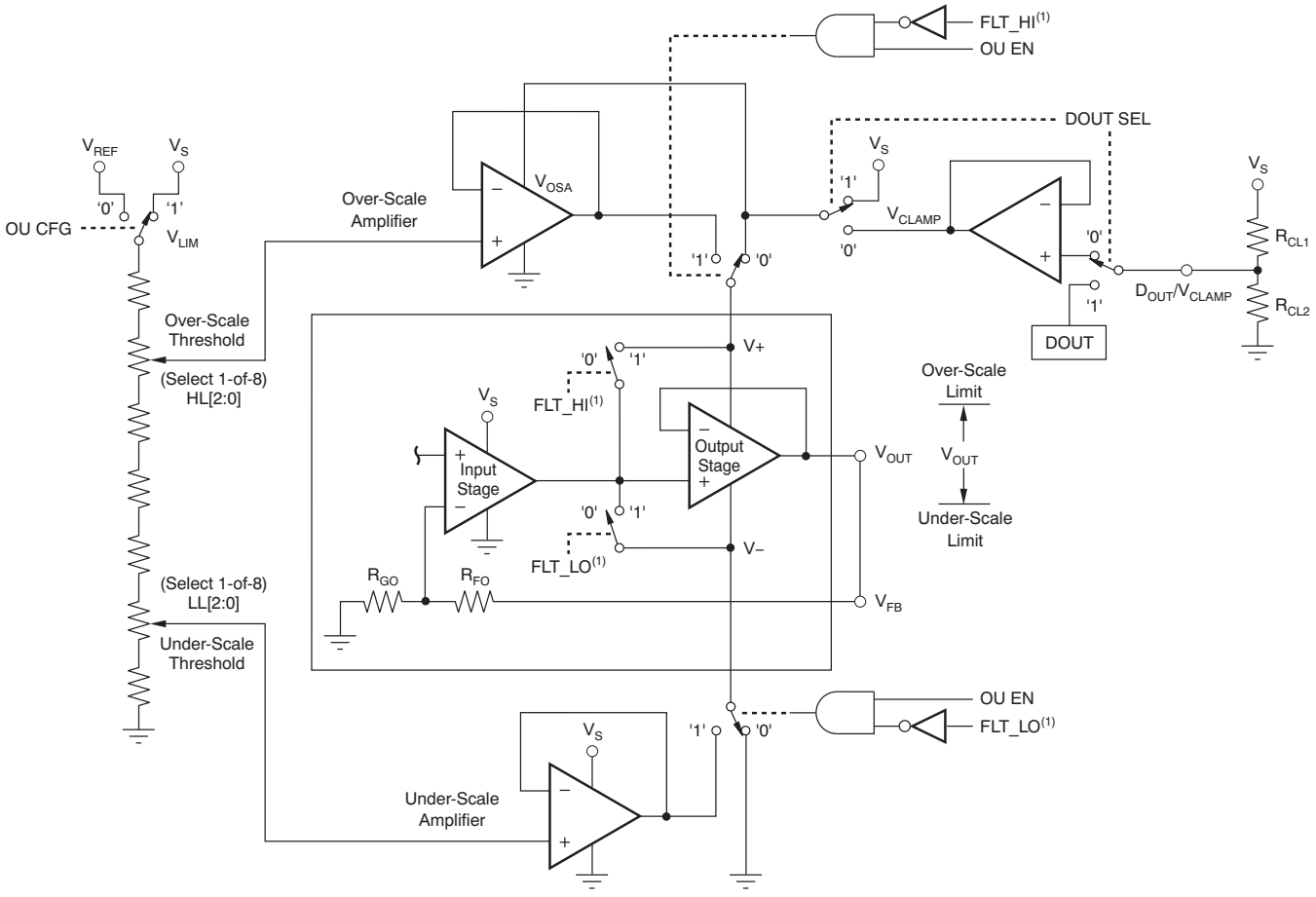


Figure 3-10. Output Amplifier Minimum Gain at Low Supply

3.5 Over-Scale and Under-Scale Limits

The Over-Scale and Under-Scale Limit circuitry provides programmable upper and lower clip limits for the PGA308 output voltage. When combined with the Fault Monitor circuitry, system diagnostics can be performed to determine if a conditioned sensor is defective or if the process being monitored by the sensor is out of range. Figure 3-11 details the key sections of the Over-Scale and Under-Scale Limit circuitry.



(1) See Figure 3-16 for the logic that generates FLT_HI and FLT_LO.

Figure 3-11. Over-Scale and Under-Scale Limit Circuit

The reference for the Over-Scale and Under-Scale Limit circuit is selectable by the OU CFG bit (CFG1 Register [D13]). If OU CFG is '0', then the reference is the voltage on the V_{REF} pin of the PGA308, which allows for limit-scaling referenced to the same reference that an ADC would use in the system. If OU CFG is '1', then V_S is used as the reference voltage, which allows for cases where a low-voltage external reference is used to excite a sensor to minimize sensor power dissipation, but output scaling that is gained up to the wider voltage range of V_S is still desired. The Zero DAC and Coarse Offset will be referenced to the same low-voltage external reference for better accuracy because the Over-Scale and Under-Scale limits are used for system diagnostics and not precise analog signal conditioning.

The Over-Scale threshold is set by HL[2:0] (CFG1 Register D[5:3]). One of eight divided voltages of V_{LIM} (from 0.5703 × V_{LIM} to 0.9805 × V_{LIM}) can be selected. The Under-Scale threshold is set by LL[2:0] (CFG1 Register D[2:0]). One of eight divided voltages of V_{LIM}, from 0.01953 × V_{LIM} to 0.0.0547 × V_{LIM} can be selected. The resistor divider ratios are very accurate, with the dominant threshold error being the input offset voltage of the Over-Scale Amplifier and Under-Scale Amplifier, respectively.

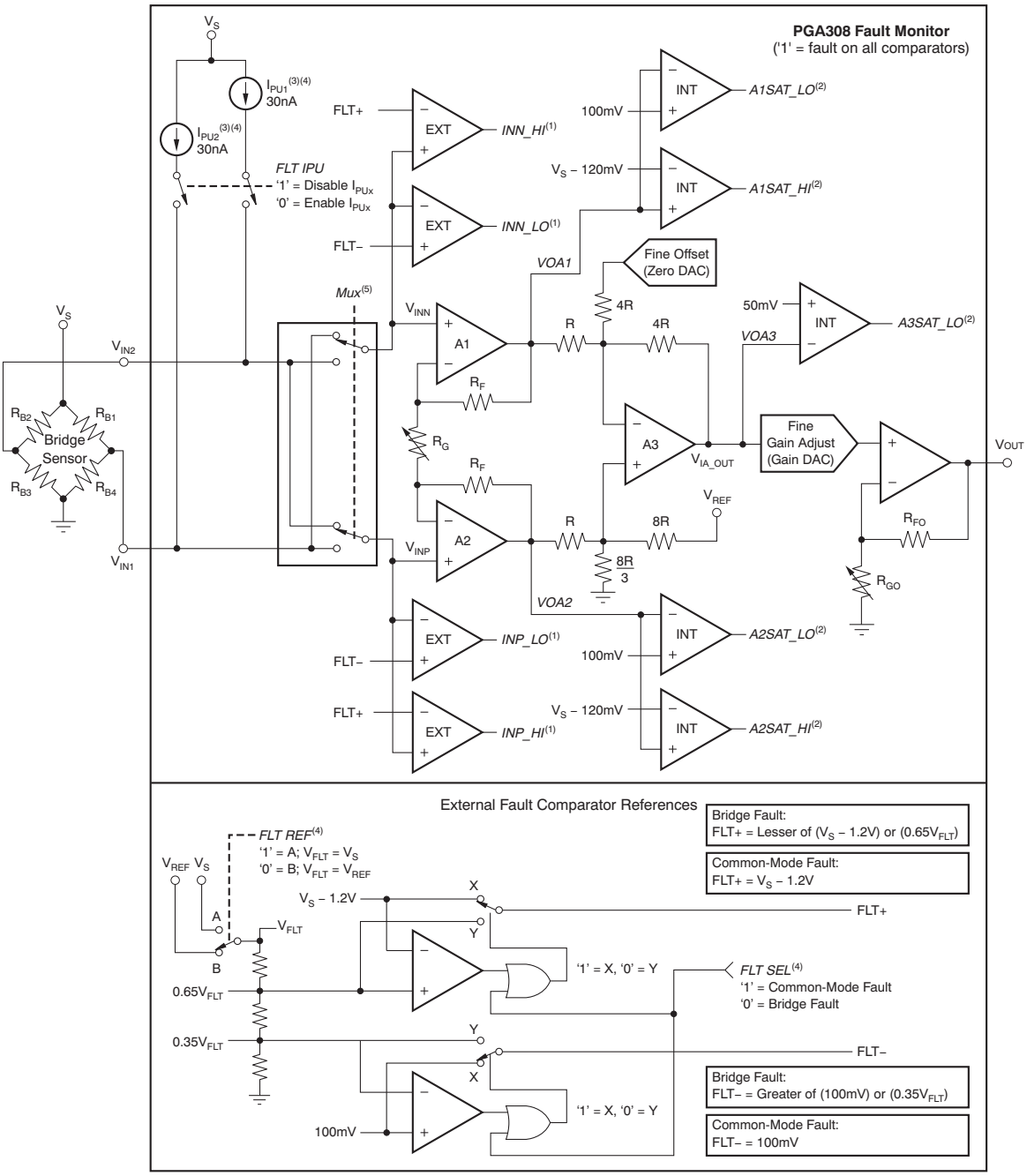
When enabled by the OU EN bit (CFG1 Register [D6]), the Over-Scale and Under-Scale amplifiers can be viewed as acting as the power-supply rails for the Output Amplifier. Therefore, under non-fault conditions, V_{OUT} of the PGA308 cannot swing outside of the Over-Scale and Under-Scale limits. The Over-Scale and Under-Scale amplifiers can be overridden by the Fault Monitor Circuitry to force the minimum level of V_{OUT} to ground, if FLT_LO is logic 1 (see Figure 3-16, *Fault Monitor Logic and Fault Level Selection*).

The maximum level of V_{OUT} can be forced to go above the Over-Scale limit when a fault is detected by the FLT_HI signal going to logic 1 (see Figure 3-16, *Fault Monitor Logic and Fault Level Selection*). When FLT_HI is logic 1, V_{OUT} is determined by the status of the DOUT SEL bit (CFG2 Register [D8]). If DOUT SEL is logic 0, then the V_{CLAMP} circuit is selected and V_{OUT} maximum is set by an external resistor divider or voltage source connected to the D_{OUT}/V_{CLAMP} pin. Note that in this mode, V_{OUT} max is limited to V_{CLAMP} regardless of whether or not the Over-Scale threshold is set higher than V_{CLAMP}, as shown in Figure 3-11, where V_{OSA} is the Over-Scale amplifier positive power supply. If DOUT SEL is logic 1, the V_{OUT} maximum is determined by V_S minus the saturation voltage of the Output Amplifier output stage.

Consider the stability of the Over-Scale and Under-Scale amplifiers when connecting capacitive loads to V_{OUT}, either through an isolation resistor (R_{ISO}) as shown in Figure 3-9, or with no isolation resistor. There is a selectable compensation in the PGA308 to give clean transitions into and out of the Over-Scale and Under-Scale limit regions of operation. The CMP SEL bit (CFG1 Register [D11]) defaults to logic 0 for light compensation and is preferred for loads less than 200pF. The CMP SEL bit must be set to logic 1 for loads greater than 1nF. This compensation is designed to work effectively for capacitive loads up to 10nF. The Over-Scale and Under-Scale amplifiers are highly integrated into the Output Amplifier. In the actual silicon, there are small-signal bandwidth and slew rate considerations for each of the CMP SEL bit settings. See the PGA308 data sheet (SBOS440) typical characteristic curves and electrical characteristics for more details.

3.6 Fault Monitor Circuitry

Fault monitoring on the PGA308 is provided through nine internal comparators; refer to Figure 3-12. These comparators are grouped into two sets: internal fault comparators and external fault comparators. In Figure 3-12, these comparators are denoted by *EXT* for those in the External Fault Comparator group and by *INT* for those in the internal fault comparator group. The external fault comparators focus on bridge sensor fault detection while the internal fault comparators monitor key internal nodes for voltage violations that could result in improper V_{OUT} voltages as a result of internal node saturations.



(1) External fault comparator group.

(2) Internal fault comparator group.

(3) I_{PU1} and I_{PU2} (register-selectable for enable/disable) are needed for fault detection of opens on V_{IN1} and V_{IN2}.

(4) CFG1 register select bits.

(5) POR mux state shown.

Figure 3-12. Fault Monitor Comparators

The internal fault comparators monitor the Front-End PGA internal nodes of the PGA308 (see Figure 3-12). When PGA308 + Sensor calibration is in process, it is crucial to have the internal comparator group enabled because it can alert the user to an internal node violation. Such a violation may yield an output voltage within the expected linear range, but it will not be accurate. Each of the Front-End PGA amplifiers, A1 and A2, has the respective output monitored for both saturation to the positive supply or to ground. If either comparator trips during calibration, it is an indication of an out-of-range scaling condition as a result of either an incorrect Front-End PGA gain select or a coarse offset adjust. The A3 amplifier in the Front-End PGA is also monitored for negative swing violations that can occur if the Zero DAC is incorrectly combined with the Front-End PGA gain select.

To understand the use of the external fault comparators, it is important to review some common bridge sensor configurations. Many bridge sensors have a very large temperature coefficient of bridge resistance (for example, 3500ppm/°C). The temperature coefficient of the bridge is often used (after calibration) to detect the temperature of the bridge sensor and compensate for bridge changes in offset and span with temperature. The compensation is accomplished by changing the Gain DAC and Zero DAC in the PGA308 through the use of an external microcontroller.

Figure 3-13 shows two cases of common bridge sensor configurations without temperature sense. *Case 1: Straight Bridge* uses V_{EXC} directly across the bridge. *Case 2: Reduced Bridge Excitation* adds equivalent value resistors in the top ®$_{EXC+}$) and bottom ®$_{EXC-}$) of the bridge to reduce the applied V_{EXC} voltage. This configuration is used in applications where an accurate voltage is used on the PGA308 V_{REF} pin but a lower net voltage across the bridge excitation pins is desired to minimize self-heating of the bridge sensor.

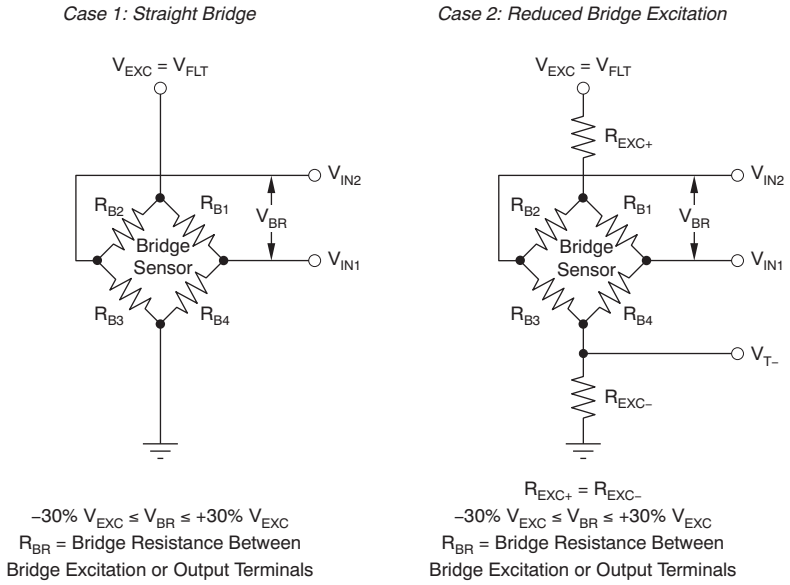


Figure 3-13. Bridge Sensor Configuration without Temperature Sense

Figure 3-14 shows two cases of common bridge sensor configurations with temperature sense. *Case 3: Bottom Bridge Temperature Sense* uses a resistor in the bottom of the bridge (R_{T-}) to provide a method of measuring a voltage (V_{T-}) that is proportional to bridge temperature. The recommended maximum value for R_{T-} is 10%of R_{BR}, where R_{BR} is the terminal resistance of the bridge sensor. *Case 4: Top Bridge Temperature Sense* uses a resistor in the top of the bridge (R_{T+}) to provide a method of measuring a voltage, (V_{T+}) that is proportional to bridge temperature. The recommended maximum value for R_{T+} is 10% of R_{BR}, where R_{BR} is the terminal resistance of the bridge sensor. This technique allows the voltage across R_{T+} to be measured relative to V_{EXC}, which has system advantages in some applications.

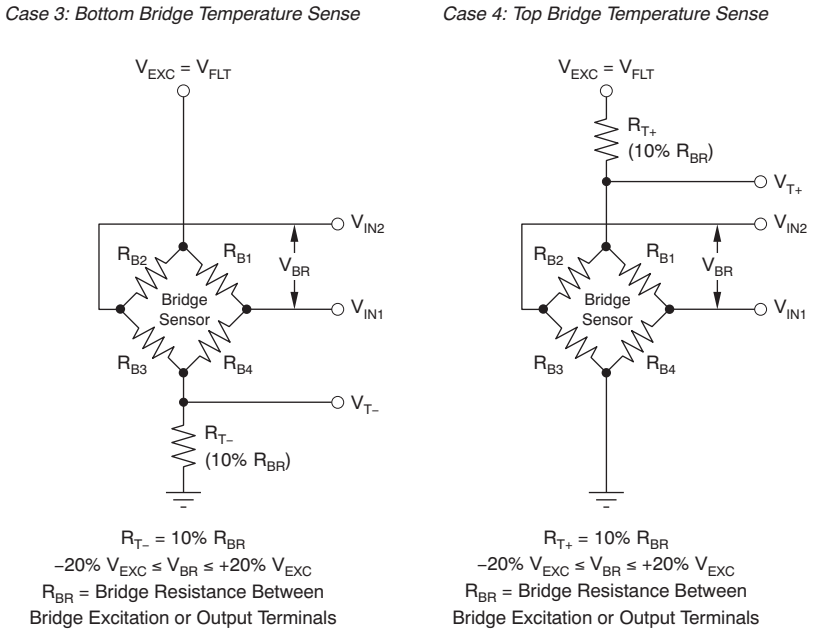


Figure 3-14. Bridge Sensor Configuration with Temperature Sense

The external fault comparator group has a choice of both fault reference and fault detection configurations, as shown in Figure 3-12. For bridge sensor applications, it is recommended to use the bridge fault configuration by setting FLT SEL = 1 (CFG1 Register [D12]). In this mode, the primary upper trip reference (FLT+) for the external fault comparators is the lesser of 0.65 × V_{FLT} or V_S – 1.2V. The primary lower trip reference (FLT–) is the greater of 0.35 × V_{FLT} or 100mV. These thresholds are designed to catch any of the bridge fault cases detailed in Table 3-4.

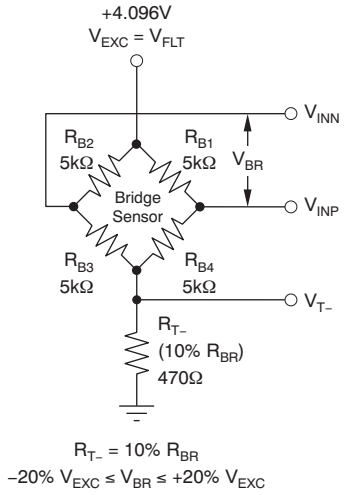
There is also a choice of setting V_{FLT} (the reference voltage to generate FLT+ and FLT–) between V_S or V_{REF}. This option gives optimum flexibility in system configurations where the bridge may be excited by a different voltage than the V_{REF} pin. The FLT REF bit (CFG1 Register [D15]) selects the external fault comparator reference between V_S (logic 1) or V_{REF} (logic 0).

The other fault detect configuration is common-mode fault. In this configuration, FLT+ is fixed at V_S – 1.2V, and FLT– is fixed at 100mV. The common-mode fault configuration trips the external fault comparators if either of the inputs into the Front-End PGA, V_{INN} or V_{INP}, are outside of the input voltage range. The input voltage range is 0.2V to (V_S – 1.4V). FTL+ and FLT– are set just beyond this range to trip in a faulted input condition and yet not trip erroneously if the input voltage is getting close to the specified range. This configuration can prove useful when using the PGA308 as a general-purpose instrumentation amplifier input with programmable gain.

For the Bridge Fault configuration, there is also a limit to the maximum input differential signal (V_{INP} – V_{INN} or V_{BR}) that can be applied to the PGA308 inputs without tripping an external fault comparator. For V_{FLT} set to V_{EXC}, the allowable V_{BR} for common bridge applications is shown in Figure 3-13 and Figure 3-14. For most bridge applications, these ranges are adequate and allow the Bridge Fault configuration to detect any and all faults described in Table 3-4. If a bridge application cannot be limited to these V_{BR} ranges and fault detection is still desired, the common mode fault configuration can be selected with application-specific analysis performed to ensure that all faults can be detected.

If fault detection of floating inputs (that is, the sensor is disconnected entirely from one or both of the PGA308 inputs) is to be accurately reported, it is necessary to add pull-up current sources (I_{PU1} and I_{PU2}) to each input (V_{IN1} and V_{IN2}) shown in Figure 3-12 because of the extremely low input bias currents of the PGA308. These 30nA (typ) current sources are designed to be large enough to overcome ESD cell leakages and force the external fault comparators into a fault-detected state for open PGA308 inputs. For most sensor applications, this additional current will only add a common-mode shift because the difference between the pull-up current sources is 2nA (typ). The FLT IPU bit (CFG1 Register [D14]) enables I_{PU1} and I_{PU2} with a logic 0, and disables them with a logic 1.

Figure 3-15 and Table 3-4 illustrate how the external fault comparators work to detect bridge sensor faults. The bridge sensor configuration in Figure 3-15 (bottom bridge temperature sense) was chosen because it highlights the capability of the fault monitor circuitry to detect faults; a straight bridge configuration is the easiest configuration to detect bridge faults.



PGA308 Configuration:
V_S = +5V
V_{REF} = +4.096V
Front-End PGA Gain = x4 (A1 = x1, A2 = x1, A3 = x4)
Zero DAC RTO VOPGA = 0.5V
Gain DAC = x0.5
Output Amplifier Gain = x2
$V_{FLT} = V_{EXC}$ = 4.096V
$0.65V_{FLT}$ = 2.6624V
$0.35V_{FLT}$ = 1.4336V
Bridge Fault Configuration

Figure 3-15. Bridge Fault Example: Bottom Bridge Temperature Sense

Table 3-4. Bridge Fault Example: Bottom Bridge Temperature Sense

Case	V_{INP}	V_{INN}	INP_HI	INP_LO	INN_HI	INN_LO	VOA1	A1SAT_HI	A1SAT_LO	VOA2	A2SAT_HI	A2SAT_LO	VOA3	A3SAT_LO
Normal	2.2240	2.2240	0	0	0	0	2.2240	0	0	2.2240	0	0	0.5000	0
R_{B1} Open (1)	0.1840	2.1400	0	1	0	0	2.1400	0	0	0.1840	0	0	<0.050	1
R_{B2} Open (1)	2.1400	0.1840	0	0	0	1	0.1840	0	0	2.1400	0	0	>4.9	0
R_{B3} Open	2.1400	4.0960	0	0	1	0	4.0960	0	0	2.1400	0	0	<0.050	1
R_{B4} Open	4.0960	2.1400	1	0	0	0	2.1400	0	0	4.0960	0	0	>4.9	0
R_{B1} Short	4.0960	2.3011	1	0	0	0	2.3011	0	0	4.0960	0	0	>4.9	0
R_{B2} Short	2.3011	4.0960	0	0	1	0	4.0960	0	0	2.3011	0	0	<0.050	1
R_{B3} Short (1)	2.3011	0.5062	0	0	0	1	0.5062	0	0	2.3011	0	0	>4.9	0
R_{B4} Short (1)	0.5062	2.3011	0	1	0	0	2.3011	0	0	0.5062	0	0	<0.050	1
Open Sensor GND	4.0960	4.0960	1	0	1	0	4.0960	0	0	4.0960	0	0	0.5000	0
Open Sensor V_{EXC}	0.0000	0.0000	0	1	0	1	<0.1	0	1	<0.1	0	1	0.5000	0
V_{EXC} Short to GND (2)	0.0000	0.0000	1	1	1	1	<0.1	0	1	<0.1	0	1	0.5000	0
V_{INP} Open	5.0000	2.2240	1	0	0	0	2.2240	0	0	>4.9	1	0	>4.9	0
V_{INN} Open	2.2240	5.0000	0	0	1	0	>4.9	1	0	2.2240	0	0	<0.050	1
V_{INP} Short to GND	0.0000	2.1324	0	1	0	0	2.1324	0	0	<0.1	0	1	<0.050	1
V_{INN} Short to GND	2.1324	0.0000	0	0	0	1	<0.1	0	1	2.1324	0	0	>4.9	0
V_{INP} Short to V_{EXC}	4.0960	2.3011	1	0	0	0	2.3011	0	0	4.0960	0	0	>4.9	0
V_{INN} Short to V_{EXC}	2.3011	4.0960	0	0	1	0	4.0960	0	0	2.3011	0	0	<0.050	1
V_{INP}, V_{INN} Open	5.0000	5.0000	1	0	1	0	>4.9	1	0	>4.9	1	0	0.5000	0
V_{INP}, V_{INN} Short to GND	0.0000	0.0000	0	1	0	1	<0.1	0	1	<0.1	0	1	0.5000	0
V_{INP}, V_{INN} Short to V_{EXC}	4.0960	4.0960	1	0	1	0	4.0960	0	0	4.0960	0	0	0.5000	0

(1) These bridge fault conditions cannot be detected in common-mode fault configuration.
(2) This bridge fault would not have been detected in bridge fault configuration without the FLT circuitry that selects FLT– equal to the greater of 100mV or (0.35 × V_{FLT}).

Figure 3-16 provides an equivalent logic diagram of the PGA308 fault monitor logic and fault selection functions. Each individual Internal and external fault comparator output can be read through the One-Wire interface. The current results are stored in the ALRM Register [D8:D0] with the respective bit names corresponding to the fault comparator outputs as detailed in Figure 3-12 and Figure 3-16.

When the PGA308 output is enabled, the values of the ALRM Register bits reflect the current state of the fault comparators. When V_{OUT} is disabled, the values of the bits in the register indicate the respective comparator status immediately before the output was disabled. The ALRM Register allows for easier identification and debugging of a three terminal sensor module (1W shorted to V_{OUT}). See Section 2.11, *One-Wire Operation with 1W Connected to V_{OUT}* , for details. In addition, each group of comparators (internal fault and external fault) can be programmed such that if any comparator in the respective group is logic high, indicating a fault, the PGA308 output (V_{OUT}) will be forced to a fault that indicates voltage of either a high fault or low fault level beyond the calibrated linear output voltage range of V_{OUT}.

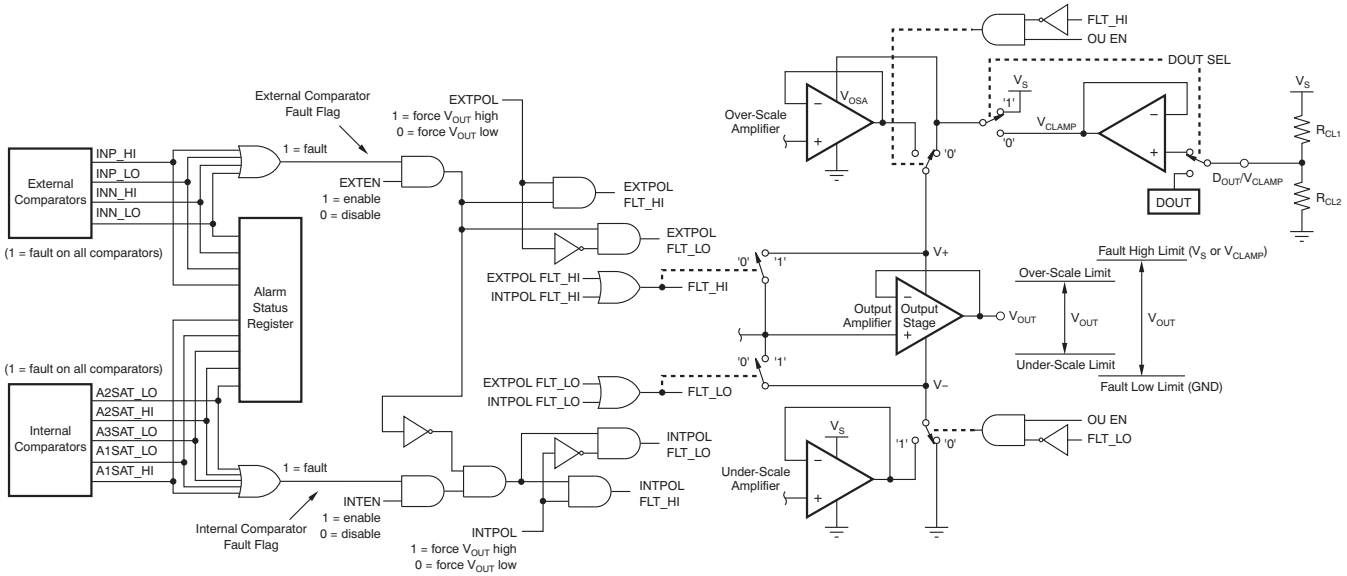


Figure 3-16. Fault Monitor Logic and Fault Level Selection

Refer to Figure 3-16 for the following detailed discussion of selecting and using the Fault Monitor Logic and Fault Selection functions.

The individual comparator outputs in both the internal and external fault comparator groups are combined to generate an internal comparator fault flag and an external comparator fault flag. For the external comparator group, EXTEN (CFG1 Register [D10]) determines whether the external comparator fault flag will be sent forward to force V_{OUT} to a fault indication state. For the internal comparator group, INTEN (CFG1 Register [D9]) determines whether the internal comparator fault flag will be sent forward to force V_{OUT} to a fault indication state. A fault indication on V_{OUT} can be programmed as either a low fault (V_{OUT} driven to GND) or a high fault (V_{OUT} driven to V_S or V_{CLAMP}). A low fault indication will be the negative saturation voltage on V_{OUT} (0.1V for 4mA sink). High fault indication will depend on the DOUT SEL bit (CFG2 Register [D8]), which sets the D_{OUT}/V_{CLAMP} pin as either a digital output function or as a V_{CLAMP} function.

If DOUT SEL is logic 1 (D_{OUT}/V_{CLAMP} pin = digital output function) then a high fault indication will be positive saturation of V_{OUT} to V_S (V_S – 0.1V for 4mA source). If DOUT SEL is logic 0 (D_{OUT}/V_{CLAMP} pin = V_{CLAMP} function) then a high fault indication will be the positive saturation of V_{OUT} to V_{CLAMP} (V_{CLAMP} – 0.1V for 4mA source), where V_{CLAMP} is the external voltage set on the D_{OUT}/V_{CLAMP} pin.

For each of the comparator groups, the fault indication state on V_{OUT} is programmable as either high fault or low fault. INT POL (CFG1 Register [D7]) selects this state for the internal comparator group, and EXTPOL (CFG1 Register [D8]) selects this state for the external comparator group.

The external comparator fault flag has priority over the internal comparator fault flag, as shown in Figure 3-16. For example, if the internal fault comparator group is set to force V_{OUT} to a low fault and the external fault comparator group is set to force V_{OUT} to a high fault, and both groups detect a fault (which is possible if both are enabled), then the external fault comparator group takes precedence and V_{OUT} is forced to a high fault, indicating a sensor fault was detected. This detection priority ensures that for most real-world applications, a critical sensor fault will be reported as a priority over an internal node violation. At the time of a detected fault, the fault logic always prevails (if enabled), and will override the linear output or the Over-Scale or Under-Scale limits (if enabled) to indicate a fault on V_{OUT} as a high fault level or a low fault level.

3.7 D_{OUT}/V_{CLAMP} Pin

The D_{OUT}/V_{CLAMP} pin is selectable as either a push/pull digital output pin or as a V_{CLAMP} input pin. The DOUT SEL bit (CFG2 Register [D8]) sets the D_{OUT}/V_{CLAMP} pin as either a digital output function (DOUT SEL = 1) or as a V_{CLAMP} function (DOUT SEL = 0).

In the Digital Output Function Mode, the DOUT bit (CFG2 Register [D7]) determines whether the D_{OUT}/V_{CLAMP} pin is logic high or logic low. The D_{OUT}/V_{CLAMP} pin in D_{OUT} Mode is a push/pull digital output. The value in the DOUT bit may be preprogrammed in OTP, or controlled through the One-Wire interface (1W pin). The POR value for DOUT SEL is 0', which configures D_{OUT}/V_{CLAMP} as a high-impedance input in V_{CLAMP} Mode.

In V_{CLAMP} Mode, the Output Amplifier output, V_{OUT}, is limited to the voltage applied to the D_{OUT}/V_{CLAMP} pin (see Figure 3-17). V_{CLAMP} Option 1 shows an implementation for a bridge sensor module that is powered from +5V. This option allows maximum voltage for the V_{EXC} of a bridge sensor. This module will be scaled for a linear output of 0.3V to 3.0V, with the Over-Scale Limit set to 3.13V and the Under-Scale Limit set to 0.18V. A bridge sensor fault condition will drive V_{OUT} high. However, because this sensor module is intended to interface with a 3.3V microcontroller, V_{OUT} must not be driven as high as V_S (+5V). If V_{OUT} goes to +5V, it will turn on the ESD structures inside the microcontroller ADC input. This action can cause the microcontroller to latch up, and requires a power cycle to recover. Instead, use a resistor divider to create a 3.3V V_{CLAMP} set point on the D_{OUT}/V_{CLAMP} pin. In V_{CLAMP} Mode, the D_{OUT}/V_{CLAMP} pin is a high-impedance input (200nA typ); therefore, a resistor divider from V_S will work. If the PGA308 is being used local to the microcontroller as a programmable instrumentation amplifier front-end, then the microcontroller power supply can be connected directly to the D_{OUT}/V_{CLAMP} pin in order to set the V_{CLAMP} voltage such that it can never exceed the microcontroller supply voltage of +3.3V (see Figure 3-17, V_{CLAMP} Option 2). In this configuration, both R_X and C_X provide noise filtering.

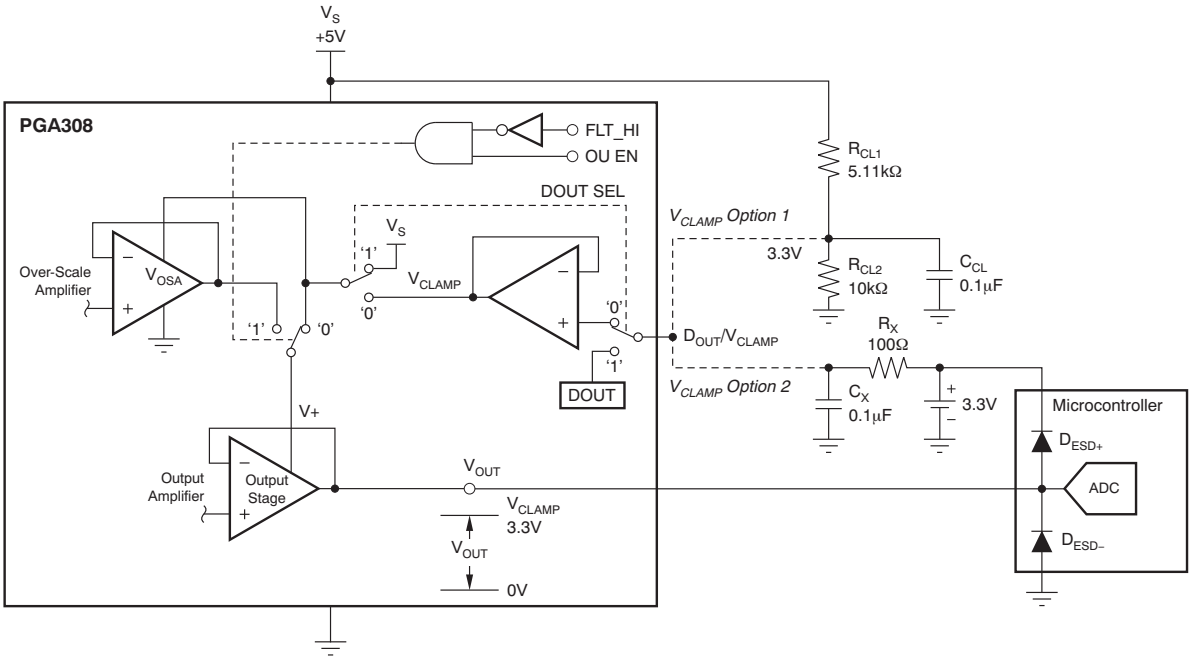


Figure 3-17. D_{OUT}/V_{CLAMP} Function

3.8 System Budget for Over-Scale, Under-Scale, Linear Output, and Fault Detection

The many features of the PGA308 allow for a linear output range as well as over-scale clip, under-scale clip, external fault detection, and internal fault detection. The use of all these features and diagnostic capabilities depends on the final application. The following example shows one way to partition a usable ADC input range to fully use all the diagnostics and features of the PGA308.

Given:

Reference specifications: V_{REF} = 4.096V, ±0.2%, 10ppm/°C

$V_{LIM} = V_{REF}$

Operating temperature range: –40°C to +125°C

V_S = +5V

External fault monitor: Trip high when fault detected

Internal fault monitor: Trip low when fault detected

System scaling relative to a 16-bit ADC with $V_{REF\ ADC}$ = 4.096V

Allow 1% of $V_{REF\ ADC}$ at the upper and lower end of ADC range for ADC headroom (noise floor, ADC gain error, ADC offset error)

Find: Recommended levels to allow for over-/under-scale limits as well as fault detection.

(a) Over-Scale Limit

(b) Under-Scale Limit

(c) Usable Linear PGS308 Output Range

(d) System ADC Trip Points: Over-Scale, Under-Scale, External Fault Detection, Internal Fault Detection

Solution:

1. Analyze the worst-case offset errors on the over-scale and under-scale amplifiers over the operating temperature range.

Table 3-5. Over-/Under-Scale Typical Offset and Drift Values

PARAMETER	TYPICAL VALUE	UNITS
Over-scale amplifier offset, under-scale amplifier offset	±9	mV
Over-scale amplifier offset drift, under-scale amplifier offset drift	±10	µV/°C

Over-Scale and Under-Scale Amplifier Offset Calculation:

Amplifier Offset Temperature Drift:

–40°C to +125°C: 1.65mV = (10µV/°C)[(+125°C – (–40°C)]

Amplifier offset min and max over temperature:

V_{OS} max = 9mV + 1.65mV = 10.65mV

2. Analyze the worst-case change in V_{REF} over the operating temperature range.

V_{REF} Temperature Drift:

–40°C to +125°C: [(10ppm/°C)/(1e6)][+125°C – (–40°C)]V_{REF} = 0.00165 V_{REF}

V_{REF} Min and Max:

V_{REF} min = 4.0878V – (0.00165)(4.096V) = 4.0810V

V_{REF} max = 4.1042V + (0.00165)(4.096V) = 4.1109V

3. Analyze the worst-case Over-Scale and Under-Scale ratio over the operating temperature range.

Ratio Temperature Drift:

Threshold tempco = ±3ppm/°C

–40°C to +125°C: 480ppm = (3ppm/°C)(+125°C – –40°C)

–40°C to +125°C: 0.00048 = (480ppm)/(1e+6)

Over-Scale (OS) Min and Max Ratio:

OS ratio min temperature = (OS ratio min) – (OS ratio min)(0.00048)

OS ratio max temperature = (OS ratio max) + (OS ratio max)(0.00048)

Under-Scale (US) Min and Max Ratio:

US ratio min temperature = (US ratio min) – (US ratio min)(0.00048)

US ratio max temperature = (US ratio max) + (US ratio max)(0.00048)

4. Calculate the over-scale and under-scale min and max clip points over the operating temperature range for each Over-Scale and Under-Scale threshold (refer to Table 3-6).

Over-Scale (OS) Min and Max Trip Points:

OS min = V_{REF} min (OS ratio min temperature) – V_{OS} max

OS max = V_{REF} max (OS ratio max temperature) + V_{OS} max

Under-Scale (US) Min and Max Trip Points:

US min = V_{REF} min (US ratio min temperature) – V_{OS} max

US max = V_{REF} max (US ratio max temperature) + V_{OS} max

Table 3-6. Over-Scale and Under-Scale Min and Max Clip Point Calculations(1)

Over-/ Under-Scale Index	Min Threshold	Typ Threshold	Max Threshold	Min Clip (V)	Typ Clip (V)	Max Clip (V)	Min Clip (% $V_{REF\ ADC}$)	Typ Clip (% $V_{REF\ ADC}$)	Max Clip (% $V_{REF\ ADC}$)
OS0	0.97000	0.98050	0.99000	3.94602	4.01613	4.08239	96.34	98.05	99.67
OS1	0.95880	0.96880	0.97880	3.90033	3.96820	4.03633	95.22	96.88	98.54
OS2	0.95090	0.96090	0.97090	3.86811	3.93585	4.00384	94.44	96.09	97.75
OS3	**0.93920**	**0.94920**	**0.94920**	**3.82039**	**3.88792**	**3.91459**	**93.27**	**94.92**	**95.57**
OS4	0.84160	0.85160	0.86160	3.42227	3.48815	3.55430	83.55	85.16	83.77
OS5	0.76730	0.77730	0.78730	3.11920	3.18382	3.24872	76.15	77.73	79.31
OS6	0.61890	0.62890	0.63890	2.51387	2.57597	2.63836	61.37	62.89	64.41
OS7	0.56030	0.57030	0.58030	2.27484	2.33595	2.39735	55.54	57.03	58.53
US0	0.01353	0.01953	0.02553	0.04454	0.07999	0.11565	1.09	1.95	2.82
US1	0.01743	0.02343	0.02943	0.06045	0.09597	0.13169	1.48	2.34	3.22
US2	0.02525	0.03125	0.03725	0.09235	0.12800	0.16385	2.25	3.13	4.00
US3	0.02916	0.03516	0.04116	0.10829	0.14402	0.17994	2.64	3.52	4.39
US4	0.03306	0.03906	0.04506	0.12420	0.15999	0.19598	3.03	3.91	4.78
US5	**0.04088**	**0.04688**	**0.05288**	**0.15610**	**0.19202**	**0.22814**	**3.81**	**4.69**	**5.57**
US6	0.04478	0.05078	0.05678	0.17201	0.20799	0.24418	4.20	5.08	5.96
US7	0.04870	0.05470	0.06070	0.18800	0.22405	0.26030	4.59	5.47	6.36

(1) V_{OS} max = 0.01065V; Ratio Δ Temp = 0.00048; V_{REF} min = 4.0810V; V_{REF} max = 4.1109V; V_{REF} typ = 4.096V; $V_{REF\ ADC}$ = 4.0960V; V_S = 5V.

5. From the over-scale and under-scale min and max clip point calculations, choose the best selection that will allow for the optimum system ADC range budget (see Figure 3-18). For this example, the PGA308 is scalable for a linear output of 8% to 91% of the system ADC reference. In addition, we can set reasonable trip points for detecting the over-scale limit, under-scale limit, and both internal and external faults.
6. Check that the PGA308 V_{OUT} can support the voltage swings defined in the System ADC range budget. In this example, the lower end is limited by the $V_{OUT\ LOW}$ of the PGA308 and not the ADC Lower Headroom. The upper end has plenty of margin since $V_{REF\ ADC}$ is 4.096V and the PGA308 will be supplied by V_S = 5V.

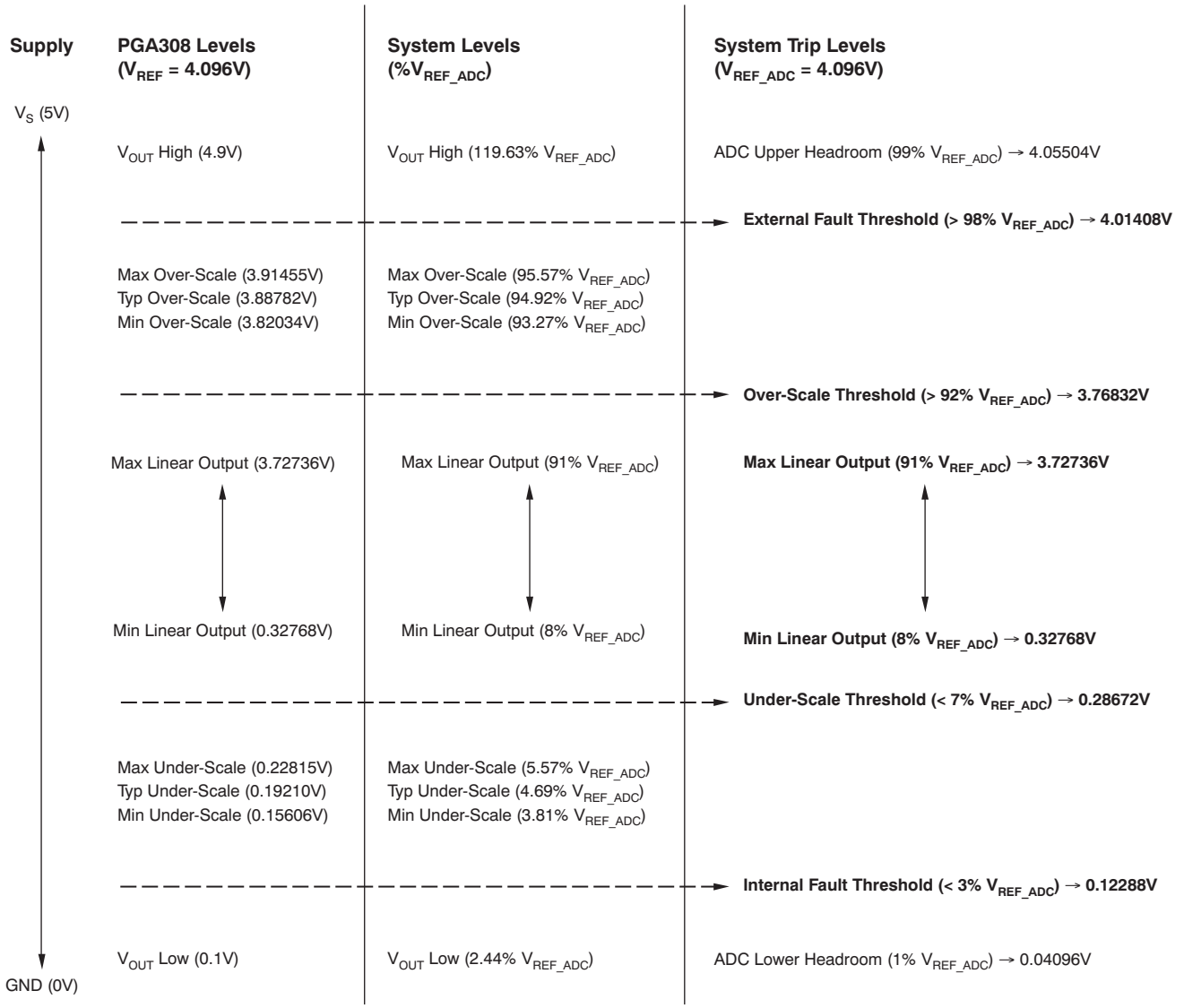


Figure 3-18. System ADC Range Budget: Over-Scale, Under-Scale, Linear Output, Fault Detect

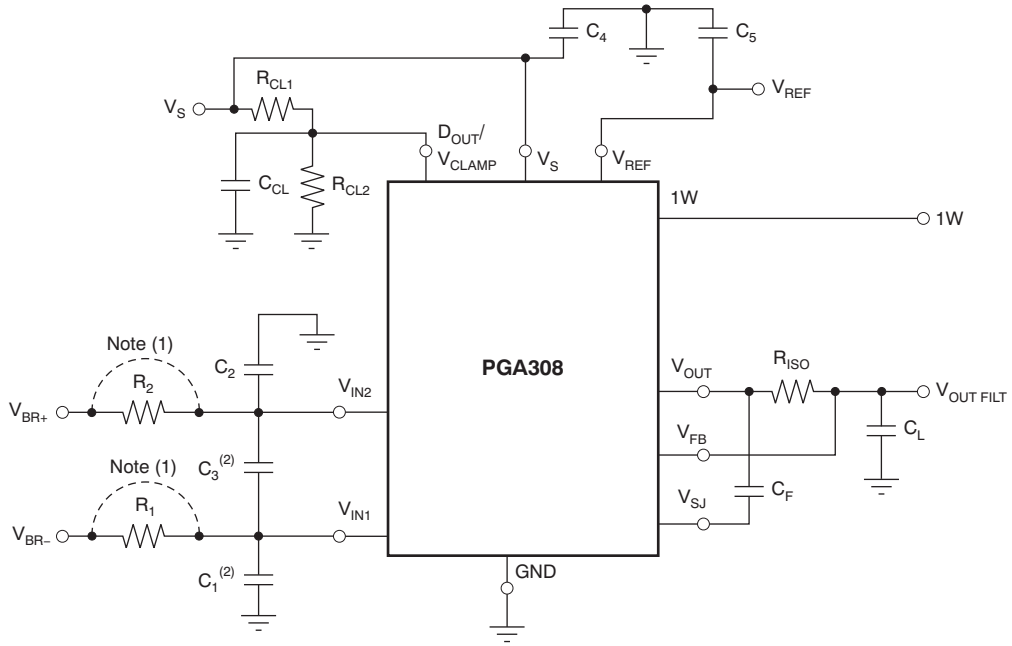
3.9 V_{REF} Pin

The reference voltage input pin, V_{REF}, is always used for the coarse offset adjust reference and for the Zero DAC reference. V_{REF} or V_S may be individually selected for Over/Under-Scale threshold reference and fault monitor comparator reference. Input current drive requirements for V_{REF} are 100µA (typ) with an input voltage range from 1.8V to V_S. Noise on the V_{REF} input reflects directly into the PGA308 internal circuitry; consequently, it is advisable to bypass the V_{REF} pin with at least a 0.1µF ceramic capacitor directly at the PGA308 to the PGA308 local ground connection.

3.10 General AC Considerations

In addition to normal good analog layout and design practices, there are several key items to check when designing with the PGA308.

1. V_{REF}, pin 10: Bypass this pin with a 0.1µF capacitor.
2. V_{SJ}, pin 7: This pin is the negative input to the Output Amplifier; it is high-impedance. Route low-impedance traces (such as V_{OUT}) and noisy traces away from V_{SJ}. Minimize trace lengths to avoid unwanted additional capacitance on V_{SJ}.
3. V_{IN1}, pin 5 and V_{IN2}, pin 6: For source resistances greater than or equal to 10kΩ, add a 1nF to 2nF capacitor between V_{IN1} and V_{IN2} to minimize noise coupling.
4. V_{IN1}, pin 5 and V_{IN2}, pin 6: RFI filtering is always a concern for instrumentation amplifier applications. RFI signals injected into instrumentation amplifiers become rectified and appear on the output as a dc drift or offset; high-gain circuits amplify this effect. Figure 3-19 depicts input filtering for the PGA308. Depending on the distance of the bridge sensor from the PGA308 and the sensor module shielding, R_1 and R_2 may be required. C_1 should be equal to C_2, and C_3 should be ten times larger than C1 to attenuate any common-mode signals that become differential as a result of the mismatch in C_1 and C_2. All input filter components should be located directly at the PGA308 inputs to avoid long trace lengths from becoming receiving RFI antennas.
5. Printed circuit board (PCB) layout: Proper routing of sensitive signals, component placement, and local bypass capacitors are all important to optimize PGA308 performance. Figure 3-19 is a schematic of a typical PGA308 application. Figure 3-20 is a recommended two-layer PCB layout for this application.



(1) Depends on bridge sensor resistance and distance from the bridge sensor to thePGA308.

(2) $C_1 = C_2$, $C_3 = 10 \times C_1$.

Figure 3-19. PGA308 Application Schematic: AC Considerations

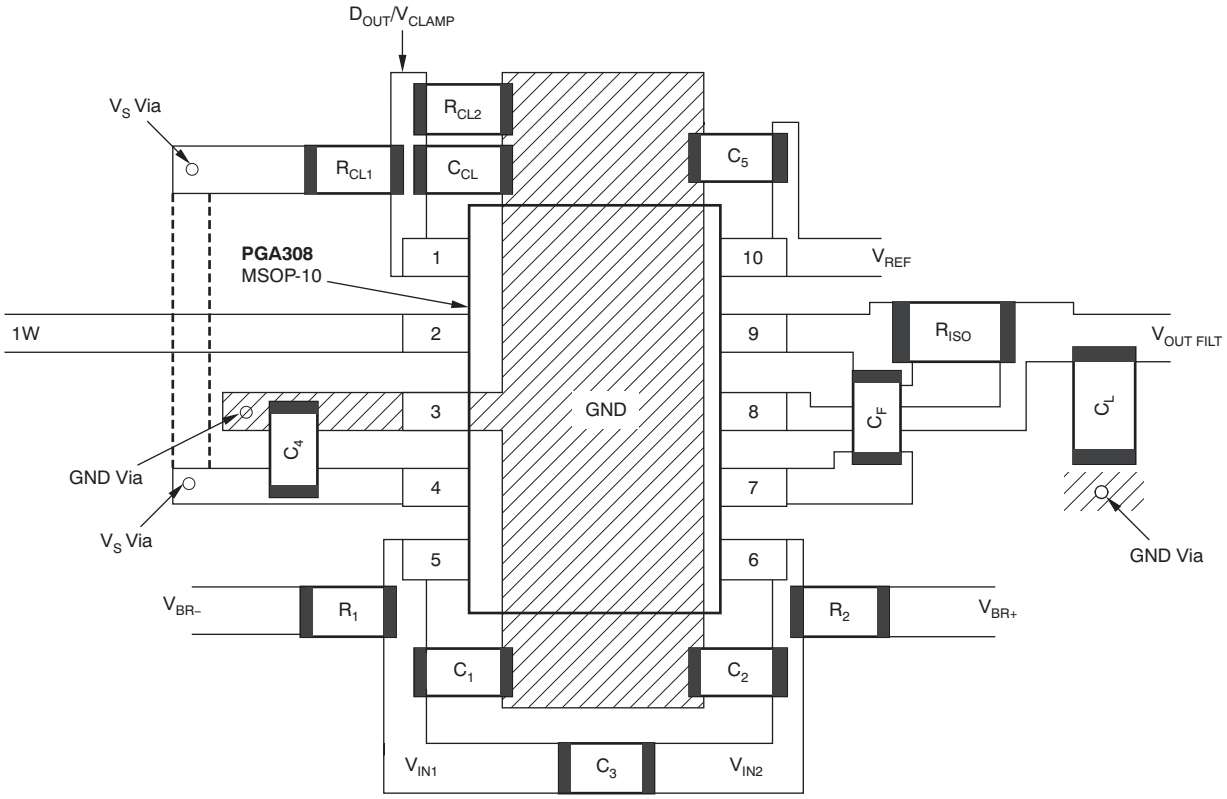


Figure 3-20. PGA308 Application PCB Layout: AC Considerations

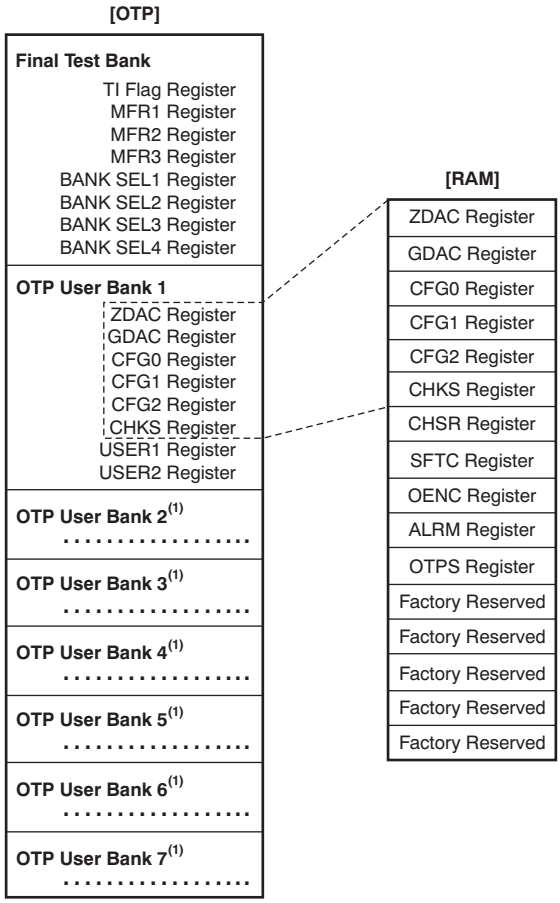
Detailed Digital Description

This chapter provides a detailed description of the digital circuitry for the PGA308.

Topic **Page**

4.1 Memory Structure

Figure 4-1 shows the internal memory structure of the PGA308. The memory is divided into two separate regions: one time programmable (OTP) memory and random access memory (RAM). The OTP memory section contains one final test bank and seven OTP user banks. Each of these banks consists of eight 16-bit registers. For specific register bit definitions, see Chapter 7, *Detailed Register Description*.



(1) Contents same as OTP User Bank 1.

Figure 4-1. PGA308 Memory Structure

4.2 OTP Memory Section

The Final Test Bank contains four factory registers used during final test to trim the PGA308 for optimum performance:

- TI FLAG Register
- MFR1 Register
- MFR2 Register
- MFR3 Register

The remaining four registers are used to program a pointer to the desired OTP User Bank *X* (where X = 1 to 7) to be loaded on power-up for Standalone Mode:

- BANK SEL1 Register
- BANK SEL2 Register
- BANK SEL3 Register
- BANK SEL4 Register

OTP User Bank *X* selection may be set four times by programming the BANK SEL*x* registers in order (where x = 1, 2, 3, or 4). The default power-on reset (POR) OTP User Bank *X* (1 of 7) selected will be the one addressed by the pointer stored in the last programmed BANK SEL*x* (1 of 4) Register. Therefore, when programmed, BANK SEL4 always has priority over lower-numbered bank select registers.

The PGA308 can be programmed in OTP seven times and the POR OTP User Bank selection can be changed four times. This programmability allows for situations where a calibration may be conducted on a given module before discovery that the calibration system was not configured correctly or was out of calibration. This four-time re-programmability for OTP user bank selection allows for recalibration rather than discarding the final sensor module.

The seven OTP user banks (OTP User Bank 1 through OTP User Bank 7) each contain the same eight register sets. Six of these registers (ZDAC Register, GDAC Register, CFG0 Register, CFG1 Register, CFG2 Register, CHKS Register) map directly into the RAM section of the PGA308 and are used for configuration of the PGA308. On POR, the OTP user bank that is pointed to by the highest-number programmed BANK SEL*x* Register will have its contents loaded directly into RAM. The remaining two registers (USER1 Register, USER2 Register) are available for user data such as model number, serial number, lot code, or other manufacturing/identification information. The seven possible user OTP banks allow an end product (using a microcontroller as the interface between the end user and the PGA308) to contain up to seven factory preprogrammed configurations and allow total user flexibility for any other configuration through software communication over the One-Wire interface (1W pin).

4.3 RAM Memory Section

The RAM section contains all of the real-time registers for configuration of the PGA308. The first six of these 14 registers are used for the configuration of the PGA308:

- ZDAC Register
- GDAC Register
- CFG0 Register
- CFG1 Register
- CFG2 Register
- CHKS Register

These six registers map directly from the OTP User Bank section of the PGA308, or can be entered real-time through the One-Wire interface.

The remaining eight registers contain both factory-only usage/information, as well as advanced features of the PGA308 (see Chapter 5, *Operating Modes*, and Chapter 7, *Detailed Register Description*):

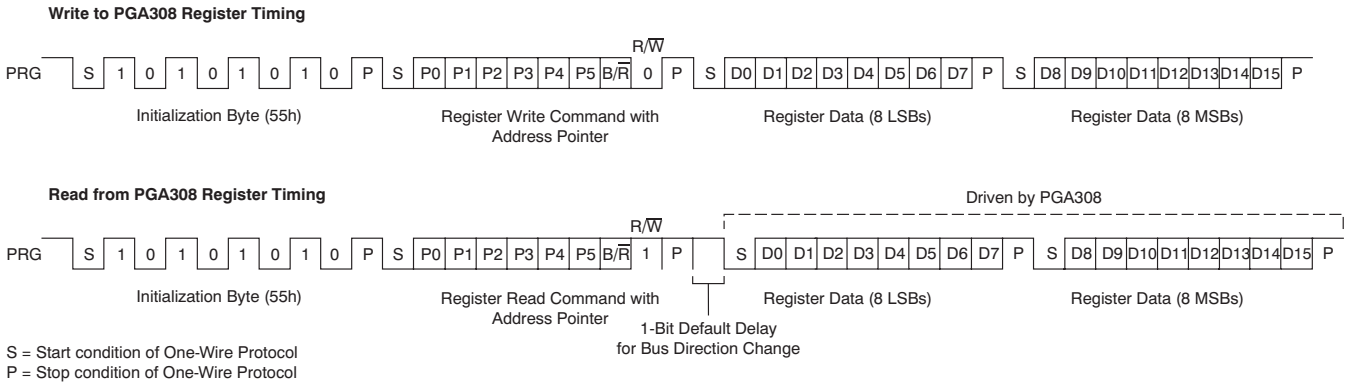
- CHSR Register
- SFTC Register
- OENC Register
- ALRM Register
- OTPS Register
- TST Register
- BDCL Register
- TRST Register

4.4 Digital Interface

The PGA308 digital interface pin, 1W, uses a One-Wire, UART-compatible interface, with bit rates from 4.8kbits/s (4800 baud) to114kbits/s (114k baud). It is possible to connect this single-wire communication pin to the V_{OUT} pin in true three-wire sensor modules (V_S, GND, and Sensor Out) and continue to allow for calibration and configuration programming (see Chapter 5, *Operating Modes*).

Figure 4-2 illustrates the One-Wire interface protocol used on the 1W pin to communicate with the PGA308. Each transaction consists of several bytes of data transfer. Each byte consists of 10-bit periods. The first bit is the start bit and is always '0'. The 1W pin should always be high when no communication is in progress. The '1' to '0' (high to low) transition signals the start of a byte transfer with all timing information for the current byte referenced to this transition. The second through ninth bits are the eight data bits for the command byte (see Figure 4-3), and are transferred LSB first. The tenth bit is the stop bit and is always '1'.

The recommended circuit implementation is to use a pull-up resistor and/or current source with an open drain (or open collector) output connected to the 1W pin, which is also an open drain output. The single wire may be driven high by the external controller during transmission from the external controller, but some form of pull-up is required to allow the signal to go high during reception because the PGA308 1W pin can only pull the output low (open-drain output). See Figure 4-4 for the typical interface between the PGA308 1W pin and an external controller used to communicate with the PGA308.



NOTE: Unless otherwise indicated, all transactions are driven by the external controller.

Figure 4-2. One-Wire Protocol Timing Diagram

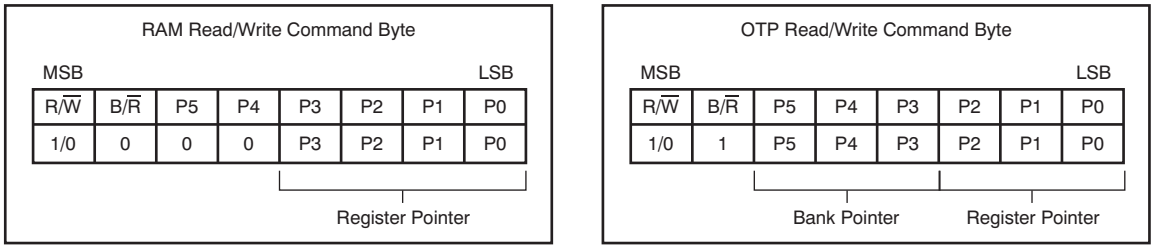


Figure 4-3. PGA308 Command Byte

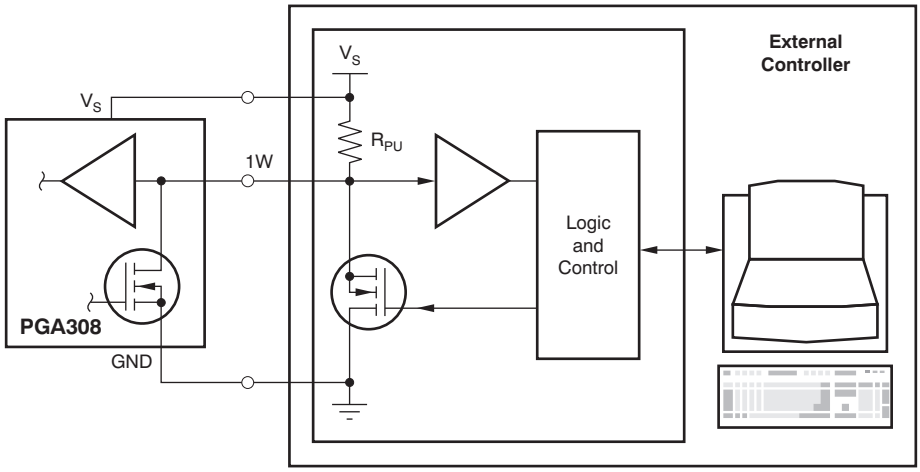


Figure 4-4. Typical PGA308 1W Pin to External Controller Connection

All communication transactions start with an initialization byte transmitted by the external controller. This byte (55h) senses the baud rate used for the communication transaction. The baud rate is sensed during the initialization byte of every transaction and is used for the entire transaction. Each transaction may use a different baud rate if desired. Baud rates of 4.8k bits/second to 114k bits/second are supported.

The second byte is the command byte (see Figure 4-3). The MSB of the command byte is the R/W bit with a '0' indicating a write command and a '1' indicating a read command. The next bit is the B/R bit, with logic 1 set for an OTP Bank read or write, and logic zero for a RAM read or write. With B/R = '1' (OTP Bank access), three bits are used as the Bank Pointer (P5, P4, P3) and three bits are used as the Register Pointer (P2, P1, P0), within the respective OTP Bank addressed by the Bank Pointer. With B/R = '0' (RAM access), four bits are used as the RAM Register Pointer (P3, P2, P1, P0).

Additional data transfer occurs after the command byte is sent. Two 8-bit bytes are always sent with the direction of data transfer, depending on the command byte. For a read sequence, the PGA308 waits for a 1-bit delay after the completion of the command byte before beginning transmission. This delay period allows time for the external controller to ensure that the PGA308 will be able to control the One-Wire interface. The first byte transmitted will be the least significant byte of the register and the second byte will be the most significant byte of the register. Under software control by the OW DLY bit (SFTC Register [D7]), the delay from transmit to receive can be selected between one bit (logic 0 default) or eight bits (logic 1). This option can be useful in systems where a microcontroller is directly connected to the PGA308 and longer delay times are required as a result of system architecture.

4.5 One-Wire Interface Timeout

A timeout mechanism is implemented to allow for resynchronization of the One-Wire interface if the synchronization between the controller and the PGA308 be lost for any reason. The timeout period is set to approximately 28ms (typical). If the timeout period expires between the initialization byte and the command byte, between the command byte and any data byte, or between any data bytes, the PGA308 will reset the One-Wire interface circuitry such that it will expect an initialization byte. Every time that a byte is transmitted on the single-wire interface, this timeout period restarts.

4.6 One-Wire Interface Timing Considerations

Figure 4-5 illustrates the key timing and jitter considerations for the One-Wire interface and Table 4-1 contains the specifications for ensured, reliable operation. During a transaction, the baud rate must remain within ±1% of its initialization byte value; however, the baud rate can change from transaction to transaction. There is an allowed delay between each byte transfer of less than 28ms, which is the bus inactivity timeout check for the PGA308 One-Wire interface.

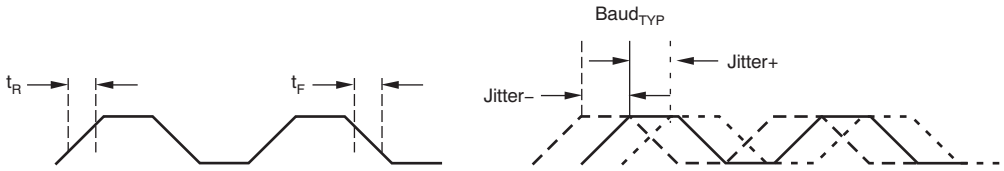


Figure 4-5. One-Wire Timing Diagram

Table 4-1. One-Wire Timing Diagram Definitions

Parameter	Min	Typ	Max	Unit
Baud	4.8k		114k	bits/s
Rise Time, t_R			0.5	%Baud
Fall Time, t_F			0.5	%Baud
Jitter(1)			±1	%Baud

(1) Transmit jitter from controller to PGA308. Standard UART interfaces accepts data sent from the PGA308 during One-Wire transactions.

Operating Modes

This chapter explains the PGA308 operating modes.

Topic **Page**

5.1 Overview

There are two primary ways to configure the PGA308: through RAM or OTP. The PGA308 configuration registers are located in RAM. These registers can be written to directly and retain the respective values until power to the device is cycled, at which time they default to the respective POR values. When calibrating and configuring a sensor module (that is, the PGA308 + sensor), direct writes to RAM can be used until the final values are determined, which are then written into an OTP User Bank.

The second way to configure the PGA308 is to load a valid OTP User Bank *X* (1 to 7) into RAM. This OTP-to-RAM load can occur automatically on device power-up (see Section 5.5, *Standalone Mode*), or under One-Wire software control, depending on the configuration data stored in the OTP User Bank *X*.

5.2 Common Applications

There are two common types of applications that can be built using the PGA308. The difference between these applications is how serial interface communications are conducted to configure and calibrate the PGA308.

Figure 5-1 shows a three-terminal module application, where a bridge sensor and the PGA308 are built together with connections of +5V, Sensor Out, and GND. The One-Wire interface pin, 1W, is connected to Sensor Out in this application; therefore, One-Wire programming the PGA308 + Sensor from the outside of this module will use special PGA308 programming features that allow for a single pin to be used for both V_{OUT} and 1W.

Figure 5-2 is a four-terminal module implementation with a bridge sensor plus the PGA308 and connections of +5V, 1W, Sensor Out, and GND. In this implementation, the One-Wire interface pin (1W) is available, thereby allowing the PGA308 to be easily programmed at any time.

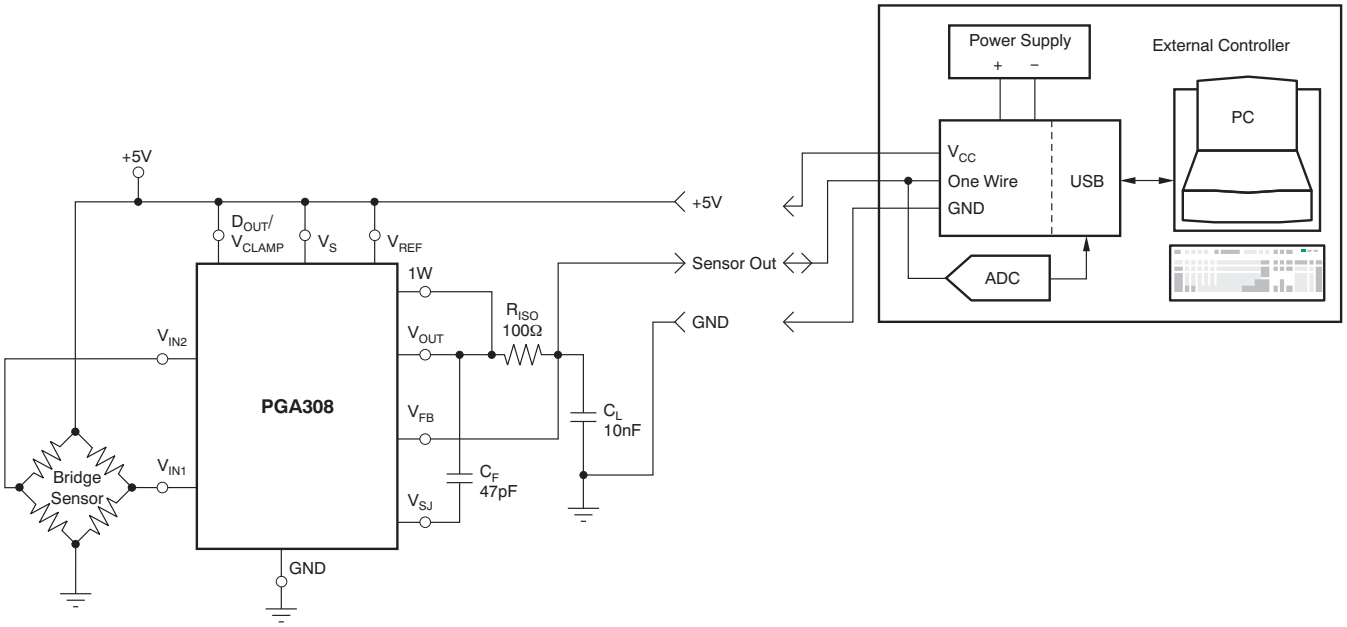


Figure 5-1. Three-Terminal PGA308 Module

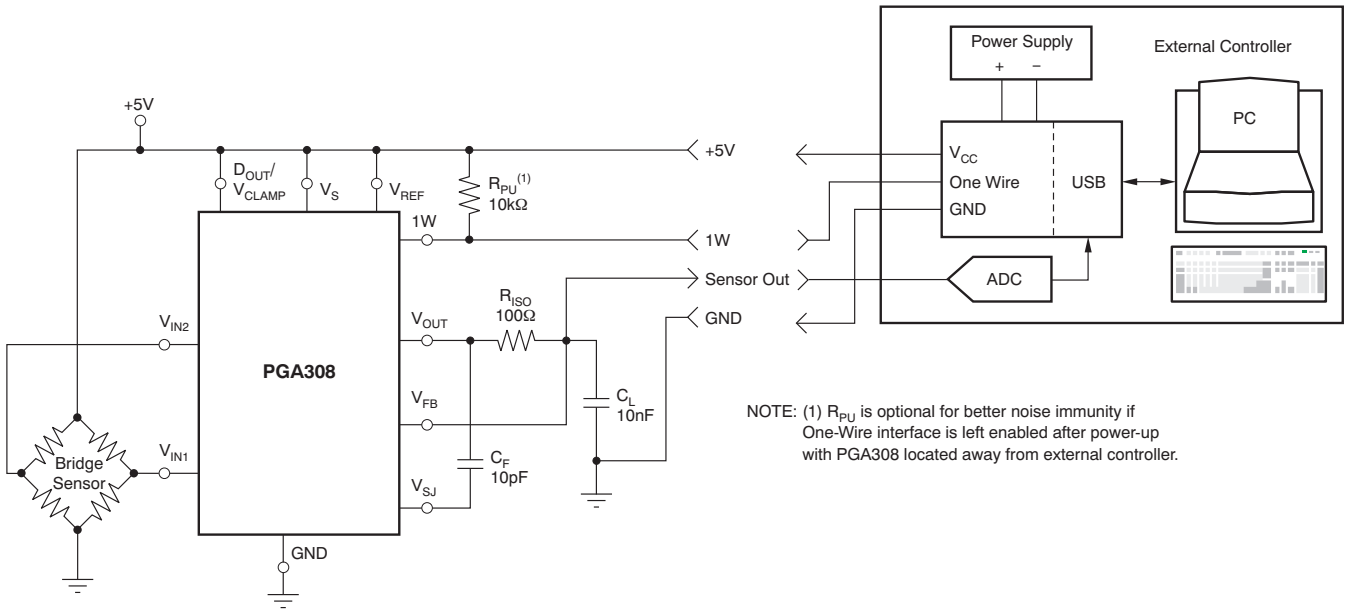


Figure 5-2. Four-Terminal PGA308 Module

In either one of these applications, it is essential that the OWD bit (CFG2 Register [D15]) be set to '1' to disable the 1W interface after final programming is complete and before the final sensor module is sent out to the end application. In three-terminal module application (refer to Figure 5-1), the 1W pin is tied to V_{OUT}, which moves in and out of the threshold region of the 1W input circuitry. There may also be periodic noise, such as an active motor or switching power supply; the 1W circuitry may interpret this noise as valid communications and put the PGA308 into an unpredictable state. In a four-terminal module, the 1W pin is connected directly to the external environment and is even more susceptible to noise coupled from periodic external sources.

Even if the OWD bit is set to '1' (to disable the 1W interface), a 28ms window remains open on device power-up. During this brief time, periodic noise can be coupled into the 1W pin and interpreted as coherent communication. The three-terminal module, on the other hand, is inherently protected from real-world noise, over-voltage, and miswired conditions. The four-terminal module requires a more detailed discussion and several considerations when putting the 1W pin into direct contact with the external environment.

5.2.1 Four-Terminal Module: Detailed Discussion

See Figure 5-5 for an illustration of the details of the 1W circuitry within the PGA308. Additional external protection components and electromagnetic interferences/radio frequency interference (EMI/RFI) filtering are included in this discussion. Considerations for programming the PGA308 four-terminal sensor module are presented with reference to Figure 5-5.

The PGA308 contains electrostatic discharge (ESD) cells, D2 and D1/SCR1, on the 1W pin to prevent ESD damage when the device is being handled before installation on a printed circuit board. These same ESD cells may not be adequate when the PGA308 is installed in a complete circuit with regards to electrical overstress. The ESD diodes D1 and D2 can handle up to 10mA continuous load. However, SCR1 will trigger with a 14V level and then drop to 3V at 80mA of sustaining current, as Figure 5-3 shows. If the current is not limited, the voltage will increase again; this increase, combined with higher currents, may cause permanent damage to the ESD cells and make the 1W circuitry unusable.

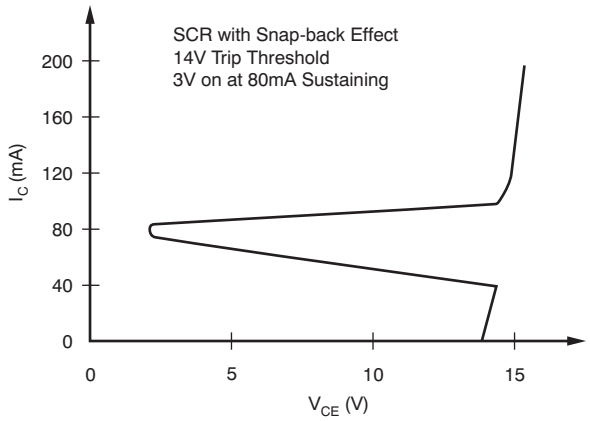


Figure 5-3. SCR ESD Cell

If miswiring is or external electrical overstresses are anticipated, the 1W pin must be protected by using external devices. SD1 and SD2 are signal Schottky diodes that steer current away from the internal ESD cells on the 1W pin during electrical overstress events. R7 will limit the current through SD1 and SD2. Z1 is a zener diode to clamp the energy passed through SD1. The selection of R7 can impact the valid logic levels at 1W_PGA308 and 1W_Programmer. SW2 and R6 represent the MOSFET switch and on-resistance used on the PGA308EVM or customer programmer that configures and calibrates the PGA308 over the 1W interface. For the PGA308, logic high is 2V or greater; logic low is 0.8V or less. Logic high is not a concern because there are pull-up resistors on the PGA308 module and on the programmer. The worst-case condition is shown in Figure 5-5; this figure illustrates the condition at approximately 610mV, which is less than the specified 0.8V (max) logic low. This configuration will be adequate for up to ±50V of miswiring on the 1W pin, based on current flow and the power dissipation of the components shown up to a temperature of +75°C.

Each individual application should be analyzed for electrical overstress and proper programming logic levels on the 1W pin.

Refer to Figure 5-6 for an illustration of common EMI/RFI filtering and the 1W pin configuration. Most EMI/RFI filter schemes typically involve connecting the chassis ground to the signal ground via capacitors in the range of 1nF to 10nF. These capacitors are connected on every pin into and out of the module. In FigDD, we connect the signal ground to the chassis ground with capacitor C2 (1nF). V_{CC} is connected to the chassis ground through capacitor C4 (100nF) and capacitor C2 (1nF). We also add capacitor C1 (10nF) from the 1W pin at the module output and tie it directly to V_{CC}. This configuration is optimal for rejecting any switching disturbances between the chassis ground and the signal ground.

EMI/RFI is often seen as disturbance referenced to the chassis ground, as shown in Figure 5-6. A common source impedance of 50Ω (through R11) is assumed. The disturbance is injected into the 1W pin of the module, and will then flow through capacitors C3 (10nF), C4 (100nF), and C2 (1nF) as it returns to chassis ground. A severe disturbance of ±5V at 100kHz will only degrade the logic high voltage on the 1W pin from 5V to 4.27V, as shown in Figure 5-4. The minimum logic high us 2V, and thus there will be no 1W miscommunication caused by this severe disturbance between chassis ground and signal ground.

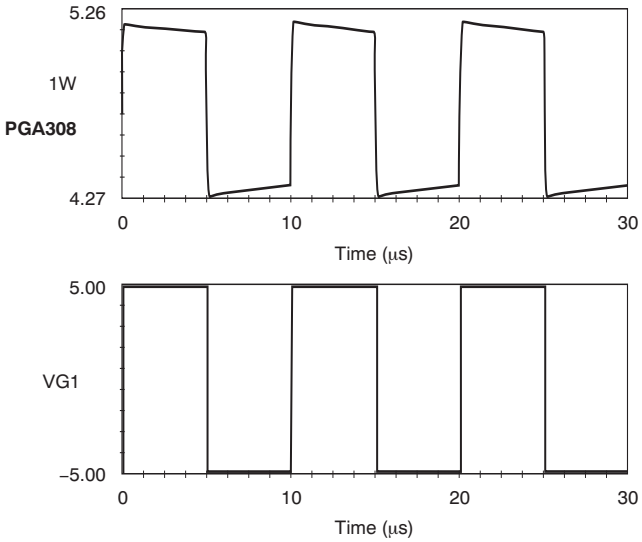


Figure 5-4. Severe EMI/RFI Disturbance

As a final note, consider Figure 5-5 once more, and observe that in order to program a 1W pin on a module with large capacitance (for example, with C1 = 10nF) on the 1W pin, the customer programmer must use a 1W speed-up circuit, which detects a rising edge on the 1W signal. Based on this rising edge, a switch connects the 1W line to +5V through a 200Ω resistor for 5µs in order to quickly charge capacitor C1 (10nF) and obtain a reasonable rising edge in logic '0' to logic '1' transitions. The PGA308EVM has this 1W speed-up circuit already installed in the PC Programmer Interface Board.

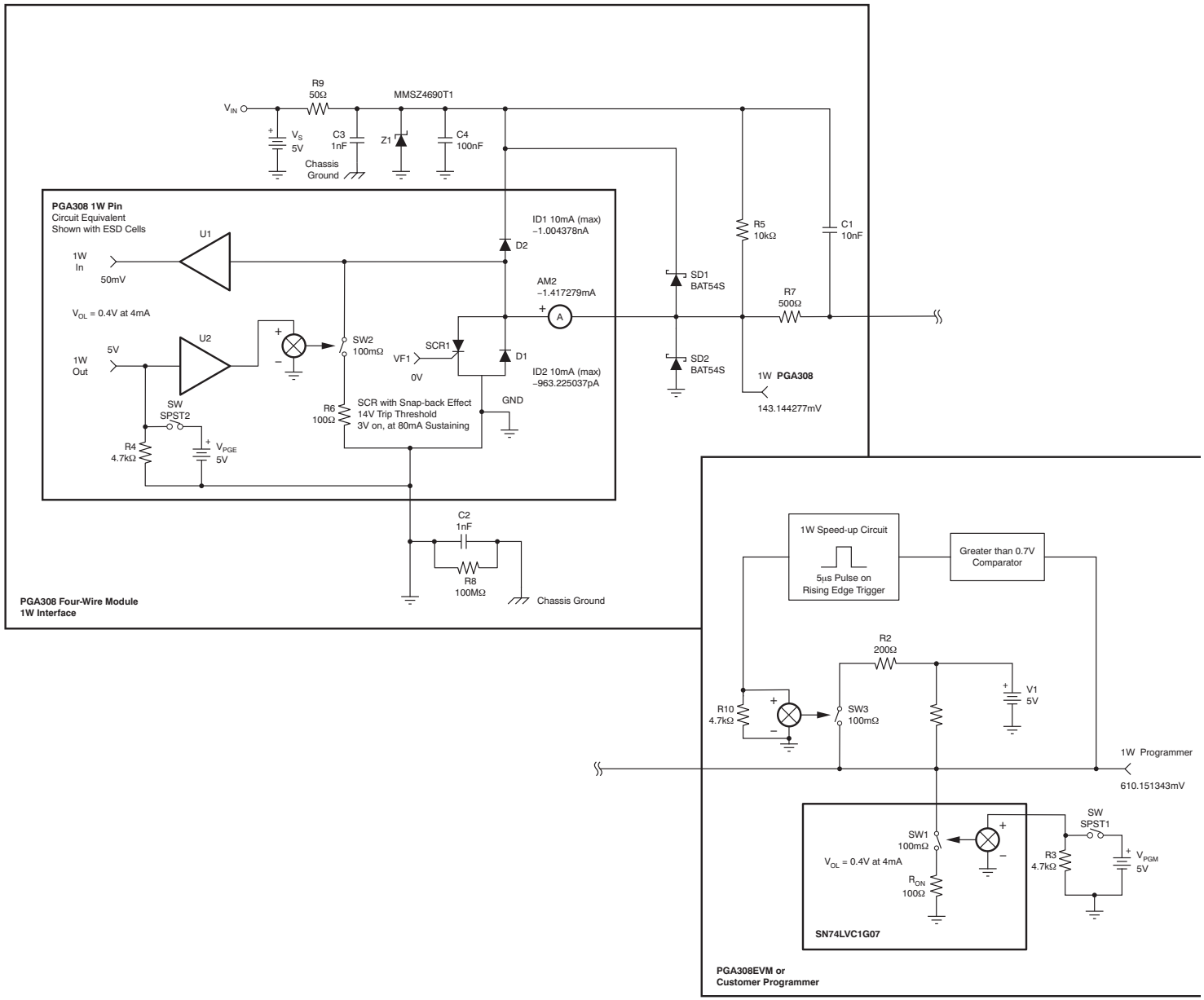


Figure 5-5. Pin 1W Circuit Protection Logic Levels

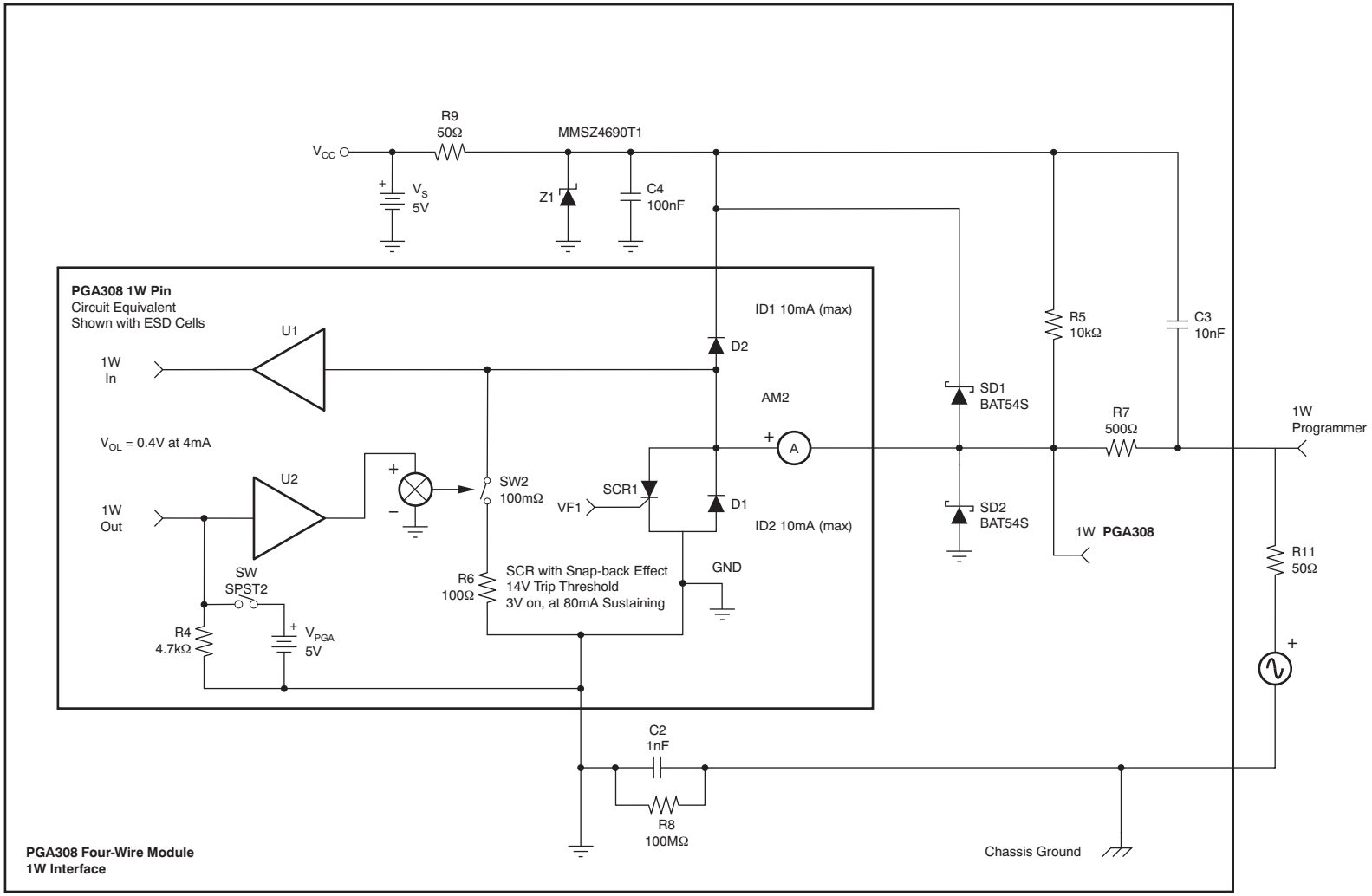


Figure 5-6. Pin 1W Circuit EMI/RFI Filtering

5.3 One-Wire Write Mode, One-Wire Read Mode

Figure 5-7 shows the algorithm used for a One-Wire write to the PGA308. If the external controller stops communication with the PGA308 for 28ms between any transmitted byte, the PGA308 will reset the One-Wire interface and wait for a new initialization byte. See Figure 5-8 for the PGA308 read algorithm. Halfway through the read transaction, the PGA308 becomes the transmitter and the external controller becomes the receiver. Therefore, the One-Wire timeout is only used when the external controller sends data. The One-Wire timeout monitors when valid data stop being received by the PGA308. When the PGA308 transmits data, it is in control of data going out; therefore, proper communication is known. Refer to Figure 4-2, *One-Wire Protocol Timing Diagram*, for further details.

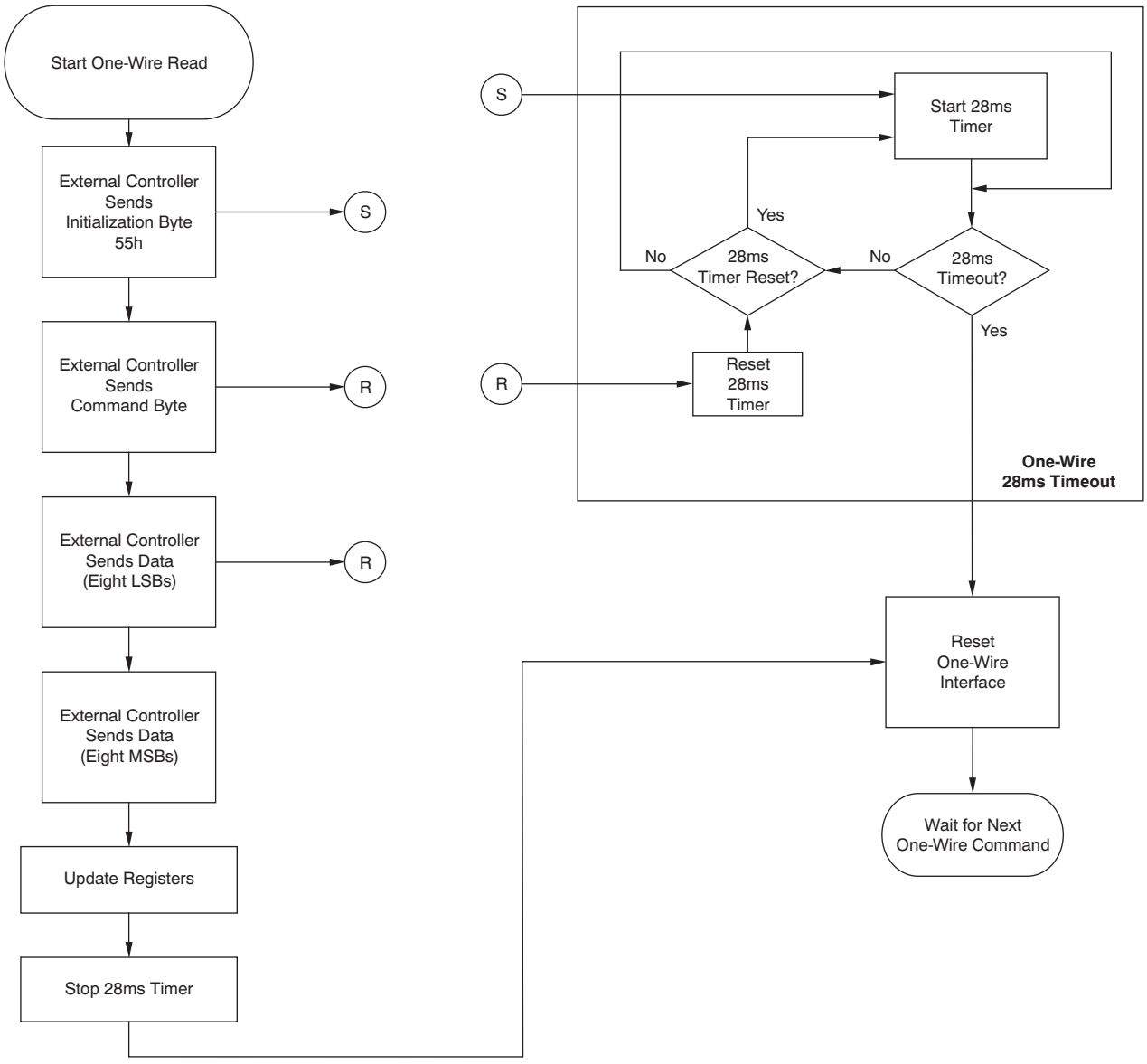


Figure 5-7. One-Wire Write Mode

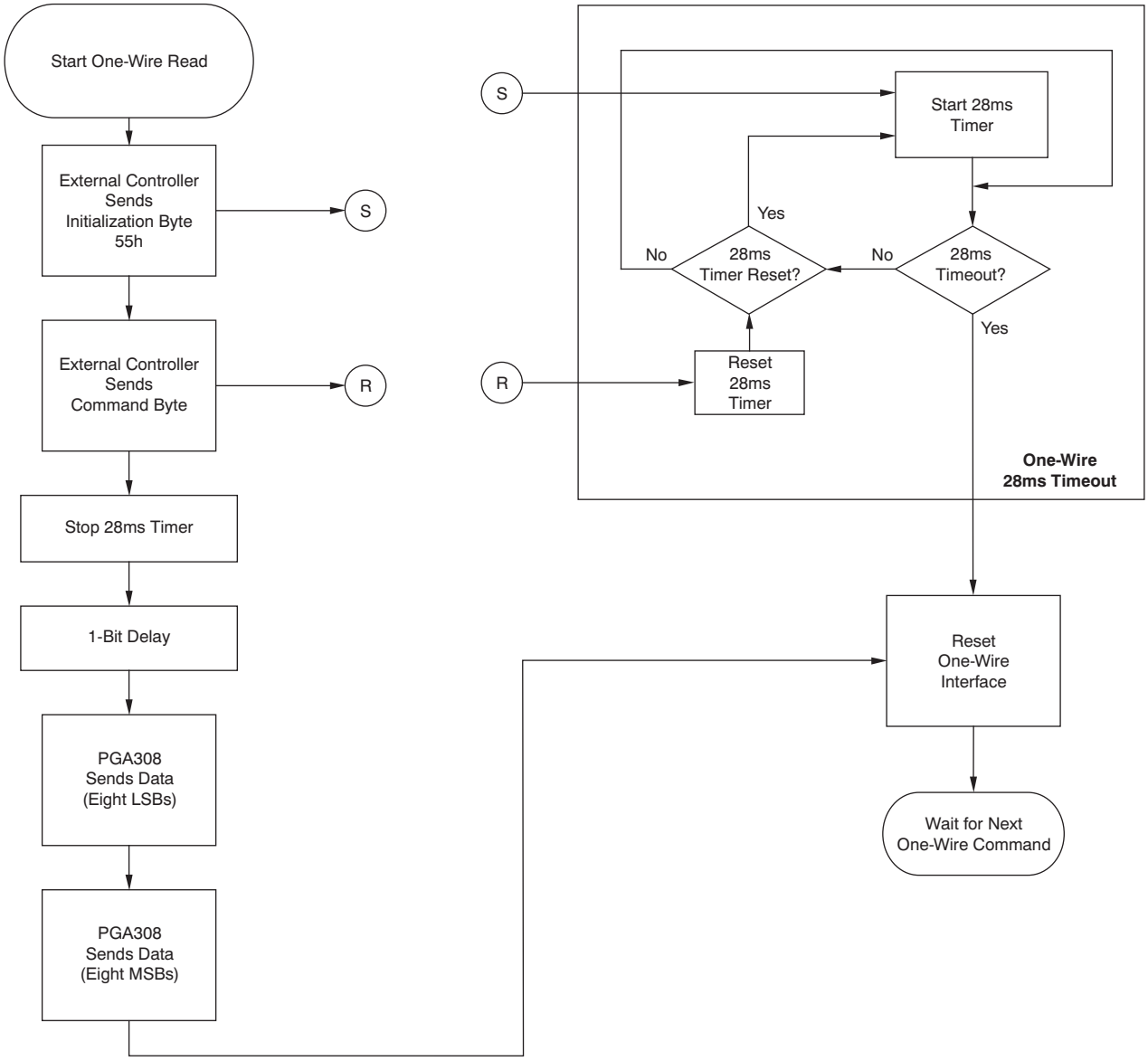


Figure 5-8. One-Wire Read Mode

5.4 OTP Program Mode

Figure 5-9 outlines the OTP program sequence for the PGA308. Note the requirement for $V_S \geq +4.5V$ to ensure reliable programming of the OTP. When programming the OTP memory, polling the OTP BSY bit, or inserting a 3ms delay between the OTP One-Wire Writes ensures that the PGA308 has finished programming the previous OTP Write data.

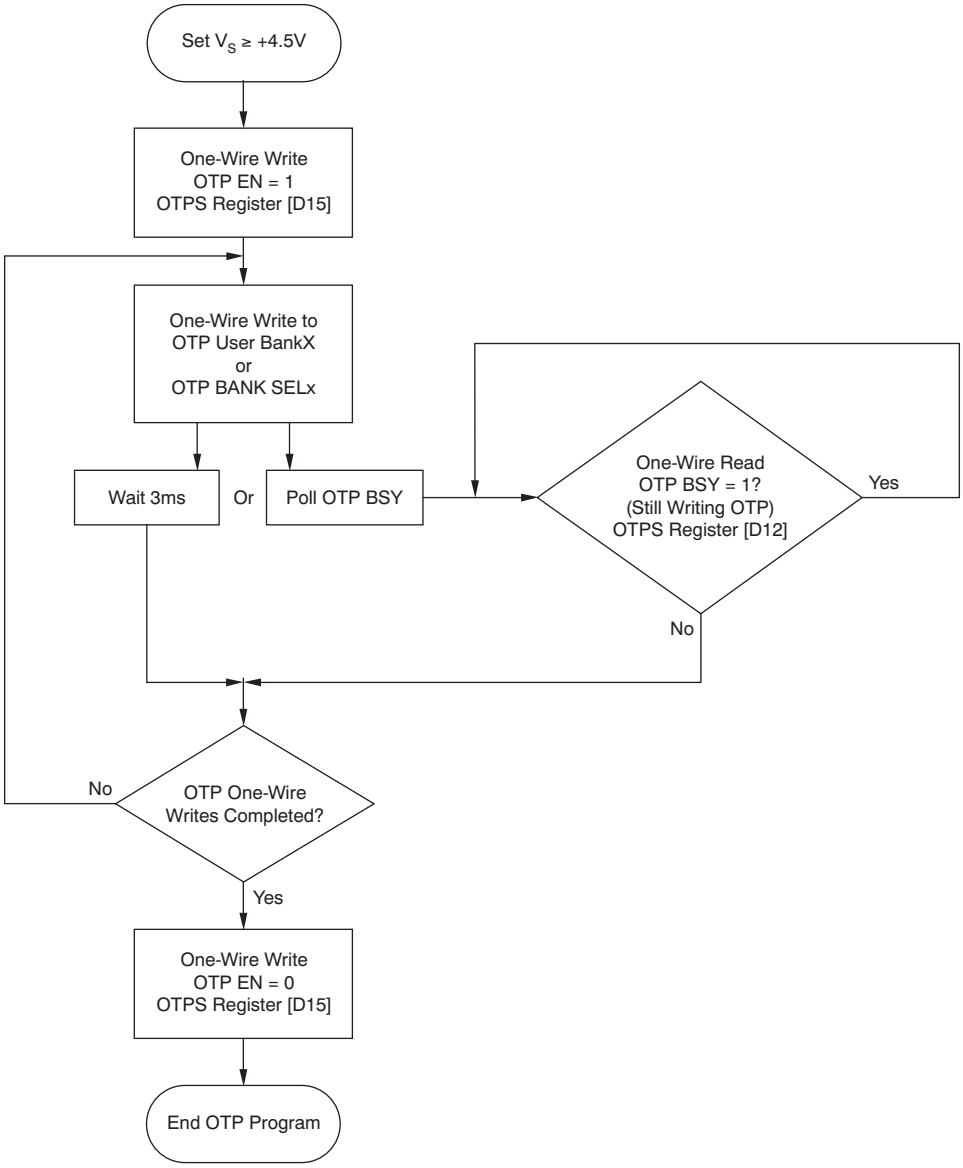


Figure 5-9. OTP Program Mode

5.5 Standalone Mode

Standalone Mode operation of the PGA308 can be used when two conditions have been met:

1. The PGA308 OTP has been programmed; and
2. On device power-up, the application will operate from a selected OTP User Bank *X*.

The specific OTP bank to be used is determined by the pointer stored in the BANK SEL*x* register in OTP. The OTP BANK SEL*x* register contents to be used at POR are the contents of the highest numbered OTP BANK SEL*x* register that is programmed.

There are four OTP BANK SEL*x* registers. The selection of the appropriate OTP BANK SEL*x* occurs according to the following protocol:

Assume that the user has several OTP User Banks programmed in to the PGA308. The first written OTP BANK SEL*x* was OTP BANK SEL4 and the last written OTP BANK SEL*x* register was OTP BANK SEL1. At POR, the PGA308 loads into RAM the contents of the OTP User Bank *X* that is pointed to by the BANK SEL4 register, because it is the highest numbered OTP BANK SELx register programmed.

The OTP BANK SEL*x* registers are OTP; therefore, they may be written to only once. The highest-numbered register that has been written to becomes the POR default register that points to the OTP User Bank *X* that is loaded into the PGA308 RAM.

If an OTP User Bank *X* is loaded with a valid checksum, there are two independent parallel process paths to determine the configuration of V_{OUT} and the One-Wire interface. Figure 5-10 details the Standalone Mode algorithm for how the PGA308 state machine operates in Standalone Mode.

In most applications, it is recommended to disable the One-Wire interface when operating in Standalone Mode. This configuration prevents the One-Wire interface from being subjected to unwanted noise transitions that could be misinterpreted as valid logic levels and, with the combination of periodic and random noise, as valid One-Wire communications. This problem is especially true in three-terminal modules where the 1W pin is connected directly to V_{OUT}. A valid analog voltage on V_{OUT} could be at 1.4V (between the logic high and logic low input levels for 1W). Any system noise spikes on V_{OUT} could then cause erroneous logic changes on the 1W pin.

There are two recommended configurations, depending on the application, to disable the One-Wire interface and enable V_{OUT} for a three-terminal module. Configuration 1 (shown in Table 5-1) allows access to the One-Wire interface for 25ms after power is valid because the One-Wire interface is enabled and V_{OUT} is disabled (see Section 2.11, *One-Wire Operation with 1W Connected to V_{OUT}* , for programming details). This configuration allows reprogramming of a three-terminal module, if needed.

For three-terminal modules that are programmed for the last time with the desired final values, Configuration 2 uses the NOW bit to enable V_{OUT} almost instantly (60µs typical) and uses the OWD and OWD OFF bits to disable the One-Wire interface almost instantly (60µs typical). The only way to reprogram a three-terminal module that uses Configuration 2 is shown in Figure 5-11. Access to the V_{REF} pin and the ability to ground the V_{REF} pin is required. Once the module is reprogrammed, cycle power with V_{REF} at the normal value for normal PGA308 operation.

Table 5-1. Recommended Standalone Mode Configurations for Three-Terminal Modules

Configuration 1					
		V_{OUT}			One-Wire
DIS OUT	0	Enable 25ms after power valid	OWD	1	Disabled 25ms after power valid
NOW	0		OWD OFF	0	
Configuration 2					
		V_{OUT}			One-Wire
DIS OUT	0	Enable 60µs after power valid	OWD	1	Disabled 60µs after power valid
NOW	1		OWD OFF	1	

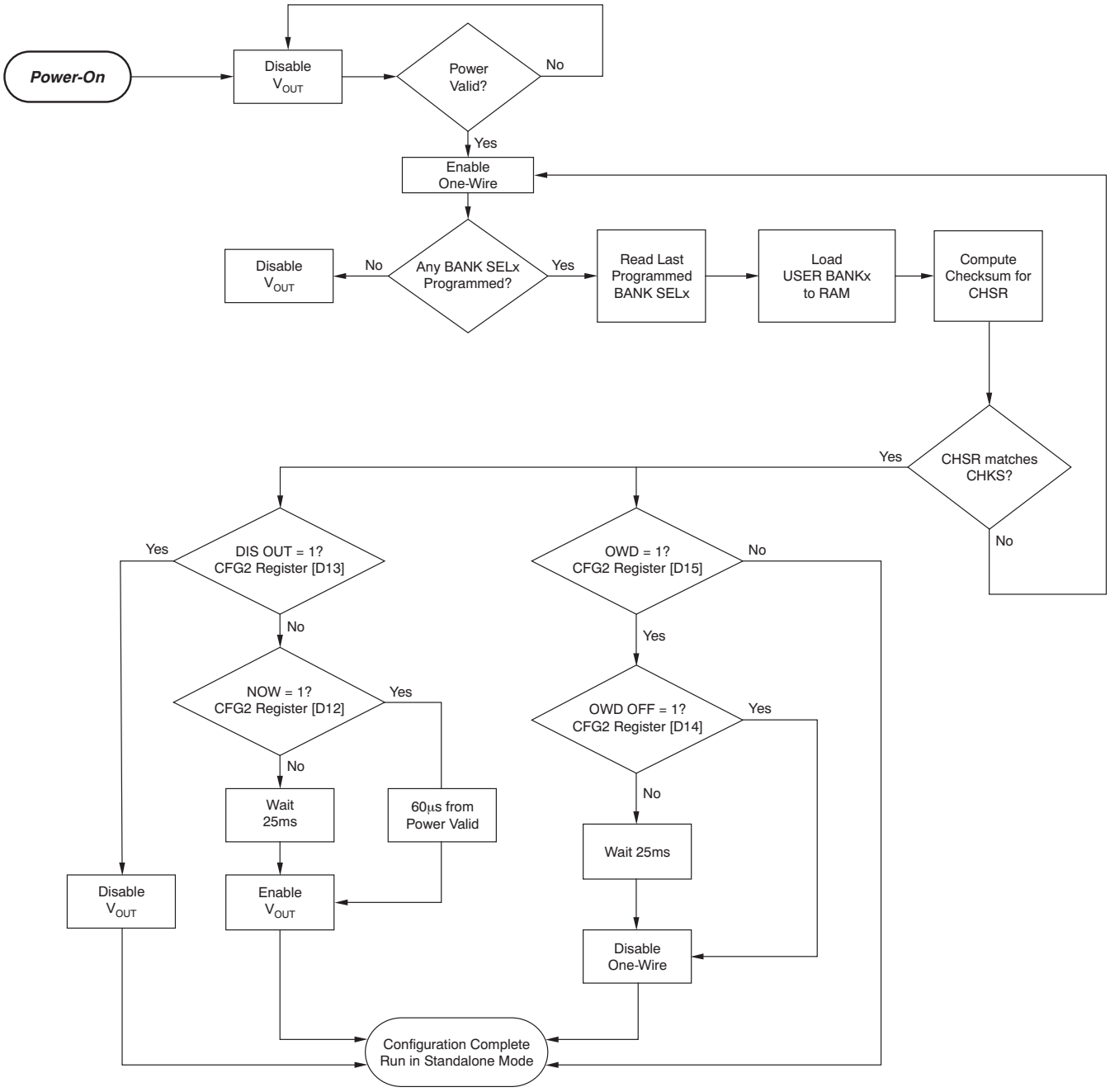


Figure 5-10. Standalone Mode Operation

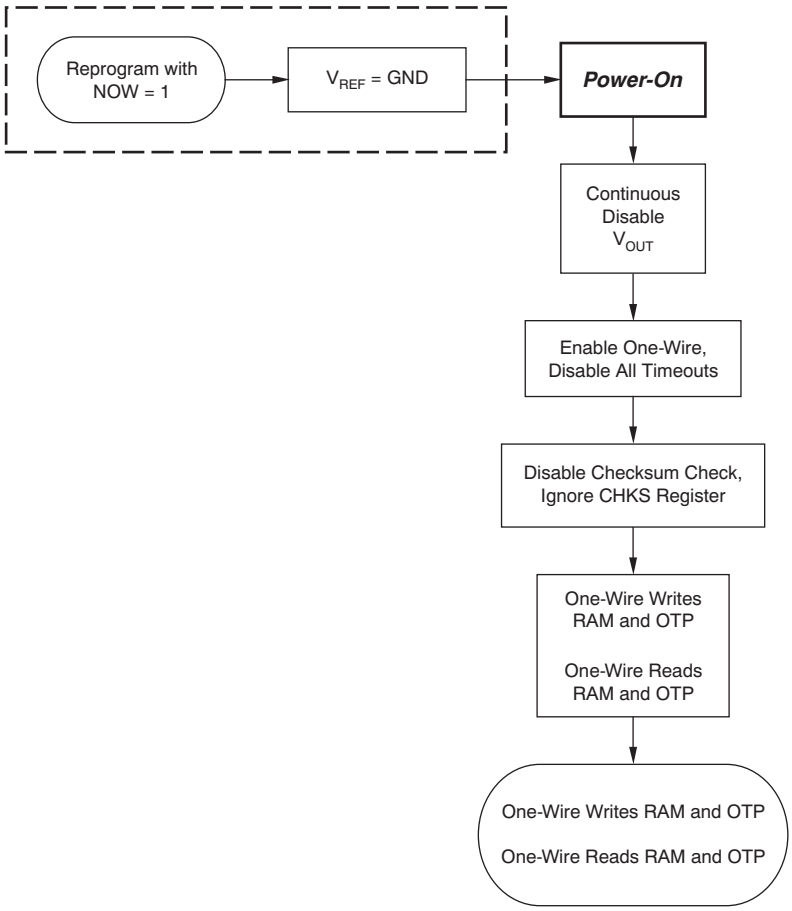


Figure 5-11. Reprogram with NOW = 1 Mode

5.6 1W Connected to V_{OUT} Program Mode, Virtual Software Lock Mode

For three-terminal sensor modules, it is essential to program and calibrate the PGA308 with one sensor out terminal. Figure 5-12 details one method of programming the PGA308 with 1W connected to V_{OUT}. The PGA308 contains an output enable counter configured by the OENC Register that enables V_{OUT} for a programmed period of time so that voltage readings can be taken, and then disables V_{OUT} so that One-Wire communication can occur. As shown in Figure 5-12, after the One-Wire interface is enabled, it stays enabled as long as valid One-Wire communications take place.

The other method of programming the PGA308 with 1W connected to V_{OUT} is to use the Virtual Software Lock Mode (see Section 5.7, *Virtual Software Lock Mode*). For Virtual Software Lock Mode to take effect, power must be cycled each time the PGA308 is to be written with new RAM values because the One-Wire interface must be enabled in order to use this mode.

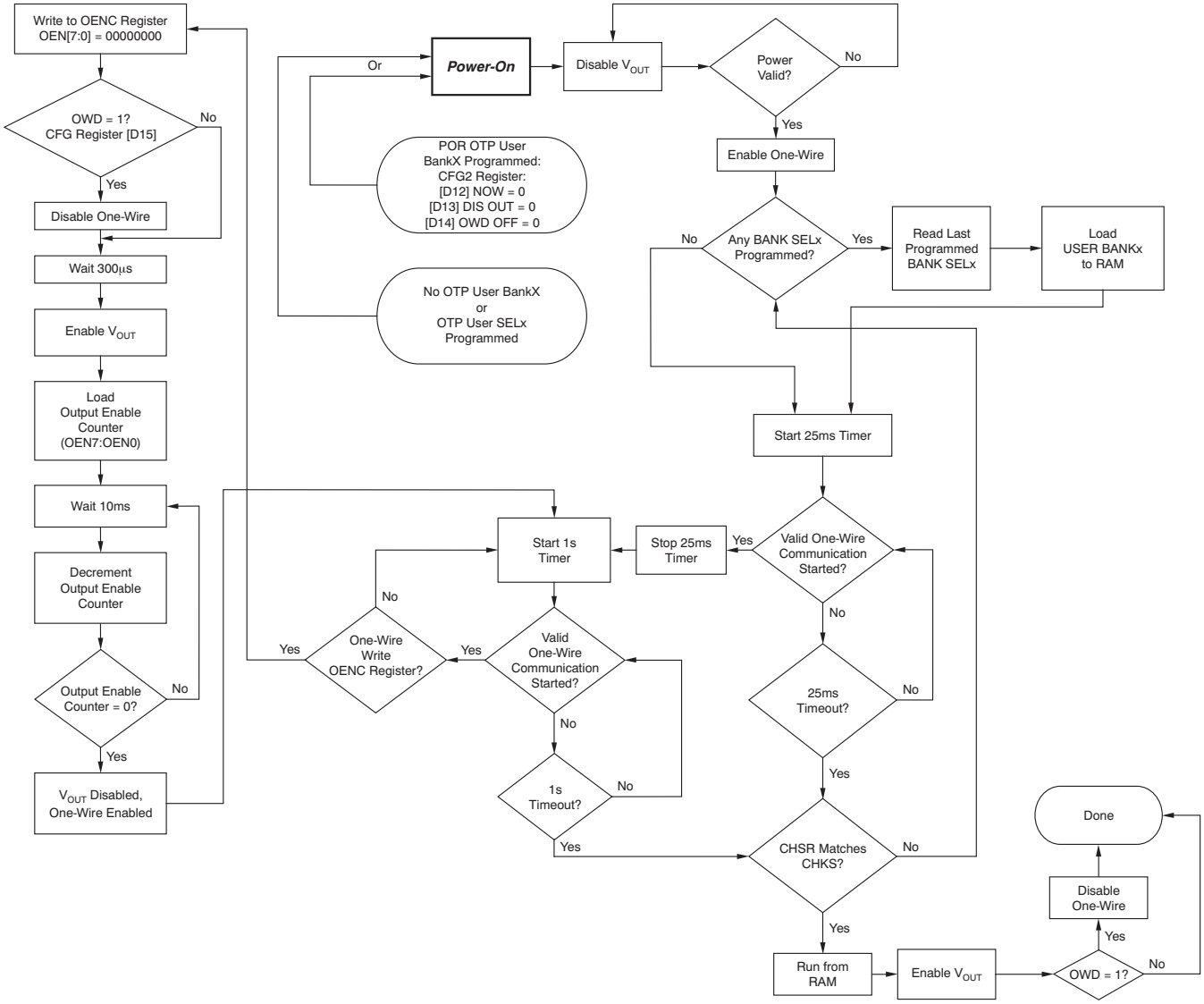
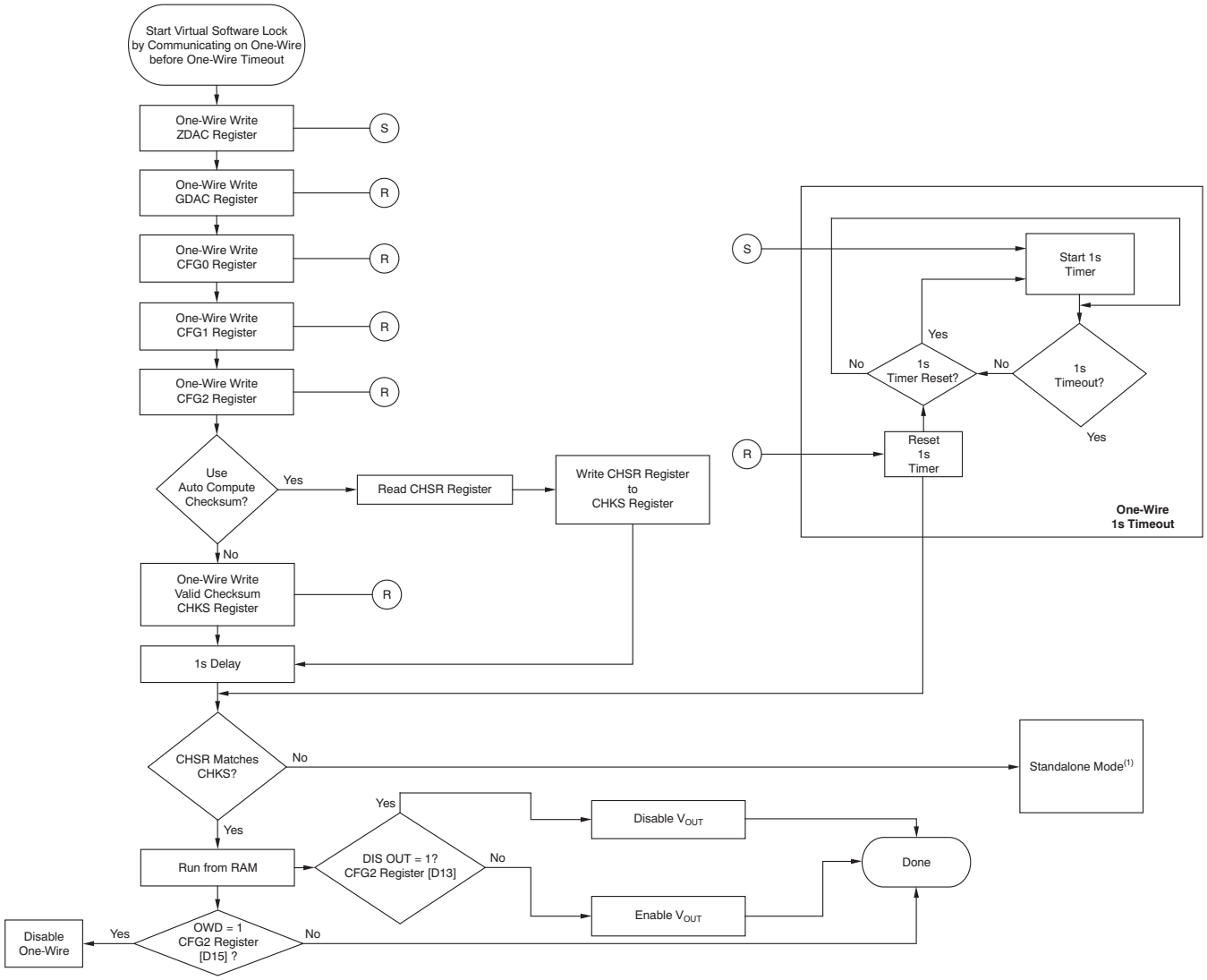


Figure 5-12. 1W Connected to V_{OUT} Program Mode

5.7 Virtual Software Lock Mode

Virtual Software Lock Mode can be used any time the One-Wire interface is enabled and when it is desired to force the PGA308 to run from RAM using the most recent register contents written into RAM.

Figure 5-13 illustrates the sequence of Virtual Software Lock Mode. Writing the desired register contents into RAM and the correct checksum into the CHKS Register forces the PGA308 to run with the current valid RAM contents.



(1) See Figure 5-10.

Figure 5-13. Virtual Software Lock Mode

5.8 Software Lock Mode

Software Lock Mode provides a method of controlling the PGA308 RAM directly by enabling the One-Wire interface, disabling any One-Wire timeouts, and disabling the checksum check normally performed between the CHSR Register and CHKS Register. This mode is designed for microcontroller control of the PGA308 through a microcontroller UART interface. It allows the PGA308 to be controlled as a flexible data acquisition front-end.

Figure 5-14 shows the algorithm for the Software Lock Mode. The SFTC Register allows a one-command write to load a preprogrammed OTP User Bank *X* directly into RAM and run from RAM using this OTP User Bank *X*. With a microcontroller controlling the PGA308 and an input multiplexer in front of the PGA308, a flexible single-supply data acquisition system is created. There are seven OTP User Banks, and therefore, seven different factory-preprogrammed configurations that could be stored in the PGA308 to be selected by the end user through the microcontroller. Alternatively, the end user can create his own configuration by communicating with the PGA308 RAM through the microcontroller. In addition, the OW DLY bit (SFTC Register [D7]) can be used to change the delay between the write portion and read portion of a One-Wire read from 1 bit (OW DLY = 0) to 8 bits (OW DLY = 1) if needed to facilitate communication to most microcontroller UART interfaces.

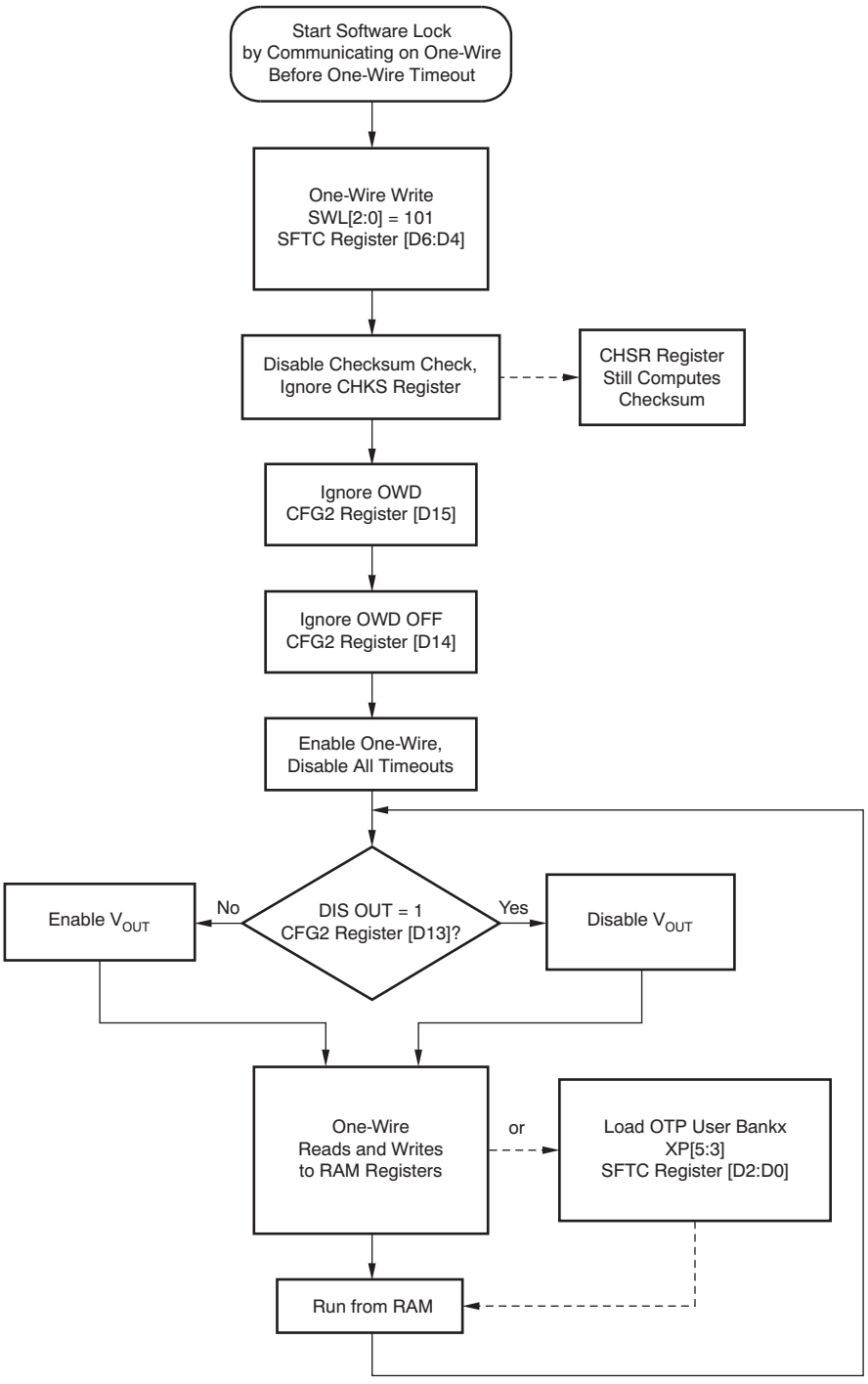


Figure 5-14. Software Lock Mode

5.9 Shutdown Mode

The PGA308 offers a Shutdown Mode to reduce quiescent current for low-power applications. V_{OUT} is disabled in Shutdown Mode. The impedance from V_{OUT} to ground in this disabled state will be the series resistance of R_{GO} + R_{FO} (see Figure 3-8 and Table 3-3) when V_{FB} is connected to V_{OUT}, which is true for most applications. This total resistance is 180kΩ typical. The typical quiescent current (which does not include current into the V_{REF} pin) is reduced from 1.3mA to 260µA. In addition, if the input pull-up current sources for fault detection (I_{PU1} and I_{PU2}; see Figure 3-12) are enabled, they will remain enabled. The dc input characteristics for V_{IN1} and V_{IN2} look the same whether or not the PGA308 is in Shutdown Mode. There is a slight reduction in noise currents on the input because the Auto-Zero input amplifier clocks are disabled in Shutdown Mode. Shutdown Mode is controlled through a One-Wire write to the SD bit (CFG2 Register [D6]). Logic 1 causes the PGA308 to be in Shutdown Mode and logic 1 returns it to normal operation. During Shutdown Mode, the digital circuitry of the PGA308 remains powered and all digital functions operate normally. Figure 5-15, Figure 5-16, Figure 5-17 and Figure 5-18 show the typical delay from the Stop bit of a One-Wire write to the SD bit to when the PGA308 is disabled or enabled, respectively. The waveforms from shutdown to enabled show a non-smooth transition that is normal for the PGA308 as internal circuitry is enabled and the overall amplifier takes a few microseconds to close its loop and control V_{OUT}.

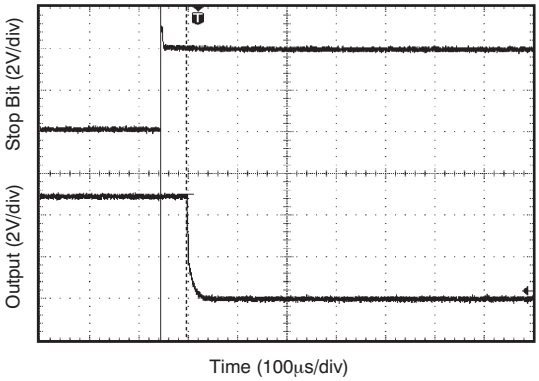


Figure 5-15. V_{OUT} Enabled to Shutdown Delay (V_S = +5V, V_{OUT} = 4.9V, C_L = 0nF)

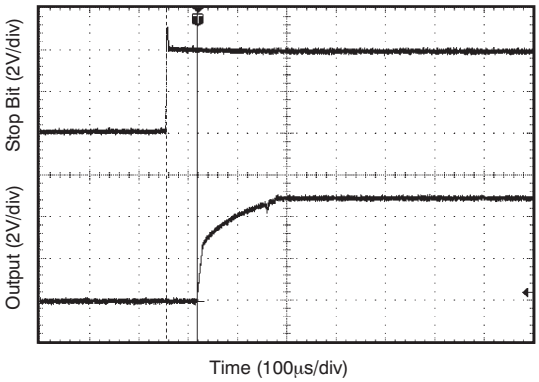


Figure 5-16. Shutdown to V_{OUT} Enabled Delay (V_S = +5V, V_{OUT} = 4.9V, C_L = 0nF)

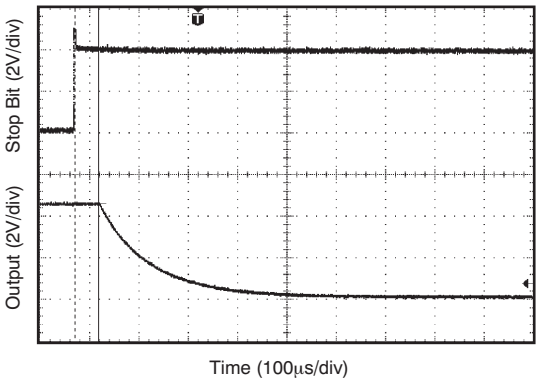


Figure 5-17. V_{OUT} Enabled to Shutdown Delay (V_S = +5V, V_{OUT} = 4.9V, C_L = 10nF)

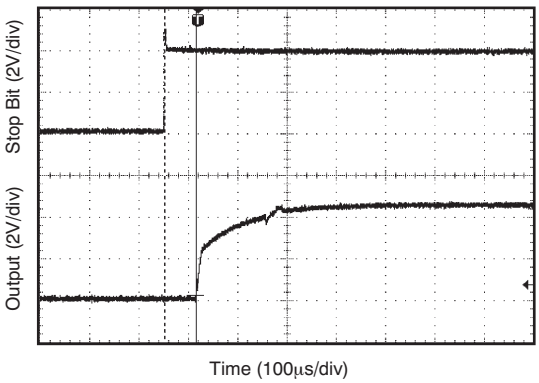


Figure 5-18. Shutdown to V_{OUT} Enabled Delay (V_S = +5V, V_{OUT} = 4.9V, C_L = 10nF)

Applications

This chapter discusses several practical applications that can be used with the PGA308.

Topic **Page**

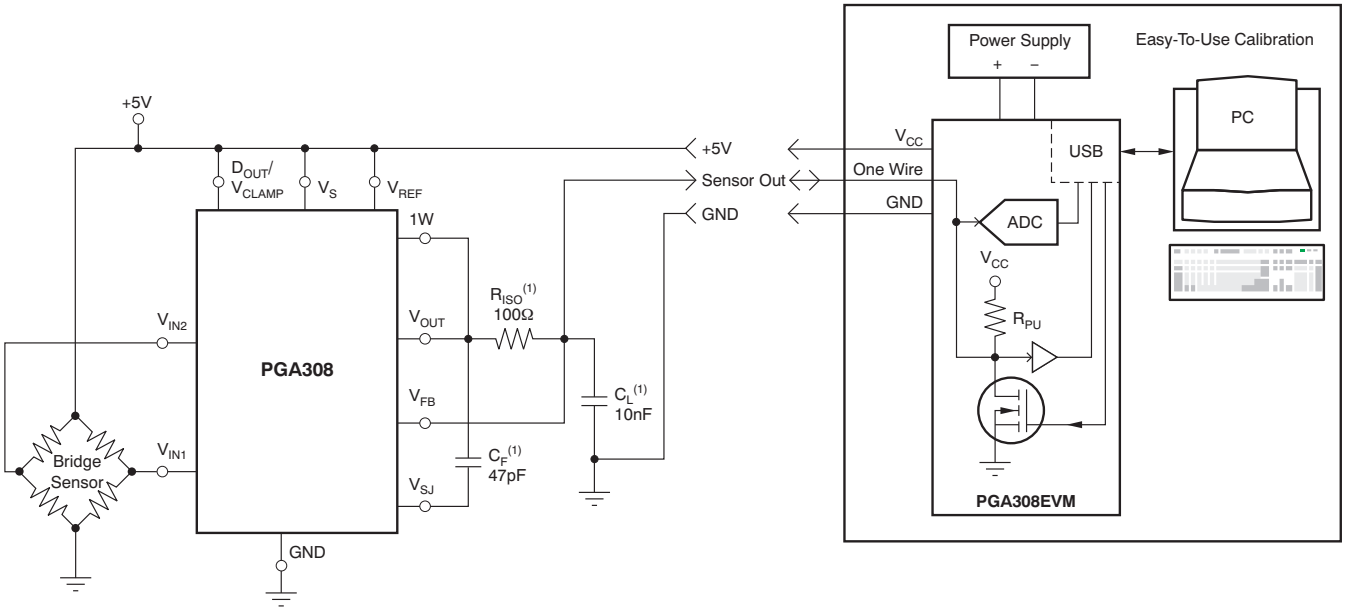
6.1 Typical Application Circuits

The PGA308 is a versatile building block with calibration and configuration for Sensor Signal Conditioning Modules. As such, the PGA308 can be used in a variety of applications. Three common applications are included here. Each application can be tested by using the PGA308EVM, a complete evaluation module that includes the programming hardware/software connection to an external PC for calibration and configuration over the One-Wire interface pin, 1W.

Figure 6-1 shows a three-terminal module, ratiometric, voltage-output, bridge sensor conditioning application. In this application, V_{REF} is connected to V_S and the resistive bridge sensor is excited by V_S, causing V_{OUT} to shift ratiometrically with regard to changes in V_S.

Figure 6-2 shows a three-terminal module, absolute, voltage-output, bridge sensor conditioning application. In this design, a precision voltage reference (the REF3240) is used for the PGA308 V_{REF} pin and to excite the resistive bridge sensor, thus creating an absolute referenced V_{OUT}.

Figure 6-3 shows a 4-20mA output module, bridge sensor conditioning application. Here the XTR116 4-20mA Current-Loop Transmitter provides a regulated 5V to power the PGA308, an accurate 4.096V reference for the PGA308 V_{REF} pin, and voltage-to-current conversion from the PGA308 V_{OUT}. Note that in this application, the 1W pin is not brought out directly; instead, it is connected to V_{OUT}, and V_{OUT} is brought out to the module output. This approach provides two benefits in the end application. First, it protects the 1W pin from real-world overvoltages and transients; and second, it allows the PGA308 V_{OUT} to be measured for module troubleshooting and debugging (for example, in a non-working module that fails because of the XTR116 or PGA308).



(1) Although not needed in all applications:

- R_{ISO} provides the PGA308 with overvoltage protection on Sensor Out.
- C_L provides EMI/RFI filtering.
- C_F provides the PGA308 with stability for the capacitive load of C_L.

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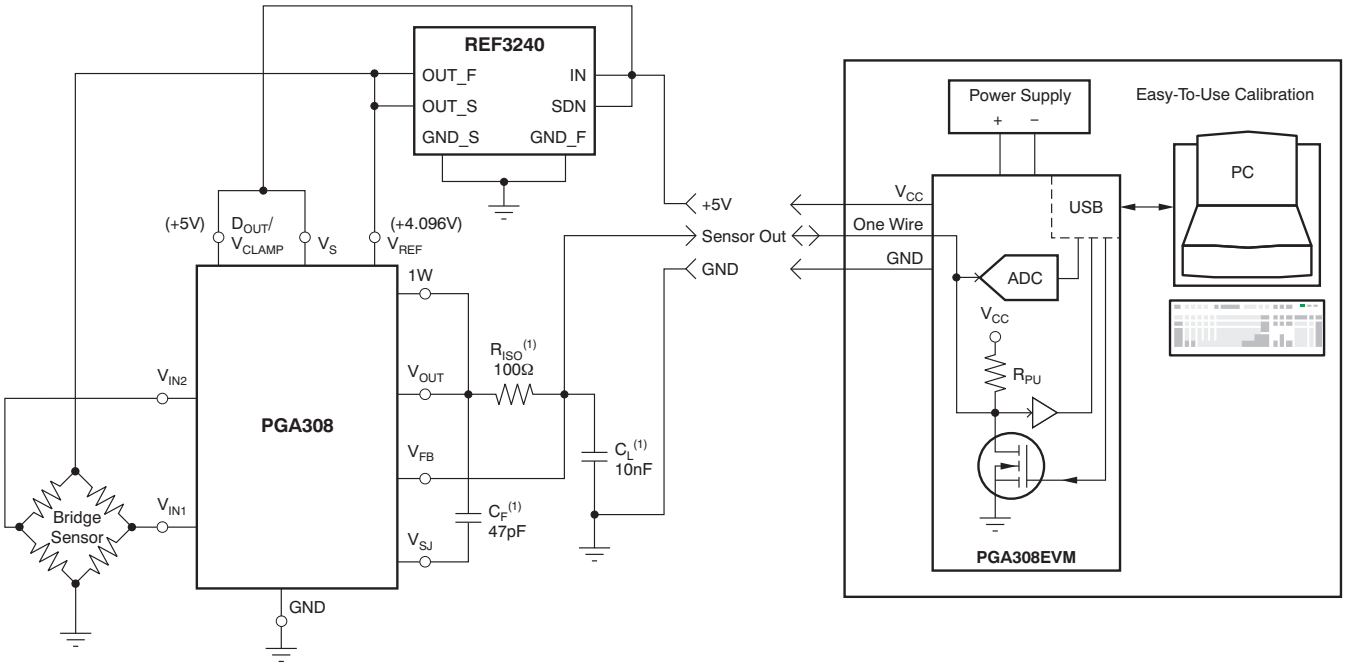
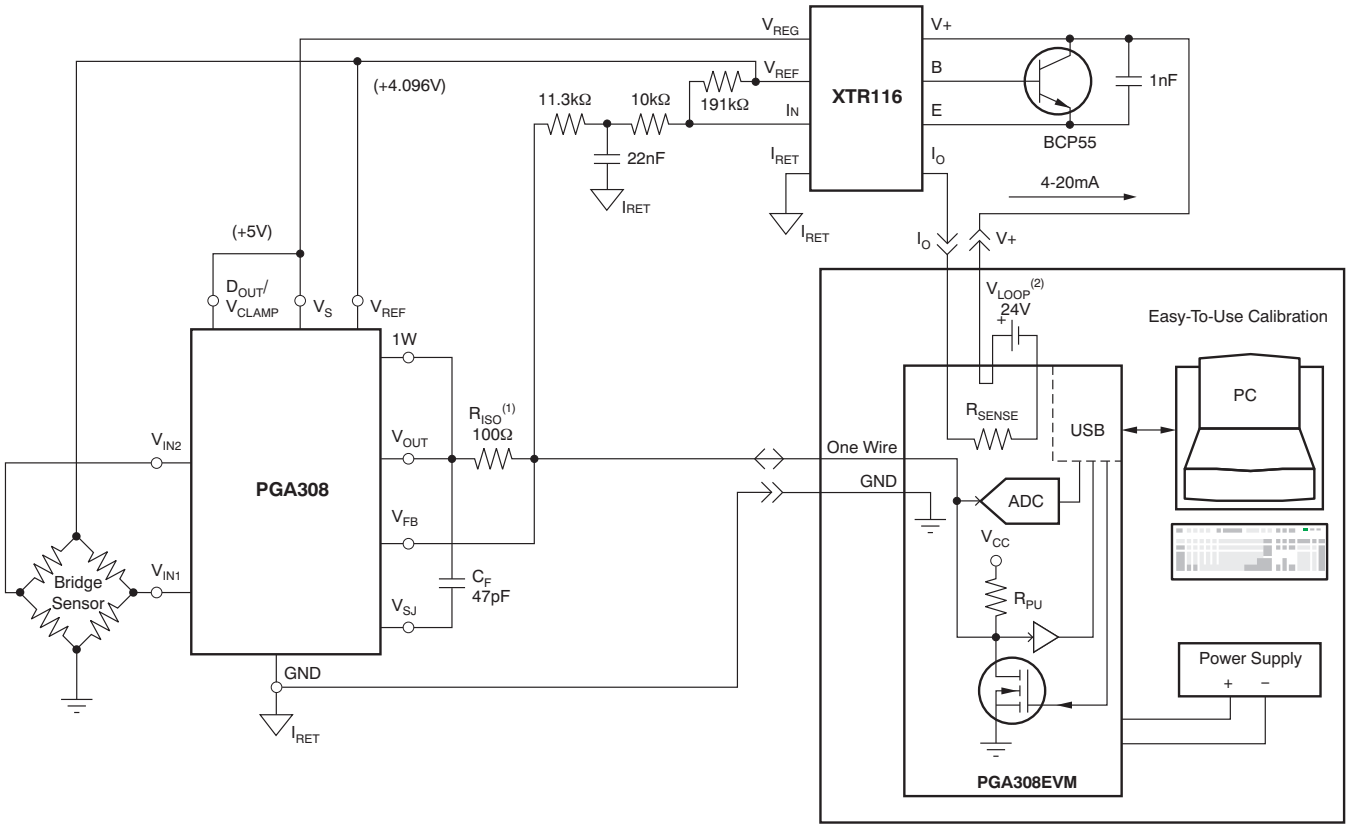
Figure 6-1. Three-Terminal Module, Ratiometric, Voltage Output, Bridge Sensor Conditioning



(1) Although not needed in all applications:

- R_{ISO} provides the PGA308 with overvoltage protection on Sensor Out.
- C_L provides EMI/RFI filtering.
- C_F provides the PGA308 with stability for the capacitive load of C_L.

Figure 6-2. Three-Terminal Module, Absolute, Voltage Output, Bridge Sensor Conditioning



(1) R_{ISO} provides 1W with overvoltage protection by using V_{OUT} internal diode clamps to $+V_S$ and GND.

(2) V_{LOOP} must be an isolated or floating supply for the PGA308EVM to program the PGA308 and read the 4-20mA output accurately.

Figure 6-3. 4-20mA Output Module, Bridge Sensor Conditioning

Detailed Register Descriptions

This chapter provides detailed descriptions of the PGA308 registers.

Topic **Page**

7.1 Memory Structure and Register Locations

This section contains detailed register descriptions.

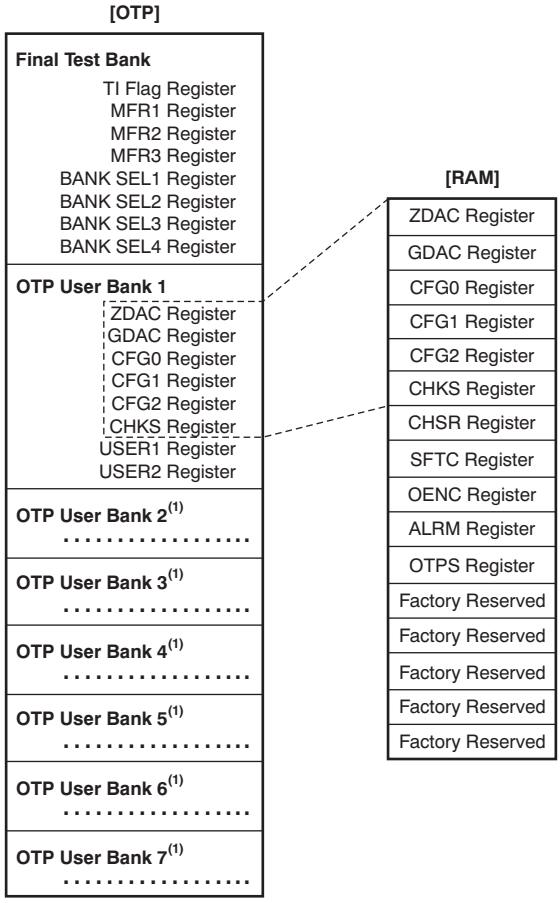


Figure 7-1. PGA308 Memory Structure

Table 7-1. [OTP] Bank and Register Locations

Read/Write Command Byte									Read/Write Command Byte								
		Bank			Register						Bank			Register			
R/$\overline{W}$	B/$\overline{R}$	P5	P4	P3	P2	P1	P0	Register Name	R/$\overline{W}$	B/$\overline{R}$	P5	P4	P3	P2	P1	P0	Register Name
								Final Test Bank									**User Bank 4**
1/0	1	0	0	0	0	0	0	TI Flag Register	1/0	1	1	0	0	0	0	0	ZDAC Register
1/0	1	0	0	0	0	0	1	MFR1 Register	1/0	1	1	0	0	0	0	1	GDAC Register
1/0	1	0	0	0	0	1	0	MFR2 Register	1/0	1	1	0	0	0	1	0	CFG0 Register
1/0	1	0	0	0	0	1	1	MFR3 Register	1/0	1	1	0	0	0	1	1	CFG1 Register
1/0	1	0	0	0	1	0	0	BANK SEL1 Register	1/0	1	1	0	0	1	0	0	CFG2 Register
1/0	1	0	0	0	1	0	1	BANK SEL2 Register	1/0	1	1	0	0	1	0	1	CHKS Register
1/0	1	0	0	0	1	1	0	BANK SEL3 Register	1/0	1	1	0	0	1	1	0	User1 Register
1/0	1	0	0	0	1	1	1	BANK SEL4 Register	1/0	1	1	0	0	1	1	1	User2 Register
								User Bank 1									**User Bank 5**
1/0	1	0	0	1	0	0	0	ZDAC Register	1/0	1	1	0	1	0	0	0	ZDAC Register
1/0	1	0	0	1	0	0	1	GDAC Register	1/0	1	1	0	1	0	0	1	GDAC Register
1/0	1	0	0	1	0	1	0	CFG0 Register	1/0	1	1	0	1	0	1	0	CFG0 Register
1/0	1	0	0	1	0	1	1	CFG1 Register	1/0	1	1	0	1	0	1	1	CFG1 Register
1/0	1	0	0	1	1	0	0	CFG2 Register	1/0	1	1	0	1	1	0	0	CFG2 Register
1/0	1	0	0	1	1	0	1	CHKS Register	1/0	1	1	0	1	1	0	1	CHKS Register
1/0	1	0	0	1	1	1	0	User1 Register	1/0	1	1	0	1	1	1	0	User1 Register
1/0	1	0	0	1	1	1	1	User2 Register	1/0	1	1	0	1	1	1	1	User2 Register
								User Bank 2									**User Bank 6**
1/0	1	0	1	0	0	0	0	ZDAC Register	1/0	1	1	1	0	0	0	0	ZDAC Register
1/0	1	0	1	0	0	0	1	GDAC Register	1/0	1	1	1	0	0	0	1	GDAC Register
1/0	1	0	1	0	0	1	0	CFG0 Register	1/0	1	1	1	0	0	1	0	CFG0 Register
1/0	1	0	1	0	0	1	1	CFG1 Register	1/0	1	1	1	0	0	1	1	CFG1 Register
1/0	1	0	1	0	1	0	0	CFG2 Register	1/0	1	1	1	0	1	0	0	CFG2 Register
1/0	1	0	1	0	1	0	1	CHKS Register	1/0	1	1	1	0	1	0	1	CHKS Register
1/0	1	0	1	0	1	1	0	User1 Register	1/0	1	1	1	0	1	1	0	User1 Register
1/0	1	0	1	0	1	1	1	User2 Register	1/0	1	1	1	0	1	1	1	User2 Register
								User Bank 3									**User Bank 7**
1/0	1	0	1	1	0	0	0	ZDAC Register	1/0	1	1	1	1	0	0	0	ZDAC Register
1/0	1	0	1	1	0	0	1	GDAC Register	1/0	1	1	1	1	0	0	1	GDAC Register
1/0	1	0	1	1	0	1	0	CFG0 Register	1/0	1	1	1	1	0	1	0	CFG0 Register
1/0	1	0	1	1	0	1	1	CFG1 Register	1/0	1	1	1	1	0	1	1	CFG1 Register
1/0	1	0	1	1	1	0	0	CFG2 Register	1/0	1	1	1	1	1	0	0	CFG2 Register
1/0	1	0	1	1	1	0	1	CHKS Register	1/0	1	1	1	1	1	0	1	CHKS Register
1/0	1	0	1	1	1	1	0	User1 Register	1/0	1	1	1	1	1	1	0	User1 Register
1/0	1	0	1	1	1	1	1	User2 Register	1/0	1		1	1	1	1	1	User2 Register

7.2 Final Test Bank [OTP] Register

7.2.1 Final Test Bank [OTP] Register Overview

Table 7-2. Final Test Bank [OTP] Register Overview

R/ $\overline{W}$	B/ $\overline{R}$	P5	P4	P3	P2	P1	P0	Register Name	Location	Type [1]	Register Contents
1/0	1	0	0	0	0	0	0	TIFlag Register	OTP	R/FW	One-time write of CC00h allows writes to all OTP banks. Done at factory final test.
1/0	1	0	0	0	0	0	1	MFR1 Register	OTP	R/FW	Factory use only.
1/0	1	0	0	0	0	1	0	MFR2 Register	OTP	R/FW	Factory use only.
1/0	1	0	0	0	0	1	1	MFR3 Register	OTP	R/FW	Factory use only.
1/0	1	0	0	0	1	0	0	BANK SEL1 Register	OTP	R/OW	POR User Bank Pointer (PGA308 uses the highest-numbered BANK SEL*x* register programmed by an OTP write.)
1/0	1	0	0	0	1	0	1	BANK SEL2 Register	OTP	R/OW	POR User Bank Pointer (PGA308 uses the highest-numbered BANK SEL*x* register programmed by an OTP write.)
1/0	1	0	0	0	1	1	0	BANK SEL3 Register	OTP	R/OW	POR User Bank Pointer (PGA308 uses the highest-numbered BANK SEL*x* register programmed by an OTP write.)
1/0	1	0	0	0	1	1	1	BANK SEL4 Register	OTP	R/OW	POR User Bank Pointer (PGA308 uses the highest-numbered BANK SEL*x* register programmed by an OTP write.)

(1) R/FW = User Read-Only/Factory OTP Write; R/OW = Read/OTP Write; POR = Power-On Reset.

7.2.2 Final Test Bank [OTP] Register Details

Table 7-3. Final Test Bank [OTP] Read/Write Command

R/ $\overline{W}$	B/ $\overline{R}$	P5	P4	P3	P2	P1	P0
1/0	1	0	0	0	P2	P1	P0

Table 7-4. TI Flag Register [OTP: Final Test Bank]

P2	P1	P0	Description	Type [1]	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	TI Flag	R/FW	TI15	TI14	TI13	TI12	TI11	TI10	TI9	TI8	TI7	TI6	TI5	TI4	TI3	TI2	TI1	TI0
0	0	0	POR Values	R/FW	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0

(1) R/FW = User Read-Only/Factory OTP Write. POR = Power-On Reset.

TI[15:0] **OTP Write Enable Bits**

A one-time write of CC00h allows writes to all OTP Banks.

TI[15:12]—Writing Ch (1100b) allows the PGA308 to read its OTP Bank on POR; performed at factory final test. (Factory Fuse Disable bit must be set to for V_{OUT} to become active in Standalone Mode).

TI[11:8]—Writing Ch (1100b) allows the PGA308 to operate in Software Lock Mode; performed at factory final test.

Table 7-5. MFR1 Register: Factory Trim Register 1 - [OTP:Final Test Bank]

P2	P1	P0	Description	Type [1]	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	MFR1	R/FW	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
0	0	1	POR Values	R/FW	X[2]	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

(1) R/FW = User Read-Only/Factory OTP Write; POR = Power-On Reset.
(2) X = Logic state depends on bit state programmed by factory.

MA[15:0] Reserved Factory Bits

Table 7-6. MFR2 Register: Factory Trim Register 2 [OTP: Final Test Bank]

P2	P1	P0	Description	Type [1]	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	MFR2	R/FW	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
0	1	0	POR Values	R/FW	X[2]	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

(1) R/FW = User Read-Only/Factory OTP Write; POR = Power-On Reset.
(2) X = Logic state depends on bit state programmed by factory.

MB[15:0] Reserved Factory Bits

Table 7-7. MFR3 Register: Factory Trim Register 3 [OTP: Final Test Bank]

P2	P1	P0	Description	Type [1]	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	MFR3	R/FW	MC15	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0
0	1	1	POR Values	R/FW	X[2]	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

(1) R/FW = User Read-Only/Factory OTP Write; POR = Power-On Reset.
(2) X = Logic state depends on bit state programmed by factory.

MC[15:0] Reserved Factory Bits

Table 7-8. BANK SEL1 Register: OTP Bank Selection 1 Register [OTP: Final Test Bank]

P2	P1	P0	Description	Type [1]	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	BANK SEL1	R/OW	0	0	0	0	0	0	0	0	0	0	0	0	0	AP5	AP4	AP3
1	0	0	POR Values	R/OW	0	0	0	0	0	0	0	0	0	0	0	0	0	X[2]	X	X

(1) R/OW = Read/OTP Write; POR = Power-On Reset.
(2) X = Logic state depends on bit state programmed by user.

AP[5:3] OTP User Bank Selection (P[5:3] in Read/Write Command Byte) for POR Standalone Mode

The POR (Power-On-Reset) OTP User Bank *X* (1 of 7) is selected for Standalone Mode by using the BANK SEL*x* registers (BANK SEL1, BANK SEL2, BANK SEL3, BANK SEL4). OTP User Bank *X* selection can be set four times by programming the BANK SEL*x* registers in order (1, 2, 3, 4). The default OTP User Bank *X* used on POR is the location stored in the last programmed BANK SEL*x* register. Therefore, if programmed, BANK SEL4 always has priority over lower-numbered bank select registers.

Table 7-9. BANK SEL1 OTP User Bank Selection

AP5	AP4	AP3	OTP User Bank *X*
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5

Table 7-9. BANK SEL1 OTP User Bank Selection (continued)

AP5	AP4	AP3	OTP User Bank *X*
1	1	0	6
1	1	1	7

Table 7-10. BANK SEL2 Register: OTP Bank Selection 2 Register [OTP: Final Test Bank]

P2	P1	P0	Description	Type (1)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	BANK SEL2	R/OW	0	0	0	0	0	0	0	0	0	0	0	0	0	BP5	BP4	BP3
1	0	0	POR Values	R/OW	0	0	0	0	0	0	0	0	0	0	0	0	0	X(2)	X	X

(1) R/OW = Read/OTP Write; POR = Power-On Reset.
(2) X = Logic state depends on bit state programmed by user.

BP[5:3] OTP User Bank Selection (P[5:3] in Read/Write Command Byte) for POR Standalone Mode

The POR (Power-On-Reset) OTP User Bank *X* (1 of 7) is selected for Standalone Mode by using the BANK SEL*x* registers (BANK SEL1, BANK SEL2, BANK SEL3, BANK SEL4). OTP User Bank *X* selection can be set four times by programming the BANK SEL*x* registers in order (1, 2, 3, 4). The default OTP User Bank *X* used on POR is the location stored in the last programmed BANK SEL*x* register. Therefore, if programmed, BANK SEL4 always has priority over lower-numbered bank select registers.

Table 7-11. BANK SEL2 OTP Bank Selection

BP5	BP4	BP3	OTP User Bank *X*
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table 7-12. BANK SEL3 Register: OTP Bank Selection 3 Register [OTP: Final Test Bank]

P2	P1	P0	Description	Type (1)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	BANK SEL3	R/OW	0	0	0	0	0	0	0	0	0	0	0	0	0	CP5	CP4	CP3
1	0	0	POR Values	R/OW	0	0	0	0	0	0	0	0	0	0	0	0	0	X(2)	X	X

(1) R/OW = Read/OTP Write; POR = Power-On Reset.
(2) X = Logic state depends on bit state programmed by user.

CP[5:3] OTP User Bank Selection (P[5:3] in Read/Write Command Byte) for POR Standalone Mode

The POR (Power-On-Reset) OTP User Bank *X* (1 of 7) is selected for Standalone Mode by using the BANK SEL*x* registers (BANK SEL1, BANK SEL2, BANK SEL3, BANK SEL4). OTP User Bank *X* selection can be set four times by programming the BANK SEL*x* registers in order (1, 2, 3, 4). The default OTP User Bank *X* used on POR is the location stored in the last programmed BANK SEL*x* register. Therefore, if programmed, BANK SEL4 always has priority over lower-numbered bank select registers.

Table 7-13. BANK SEL3 OTP Bank Selection

CP5	CP4	CP3	OTP User Bank *X*
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table 7-14. BANK SEL4 Register: OTP Bank Selection 4 Register [OTP: Final Test Bank]

P2	P1	P0	Description	Type (1)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	BANK SEL4	R/OW	0	0	0	0	0	0	0	0	0	0	0	0	0	DP5	DP4	DP3
1	0	0	POR Values	R/OW	0	0	0	0	0	0	0	0	0	0	0	0	0	X(2)	X	X

(1) R/OW = Read/OTP Write; POR = Power-On Reset.
(2) X = Logic state depends on bit state programmed by user.

DP[5:3] OTP User Bank Selection (P[5:3] in Read/Write Command Byte) for POR Standalone Mode

The POR (Power-On-Reset) OTP User Bank *X* (1 of 7) is selected for Standalone Mode by using the BANK SEL*x* registers (BANK SEL1, BANK SEL2, BANK SEL3, BANK SEL4). OTP User Bank *X* selection can be set four times by programming the BANK SEL*x* registers in order (1, 2, 3, 4). The default OTP User Bank *X* used on POR is the location stored in the last programmed BANK SEL*x* register. Therefore, if programmed, BANK SEL4 always has priority over lower-numbered bank select registers.

Table 7-15. BANK SEL4 OTP Bank Selection

DP5	DP4	DP3	OTP User Bank *X*
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

7.3 User Bank *X* [OTP] Register

7.3.1 User Bank X [OTP] Register Overview

Table 7-16. User Bank *X* [OTP] Register Overview(1)

R/ $\overline{W}$	B/ $\overline{R}$	P5	P4	P3	P2	P1	P0	Register Name	Location	Type (2)	Register Contents
1/0	1	P5	P4	P3	0	0	0	ZDAC Register(3)	OTP	R/OW	Fine Offset Adjust (Zero DAC)
1/0	1	P5	P4	P3	0	0	1	GDAC Register(3)	OTP	R/OW	Fine Gain Adjust (Gain DAC)
1/0	1	P5	P4	P3	0	1	0	CFG0 Register(3)	OTP	R/OW	Output Amplifier Gain Select; Front-End PGA Gain Select; Coarse Offset Adjust on Front-End PGA
1/0	1	P5	P4	P3	0	1	1	CFG1 Register(3)	OTP	R/OW	Fault Monitor Comparator Reference Select; Over-/Under-Scale Reference Select; External and Internal Fault Comparator Configuration; Over-/Under-Scale Enable, Thresholds and Compensation
1/0	1	P5	P4	P3	1	0	0	CFG2 Register(3)	OTP	R/OW	One-Wire Disable and Instant-On Configuration; Shutdown Select; V_{CLAMP}/D_{OUT} Select; D_{OUT} State; Front-End PGA Coarse Offset Reference Range
1/0	1	P5	P4	P3	1	0	1	CHKS Register(3)	OTP	R/OW	Checksum for ZDAC + GDAC + CFG1 + CFG2 Registers
1/0	1	P5	P4	P3	1	1	0	USER1 Register	OTP	R/OW	User information such as identification number, serial number, model number, etc.
1/0	1	P5	P4	P3	1	1	1	USER2 Register	OTP	R/OW	User information such as identification number, serial number, model number, etc.

(1) For any Bank Pointer except P[5:3] = '000'.
(2) R/OW = Read/OTP Write.
(3) For these register details, see Section 7.4.2.

7.3.2 User Bank X [OTP] Register Details

Table 7-17. User Bank *X* OTP Read/Write Command

R/ $\overline{W}$	B/ $\overline{R}$	P5	P4	P3
1/0	1	P5	P4	1

Table 7-18. USER1 Register: User1 Register - [OTP: User Bank *X*]

P2	P1	P0	Description	Type (1)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	USER1 Register	R/OW	UA15	UA14	UA13	UA12	UA11	UA10	UA9	UA8	UA7	UA6	UA5	UA4	UA3	UA2	UA1	UA0
1	1	0	POR Values	R/OW	X(2)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

(1) R/OW = Read/OTP Write; POR = Power-On Reset.
(2) X = Logic state depends on bit state programmed by user.

UA[15:0] USER1 Register Data Bits
OTP user-programmable bits for user information such as identification number, serial number, model number, etc.

Table 7-19. USER2 Register: User2 Register [OTP: User Bank *X*]

P2	P1	P0	Description	Type (1)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	USER2 Register	R/OW	UB15	UB14	UB13	UB12	UB11	UB10	UB9	UB8	UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0
1	1	1	POR Values	R/OW	X(2)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

(1) R/OW = Read/OTP Write. POR = Power-On Reset.
(2) X = Logic state depends on bit state programmed by user.

UB[15:0] USER2 Register Data Bits
OTP user-programmable bits for user information such as identification number, serial number, model number, etc.

7.4 [OTP AND RAM] Registers

7.4.1 [OTP and RAM] Register Overview

Table 7-20. [OTP and RAM] Register Overview(1)

R/ $\overline{W}$	B/ $\overline{R}$	P5	P4	P3	P2	P1	P0	Register Name	Location	Type (2)	Register Contents
1/0	1/0	P5	P4	P3	0	0	0	ZDAC Register	OTP RAM	R/OW R/W	Fine Offset Adjust (Zero DAC)
1/0	1/0	P5	P4	P3	0	0	1	GDAC Register	OTP RAM	R/OW R/W	Fine Gain Adjust (Gain DAC)
1/0	1/0	P5	P4	P3	0	1	0	CFG0 Register	OTP RAM	R/OW R/W	Output Amplifier Gain Select; Front-End PGA Gain Select; Coarse Offset Adjust on Front-End PGA
1/0	1/0	P5	P4	P3	0	1	1	CFG1 Register	OTP RAM	R/OW R/W	Fault Monitor Comparator Reference Select; Over-/Under-Scale Reference Select; External and Internal Fault Comparator Configuration; Over-/Under-Scale Enable, Thresholds and Compensation
1/0	1/0	P5	P4	P3	1	0	0	CFG2 Register	OTP RAM	R/OW R/W	One-Wire Disable and Instant-On Configuration; Shutdown Select; V_{CLAMP}/D_{OUT} Select; D_{OUT} State; Front-End PGA Coarse Offset Reference Range
1/0	1/0	P5	P4	P3	1	0	1	CHKS Register	OTP RAM	R/OW R/W	Checksum for ZDAC + GDAC + CFG1 + CFG2 Registers

(1) For any Bank Pointer except P[5:3] = '000'.
(2) R/FW = User Read-Only/Factory OTP Write; R/OW = Read/OTP Write; POR = Power-On Reset.

7.4.2 [OTP and RAM] Register Details

Table 7-21. OTP and RAM Read/Write Command

R/ $\overline{W}$	B/ $\overline{R}$	P5	P4	P3	P2	P1	P0	Memory Access
1/0	0	0	0	0	P2	P1	P0	RAM
1/0	1	See Note (1)	See Note (1)	See Note (1)	P2	P1	P0	OTP

(1) For any OTP Bank Pointer except P[5:3] = '000'

Table 7-22. ZDAC Register: Zero DAC Register [OTP and RAM]

P2	P1	P0	Description	Type (1)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	ZDAC	R/OW R/W	ZD15	ZD14	ZD13	ZD12	ZD11	ZD10	ZD9	ZD8	ZD7	ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0
0	0	0	POR Values OTP	R/OW	X(2)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
0	0	0	POR Values RAM	R/W	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) R/W = Read/Write; R/OW = Read/OTP Write; POR = Power-On Reset.
(2) X = Logic state depends on bit state programmed by user.

ZD[15:0] Zero DAC Control
16-bit unsigned data format.

Table 7-23. Zero DAC: Data Format Example (V_{REF} = +5V, V_S = +5V); See Figure 7-2

Digital Input (Hex)	Digital Input (Binary) ZD15……ZD0	Programmed Voltage Out of Zero DAC (V)	Programmed Voltage Out of Zero DAC RTO V_{OPGA} Formula	Programmed Voltage Out of Zero DAC RTO V_{OPGA} (V)	Actual Voltage Out of Zero DAC RTO V_{OPGA} (V)
0000	0000 0000 0000 0000	0	$+V_{REF}/2$	+2.5	+2.4 (1)
0001	0000 0000 0000 0001	76.293945e – 6	$+V_{REF}/2$ – (1/65536) (V_{REF})	+2.499923706	+2.4 (1)
-----	----------	----------	----------	----------	+2.4 (1)
051F	0000 0101 0001 1111	0.100021362	$+V_{REF}/2$ – (1311/65536) (V_{REF})	+2.399978638	+2.399978638
-----	----------	----------	----------	----------	----------
2000	0010 0000 0000 0000	0.625	$+V_{REF}/2$ – (8192/65536) (V_{REF})	+1.875	+1.875
4000	0100 0000 0000 0000	1.25	$+V_{REF}/2$ – (16384/65536) (V_{REF})	+1.25	+1.25
8000	1000 0000 0000 0000	2.5	$+V_{REF}/2$ – (32768/65536) (V_{REF})	0	0
C000	1100 0000 0000 0000	3.75	$+V_{REF}/2$ – (49152/65536) (V_{REF})	–1.25	–1.25
E000	1110 0000 0000 0000	4.375	$+V_{REF}/2$ – (57344/65536) (V_{REF})	–1.875	–1.875
-----	----------	----------	----------	----------	----------
FAE1	1111 1010 1110 0001	–2.399978638	$+V_{REF}/2$ – (64225/65536) (V_{REF})	–2.399978638	–2.399978638
-----	----------	----------	----------	----------	–2.4 (1)
FFFE	1111 1111 1111 1110	4.999847412	$+V_{REF}/2$ – (65534/65536) (V_{REF})	–2.499847412	–2.4 (1)
FFFF	1111 1111 1111 1111	4.999923706	$+V_{REF}/2$ – (65535/65536) (V_{REF})	–2.499923706	–2.4 (1)

(1) Limited by Zero DAC amplifier output saturation voltage.

Zero DAC Program Equation:

Decimal # Counts = [($V_{REF}/2$ – Zero DAC RTO V_{OPGA}) (65,536)] / V_{REF}

Decimal counts must be ≤ 65535

Zero DAC Program Example:

Want: Zero DAC RTO V_{OPGA} = –1.5V

Given: V_{REF} := 5V

Decimal # Counts = [(5V/2 – [–1.5V]) (65,536)] / 5V = 52,428.8

Use 52,429 counts → CCCDh → 1100 1100 1100 1101

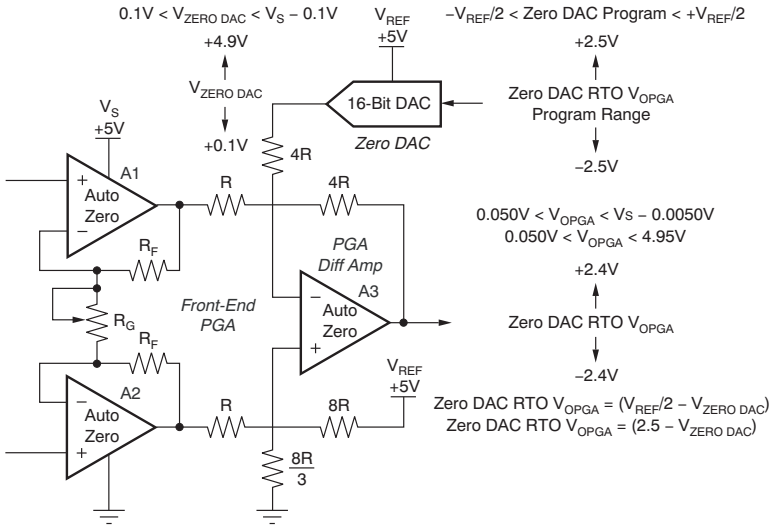


Figure 7-2. Zero DAC Scaling

Table 7-24. GDAC Register: Gain DAC Register [OTP and RAM]

P2	P1	P0	Description	Type [1]	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	GDAC	R/OW R/W	GD15	GD14	GD13	GD12	GD11	GD10	GD9	GD8	GD7	GD6	GD5	GD4	GD3	GD2	GD1	GD0
0	0	1	POR Values OTP	R/OW	X[2]	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
0	0	1	POR Values RAM	R/W	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) R/W = Read/Write. R/OW = Read/OTP Write. POR = Power-On Reset.
(2) X = Logic state depends on bit state programmed by user.

GD[15:0] Gain DAC Control
16-bit unsigned data format.

Table 7-25. Gain DAC Data Format

Digital Input (Hex)	Digital Input (Binary) GD15.....GD0	Gain Adjust
0000	0000 0000 0000 0000	0.333333333
0001	0000 0000 0000 0001	0.333343505
32F2	0011 0010 1111 0010	0.466003417
4000	0100 0000 0000 0000	0.499999999
6604	0110 0110 0000 0100	0.598999022
9979	1001 1001 0111 1001	0.733001707
CC86	1100 1100 1000 0110	0.865946449
FFFF	1111 1111 1111 1111	0.999989824

Gain DAC Equation:

1 LSB = (1.000000000 – 0.333333333) / 65536 = 1.0172526 x 10^{-5}

Decimal # counts = (Desired Gain – 0.333333333) / (1.0172526 x 10^{-5})

Decimal counts must be ≤ 65535

Gain DAC Example:

Want: Fine Gain = 0.68

Decimal # counts = (0.68 – 0.333333333) / (1.0172526 x 10^{-5}) = 34,078.72

Use 34079 counts → 0x851F → 1000 0101 0001 1111

Table 7-26. CFG0 Register: Configuration Register 0 [OTP and RAM]

P2	P1	P0	Description	Type (1)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	CFGO	R/OW R/W	GO2	GO1	GO0	GI4	GI3	GI2	GI1	GI0	OS7	OS6	OS5	OS4	OS3	OS2	OS1	OS0
0	1	0	POR Values OTP	R/OW	X(2)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
0	1	0	POR Values RAM	R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) R/W = Read/Write. R/OW = Read/OTP Write. POR = Power-On Reset.

(2) X = Logic state depends on bit state programmed by user.

GO[2:0] Output Amplifier Gain Select (1 of 7, plus internal feedback disable)

GI4 Front-End PGA Input Mux Control

GI[3:0] Front-End PGA Gain Select (1 of 16)

OS[7:0] Coarse Offset Adjust on Front-End PGA (7-bit + sign)

1LSB = (1/128)(V_{REF})(0.0256)

Table 7-27. Output Amplifier: Gain Select

GO2	GO1	GO0	Output Amplifier Gain	R_{FO} (Feedback Resistor) (1)	R_{GO} (Input Resistor) (1)
0	0	0	2	90kΩ	90kΩ
0	0	1	2.4	105kΩ	75kΩ
0	1	0	3	120kΩ	60kΩ
0	1	1	3.6	130kΩ	50kΩ
1	0	0	4.0	135kΩ	45kΩ
1	0	1	4.5	140kΩ	40kΩ
1	1	0	6	150kΩ	30kΩ
1	1	1	Disable Internal Feedback	See Note (2)	See Note (2)

(1) Refer to detailed block diagram shown in Figure 2-1.

(2) Disable Internal Feedback still leaves 180kΩ between V_{FB} and GND. V_{FB} must be connected to V_{OUT} or $V_{OUTFILT}$ for the Over-Scale and Under-Scale circuitry to work properly. See detailed block diagram shown in Figure 2-1.

Table 7-28. Front-End PGA: Mux Select

GI4 MUX CNTL	Input Mux State (1)
0	V_{IN1}= V_{INN}, V_{IN2}= V_{INP}
1	V_{IN1}= V_{INP}, V_{IN2}= V_{INN}

(1) V_{IN1} = pin 5, V_{IN2} = Pin 6. V_{INP} = positive input to Front-End PGA. V_{INN} = negative input to Front-End PGA. See Figure 2-1, *Detailed Block Diagram*.

Table 7-29. Front-End PGA: Gain Select

GI3 (GAIN SEL3)	GI2 (GAIN SEL2)	GI1 (GAIN SEL1)	GI0 (GAIN SEL0)	Front-End PGA Gain
0	0	0	0	4
0	0	0	1	6
0	0	1	0	8
0	0	1	1	12
0	1	0	0	16
0	1	0	1	32
0	1	1	0	64
0	1	1	1	100
1	0	0	0	200
1	0	0	1	400
1	0	1	0	480
1	0	1	1	600
1	1	0	0	800
1	1	0	1	960
1	1	1	0	1200
1	1	1	1	1600

Table 7-30. Coarse Offset Adjust on Front-End PGA: Data Format Example[(1)]

OS7	OS6	OS5	OS4	OS3	OS2	OS1	OS0	Coarse Offset (mV)	Coarse Offset Program
1	1	1	1	1	1	1	1	-100	- (100/128)(V_{REF})(0.0256)
•	•	•	•	•	•	•	•	•	•
1	1	1	0	0	1	0	0	-100	- (100/128)(V_{REF})(0.0256)
•	•	•	•	•	•	•	•	•	•
1	0	0	0	0	0	0	1	-1.0	- (1/128)(V_{REF})(0.0256)
1	0	0	0	0	0	0	0	0	- 0 V_{REF}
0	0	0	0	0	0	0	0	0	+ 0 V_{REF}
0	0	0	0	0	0	0	1	+1.0	+ (1/128)(V_{REF})(0.0256)
•	•	•	•	•	•	•	•	•	•
0	1	1	0	0	1	0	0	+100	+ (100/128)(V_{REF})(0.0256)
•	•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	+100	+ (100/128)(V_{REF})(0.0256)

(1) V_{REF} = +5V, 4.5V to 5.5V range; see CFG2 Register: COS VR[1:0] = '11'

Table 7-31. Coarse Offset: V_{REF} Range Select, Resolution, Range

COS VR1 [(1)]	COS VR0 [(1)]	Coarse Offset V_{REF} Range (V)	Coarse Offset Resolution (V)	Coarse Offset Range (V)
0	0	1.6 to 2.4	(1/128)(V_{REF})(0.064)	(±100mV)(V_{REF}/2)
0	1	2.4 to 3.6	(1/128)(V_{REF})(0.0427)	(±100mV)(V_{REF}/3)
1	0	3.6 to 4.5	(1/128)(V_{REF})(0.0320)	(±100mV)(V_{REF}/4)
1	1	4.5 to 5.5	(1/128)(V_{REF})(0.0256)	(±100mV)(V_{REF}/5)

(1) CFG2 Register [D11:D10]

Table 7-32. CFG1 Register: Configuration Register 1 [OTP and RAM]

P2	P1	P0	Description	Type [1]	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	CFG1	R/OW R/W	FLT REF	FLT IPU	OU CFG	FLT SEL	CMP SEL	EXT EN	INT EN	EXT POL	INT POL	OU EN	HL2	HL1	HL0	LL2	LL1	LL0
0	1	1	POR Values OTP	R/OW	X[2]	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
0	1	1	POR Values RAM	R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) R/W = Read/Write; R/OW = Read/OTP Write; POR = Power-On Reset.
(2) X = Logic state depends on bit state programmed by user.

FLT REF **Fault Monitor Reference (V_{FLT}) for Bridge Fault Mode of Operation (see FLT SEL bit CFG1 Register [D12])**
1 → $V_{FLT} = V_S$
0 → $V_{FLT} = V_{REF}$

FLT IPU **Fault Monitor Pull-up Current Source (I_{PU}, 30nA typical) Enable**
One each connected to V_{IN1} and V_{IN2} to detect open sensor conditions.
1 = Disable I_{PU}
0 = Enable I_{PU}

OU CFG **Over-Scale and Under-Scale Reference (V_{LIM}) Select**
1 → $V_{LIM} = V_S$
0 → $V_{LIM} = V_{REF}$

FLT SEL **Fault Detect Mode Select (External fault comparator trip-point selection)**
1 = Common-Mode fault
0 = Bridge fault

CMP SEL **Over-Scale and Under-Scale Amplifiers Compensation Select**
1 = Heavy compensation. Use for capacitive loads on V_{OUT} from 1nF to 10nF (max).
0 = Light compensation. Use for capacitive loads on $V_{OUT} \leq$ 200pF.

EXT EN **Enable External Fault Comparator Group (INP_HI, INP_LO, INN_LO, INN_HI)**
1 = Enable external fault comparator group
0 = Disable external fault comparator group

INT EN **Enable Internal Fault Comparator Group (A2SAT_LO, A2SAT_HI, A1SAT_LO, A1SAT_HI, A3_VCM)**
1 = Enable internal fault comparator group
0 = Disable internal fault comparator group

EXT POL **Selects V_{OUT} Output Polarity when External Fault Comparator Group Detects a Fault, if EXTEN = 1**
Note that EXT POL takes precedence over INT POL when a fault is detected.
1 = Force V_{OUT} high when any comparator in the external fault comparator group detects a fault
0 = Force V_{OUT} low when any comparator in the external fault comparator group detects a fault

INT POL **Selects V_{OUT} Output Polarity when Internal Fault Comparator Group Detects a Fault, if INTEN = 1**
1 = Force V_{OUT} high when any comparator in the internal fault comparator group detects a fault
0 = Force V_{OUT} low when any comparator in the internal fault comparator group detects a fault

OU EN **Over-Scale and Under-Scale Limit Enable**
1 = Enable Over-Scale and Under-Scale limits
0 = Disable Over-Scale and Under-Scale limits

HL[2:0] **Over-Scale Threshold Select**

LL[2:0] **Under-Scale Threshold Select**

Table 7-33. Fault Mode Select (External Fault Comparators)

FLT SEL	Fault Mode	INP_HI, INN_HI Threshold	INP_LO, INN_LO Threshold
0	Bridge	Smaller of (V_S – 1.2V) or (0.65 – V_{FLT} [(1)])	Larger of 100mV or (0.35 × V_{FLT} [(1)])
1	Common-Mode	V_S – 1.2V	100mV

(1) V_{FLT} is register selectable as V_{REF} or V_S (see FLT REF bit in CFG1 Register [D15]).

Table 7-34. Over-Scale Threshold Select[(1)]

HL2	HL1	HL0	Over-Scale Threshold (V)	Over-Scale Threshold	Over-Scale Index
0	0	0	4.9025	0.9805 × V_{LIM}	OS0
0	0	1	4.844	0.9688 × V_{LIM}	OS1
0	1	0	4.8045	0.9609 × V_{LIM}	OS2
0	1	1	4.746	0.9492 × V_{LIM}	OS3
1	0	0	4.258	0.8516 × V_{LIM}	OS4
1	0	1	3.8865	0.7773 × V_{LIM}	OS5
1	1	0	3.1445	0.6289 × V_{LIM}	OS6
1	1	1	2.8515	0.5703 × V_{LIM}	OS7

(1) V_{LIM} = +5V

Table 7-35. Under-Scale Threshold Select[(1)]

LL2	LL1	LL0	Under-Scale Threshold (V)	Under-Scale Threshold	Under-Scale Index
0	0	0	0.09765	0.01953 × V_{LIM}	US0
0	0	1	0.11715	0.02343 × V_{LIM}	US1
0	1	0	0.15625	0.03125 × V_{LIM}	US2
0	1	1	0.1758	0.03516 × V_{LIM}	US3
1	0	0	0.1953	0.03906 × V_{LIM}	US4
1	0	1	0.2344	0.04688 × V_{LIM}	US5
1	1	0	0.2539	0.05078 × V_{LIM}	US6
1	1	1	0.2735	0.0547 × V_{LIM}	US7

(1) V_{LIM} = +5V

Table 7-36. CFG2 Register: Configuration Register 2 [OTP and RAM]

P2	P1	P0	Description	Type [1]	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	CFG2	R/OW R/W	OWD	OWD OFF	DIS OUT	NOW	COS VR1	COS VR0	RFB 0	DOUT SEL	DOUT	SD	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0
1	0	0	POR Values OTP	R/OW	X[2]	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	0	0	POR Values RAM	R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) R/W = Read/Write; R/OW = Read/OTP Write; POR =Power-On Reset.
(2) X = Logic state depends on bit state programmed by user.

RFB **Reserved Factory Bit**
Set to '0' for proper operation.

OWD **One-Wire Disable Bit**
1 = Disable One-Wire
0 = Enable One-Wire

OWD OFF **One-Wire Disable Time Bit (valid only if OWD = '1')**
1 = Disable One-Wire instantly
0 = Disable One-Wire after 25ms delay (typical)

DIS OUT **V_{OUT} Disable Bit**
1 = Disable V_{OUT}
0 = Enable V_{OUT}

NOW **Instant On Bit**
V_{OUT} enable time after POR with valid checksum if DIS OUT = '0'.
1 = Instant on (V_{OUT} enabled in 60µs, typical)
0 = 25ms typical delay before V_{OUT} Enabled

COS VR[1:0] **Coarse Offset Reference Range**

DOUT SEL **Mode of Operation for Dual-Use D_{OUT}/V_{CLAMP} Pin**
1 = D_{OUT} function
0 = V_{CLAMP} function

DOUT **Logic State of D_{OUT}/V_{CLAMP} Pin (if DOUT SEL = '1')**
1 = Logic high
0 = Logic low

SD **Shutdown Mode for low standby current (260µA; does not include current into V_{REF} pin)**
1 = Shutdown
0 = Normal operation

Table 7-37. Coarse Offset: V_{REF} Range Select, Resolution, Range

COS VR1	COS VR0	Coarse Offset V_{REF} Range (V)	Coarse Offset Resolution (V)	Coarse Offset Range (V)
0	0	1.6 to 2.4	(1/128)(V_{REF})(0.064)	(±100mV)(V_{REF}/2)
0	1	2.4 to 3.6	(1/128)(V_{REF})(0.0427)	(±100mV)(V_{REF}/3)
1	0	3.6 to 4.5	(1/128)(V_{REF})(0.0320)	(±100mV)(V_{REF}/4)
1	1	4.5 to 5.5	(1/128)(V_{REF})(0.0256)	(±100mV)(V_{REF}/5)

Table 7-38. CHKS Register: Checksum Register [OTP and RAM]

P2	P1	P0	Description	Type (1)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	CHKS	R/OW	CK15	CK14	CK13	CK12	CK11	CK10	CK9	CK8	CK7	CK6	CK5	CK4	CK3	CK2	CK1	CK0
1	0	1	POR Values OTP	R/OW	X(2)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	0	1	POR Values RAM	R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) R/OW = Read/OTP Write; POR = Power-On Reset.
(2) X = Logic state depends on bit state programmed by user.

CK[15:0] Checksum for ZDAC + GDAC + CFG1 + CFG2 Registers
Correct checksum must be computed and entered by user for PGA308 in order to operate properly; refer to Table 7-39.

Table 7-39. Checksum Calculation Example for CHKS and CHSR Registers

STEP	Register/Result	Mathematical Action	Binary Carry	Hex Result	Notes
1	ZDAC	ZDAC Register contents	-------	F978	
2	GDAC	GDAC Register contents	-------	5639	
3	SUM1 =	ZDAC + GDAC	1	4FB1	SUM1_Carry = 1
4	SUM1_C =	SUM1 + SUM1_Carry	-------	4FB2	SUM1_Carry is added to LSB of SUM1
5	CFG0	CFG0 Register contents	-------	7CC5	
6	SUM2 =	SUM1_C + CFG0	0	CC77	SUM2_Carry = 0
7	SUM2_C =	SUM2 + SUM2_Carry	-------	CC77	SUM2_Carry is added to LSB of SUM2
8	CFG1	CFG1 Register contents	-------	EF0F	
9	SUM3 =	SUM2_C + CFG1	1	BB86	SUM3_Carry = 1
10	SUM3_C =	SUM3 + SUM3_Carry	-------	BB87	SUM3_Carry is added to LSB of SUM3
11	CFG2	CFG2 Register contents	-------	C171	
12	SUM4 =	CFG2 + SUM3_C	1	7CF8	SUM4_Carry = 1
13	SUM4_C =	SUM4 + SUM4_Carry	-------	7CF9	SUM4_Carry is added to LSB of SUM4
14	CHKS or CHSR	NOT (SUM4_C)	-------	8306	Invert each equivalent binary bit in hex number for SUM4_C. Must be manually entered into CHKS Register and is automatically computed by PGA308 state machine and stored in CHSR Register

7.5 [RAM] Register

7.5.1 [RAM] Register Overview

Table 7-40. [RAM] Register Overview

R/ $\overline{W}$	B/ $\overline{R}$	P5	P4	P3	P2	P1	P0	Register Name	Location	Type (1)	Register Contents
1/0	1/0	0	0	0	0	0	0	ZDAC Register(2)	OTP RAM	R/OW R/W	Fine Offset Adjust (Zero DAC)
1/0	1/0	0	0	0	0	0	1	GDAC Register(2)	OTP RAM	R/OW R/W	Fine Gain Adjust (Gain DAC)
1/0	1/0	0	0	0	0	1	0	CFG0 Register(2)	OTP RAM	R/OW R/W	Output Amplifier Gain Select; Front-End PGA Gain Select; Coarse Offset Adjust on Front-End PGA
1/0	1/0	0	0	0	0	1	1	CFG1 Register(2)	OTP RAM	R/OW R/W	Fault Monitor Comparator Reference Select; Over/Under-Scale Reference Select; External and Internal Fault Comparator Configuration; Over/Under-Scale Enable, Thresholds, and Compensation
1/0	1/0	0	0	0	1	0	0	CFG2 Register(2)	OTP RAM	R/OW R/W	One-Wire Disable and Instant-On Configuration; Shutdown Select; V_{CLAMP}/D_{OUT} Select; D_{OUT} State; Front-End PGA Coarse Offset Reference Range
1/0	1/0	0	0	0	1	0	1	CHKS Register(2)	OTP RAM	R/OW R/W	Checksum for ZDAC + GDAC + CFG1 + CFG2 Registers
1/0	0	0	0	0	1	1	0	CHSR Register	RAM	R	Checksum read for internally calculated Checksum for ZDAC + GDAC + CFG1 + CFG2 Registers
1/0	0	0	0	0	1	1	1	SFTC Register	RAM	R/W	Software Control for Software Lock Mode (POR default mode is Standalone Mode); One-Wire Turnaround Delay Select; OTP Bank Select for Software Lock Mode
1/0	0	0	0	1	0	0	0	OENC Register	RAM	R/W	Output Counter Control for when One-Wire Interface (1W) is connected to V_{OUT} in three-terminal module applications
1	0	0	0	1	0	0	1	ALRM Register	RAM	R	Fault Monitor Comparator Outputs
1/0	0	0	0	1	0	1	0	OTPS Register	RAM	R/W	OTP Memory Status/Control Register
1/0	0	0	0	1	0	1	1	Factory Reserved	RAM	R	Factory Reserved
1/0	0	0	0	1	1	0	0	Factory Reserved	RAM	R	Factory Reserved
1/0	0	0	0	1	1	0	1	Factory Reserved	RAM	R	Factory Reserved
1/0	0	0	0	1	1	1	0	Factory Reserved	RAM	R	Factory Reserved
1/0	0	0	0	1	1	1	1	Factory Reserved	RAM	R	Factory Reserved

(1) R = Read-Only; R/W = Read/Write; R/FW = User Read-Only/Factory OTP Write; R/OW = Read/OTP Write.
(2) For these register details, see [OTP and RAM] Register Details section.

7.5.2 [RAM] Register Details

Table 7-41. RAM Read/Write Command

R/ $\overline{W}$	B/ $\overline{R}$	P5	P4	P3	P2	P1	P0
1/0	0	0	0	P3	P2	P1	P0

Table 7-42. CHSR Register: Software Calculated Register Checksum Register [RAM]

P3	P2	P1	P0	Description	Type (1)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	CHKS	R/W	CS15	CS14	CS13	CS12	CS11	CS10	CS9	CS8	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
0	1	1	0	POR Values	R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) R/W = Read/Write; POR = Power-On Reset.

CS[15:0] **PGA308 Internal State Machine Calculation of Checksum for ZDAC + GDAC + CFG1 + CFG2 Registers**
See Table 7-39, *Checksum Calculation Example for CHKS and CHSR Registers*

Table 7-43. SFTC Register: Software Control Register [RAM]

P3	P2	P1	P0	Description	Type (1)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	SFTC	R/W	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0	CHKS FLG (2)	OW DLY	SW L2	SW L1	SW L0	RFB 0	XP5	XP4	XP3
0	1	1	1	POR Values	R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) R/W = Read/Write; POR = Power-On Reset.
(2) Read-only bit.

RFB **Reserved Factory Bit**
Set to '0' for proper operation.

CHKS FLG **Register Checksum Bit (Read-only)**
1 = Register checksum correct
0 = Register checksum error

OW DLY **One-Wire Delay Bit**
1 = 8-bit delay from transmit to receive during One-Wire reads
0 = 1-bit delay from transmit to receive during One-Wire reads

SWL[2:0] **Software Lock Mode Control**
Direct R/W to RAM registers configures/controls the PGA308; see Figure 5-14.

XP[5:3] **OTP Bank Selection for Software Lock Mode**
If XP[5:3] = '000', then the PGA308 operates from data written into the RAM registers from the user. Any other combination will load the respective OTP User Bank *X* contents into the respective RAM register locations and then operate the PGA308 from RAM.

Table 7-44. Software Lock Mode Control Bits

SWL2	SWL1	SWL0	Mode of Operation
0	0	0	Standalone (Runs from OTP)
0	0	1	Standalone (Runs from OTP)
0	1	0	Standalone (Runs from OTP)
0	1	1	Standalone (Runs from OTP)
1	0	0	Standalone (Runs from OTP)
1	0	1	SOFTWARE LOCK (Runs from RAM)
1	1	0	Standalone (Runs from OTP)
1	1	1	Standalone (Runs from OTP)

Table 7-45. OTP Bank Selection for Software Lock Mode

XP5	XP4	XP3	OTP User Bank Selected
0	0	0	None
0	0	1	User Bank 1
0	1	0	User Bank 2
0	1	1	User Bank 3
1	0	0	User Bank 4
1	0	1	User Bank 5
1	1	0	User Bank 6
1	1	1	User Bank 7

Table 7-46. OENC Register: Output Enable Control Register [RAM]

P3	P2	P1	P0	Description	Type (1)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	OENC	R/W	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0	OEN 7	OEN 6	OEN 5	OEN 4	OEN 3	OEN 2	OEN 1	OEN 0
1	0	0	0	POR Values	R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) R/W = Read/Write; POR = Power-On Reset.

RFB **Reserved Factory Bit**
Set to '0' for proper operation.

OEN[7:0] **Output Enable Counter for One-Wire Interface / V_{OUT} Multiplexed Mode**
Any non-zero value starts V_{OUT} enable initial count, decremented every 10ms to zero count and then V_{OUT} is disabled. After V_{OUT} is disabled, a one-second internal timer is set. If serial communication from an outside controller takes place on the One-Wire interface (1W pin), then V_{OUT} remains disabled as long as the PGA308 is addressed with a valid One-Wire transaction at least once per second (see Figure 5-12).

Table 7-47. Output Enable Counter for One-Wire Interface / V_{OUT} Multiplexed Mode(1)

Digital Input (Binary) OEN7…...OEN0	Decimal Equivalent (Initial Counter Value)	V_{OUT} Enable Timeout (ms)
0000 0000	0	0
0010 0000	32	320
0100 0000	64	640
0110 0000	96	960
1000 0000	128	1280
1010 0000	160	1600
1100 0000	192	1920
1110 0000	224	2240
1111 1111	255	2550

(1) V_{OUT} Enable Timeout = Initial Counter Value × 10ms.

Table 7-48. ALRM Register: Alarm Register [RAM]

P3	P2	P1	P0	Description	Type [1]	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	ALRM	R	0	0	0	0	0	0	0	A1SAT_HI	A1SAT_LO	A2SAT_HI	A2SAT_LO	A3SAT_LO	INN_HI	INN_LO	INP_HI	INP_LO
1	0	0	1	POR Values	R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) R = Read-Only; POR = Power-On Reset.

See Section 3.6, *Fault Monitor Circuitry*, for details.

Internal Fault Comparators (Logic 1 = Fault)

A1SAT_HI PGA A1 op amp saturation high.

A1SAT_LO PGA A1 op amp saturation low.

A2SAT_HI PGA A2 op amp saturation high.

A2SAT_LO PGA A2 op amp saturation low.

A3SAT_LO PGA A3 op amp saturation low.

External Fault Comparators (Logic 1 = Fault)

INN_HI V_{INN} FLT+ comparator.

INN_LO V_{INN} FLT– comparator.

INP_HI V_{INP} FLT+ comparator.

INP_LO V_{INP} FLT– comparator.

NOTE: FLT+ and FLT– (external fault comparator thresholds) determined by FLT REF and FLT SEL in CFG1 Register [D15, D12].

Table 7-49. OTPS Register: OTP Memory Status Register [RAM]

P3	P2	P1	P0	Description	Type [1]	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	OTPS	R/W	OTP EN	RFB 0	RFB 0	OTP BSY[2]	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0	RFB 0
1	0	1	0	POR Values	R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) R = Read-Only; POR = Power-On Reset.
(2) Read-Only bit.

RFB **Reserved Factory Bit**
Set to '0' for proper operation.

OTP EN **OTP Enable Bit**
1 = Enable write to OTP
0 = Disable write to OTP

OTP BSY **OTP Write Busy Bit (Read-only)**
1 = Busy Writing to OTP
0 = Done Writing to OTP

Table 7-50. Factory Reserved Registers: [RAM] DO NOT WRITE TO THESE REGISTERS

P3	P2	P1	P0	Description	Type	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	Factory Reserved	R	RFB(1)	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB
1	1	0	0	Factory Reserved	R	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB
1	1	0	1	Factory Reserved	R	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB
1	1	1	0	Factory Reserved	R	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB
1	1	1	1	Factory Reserved	R	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB	RFB

(1) RFB = Reserved factory bit. DO NOT WRITE TO THIS BIT.

Revision History

Changes from A Revision (December 2010) to B Revision	Page
• Changed first row of Table 7-9	83
• Changed first row in Table 7-11	84
• Changed first row in Table 7-13	85
• Changed first row in Table 7-15	85

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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