User's Guide

INA2191EVM

ABSTRACT

This user's guide describes the characteristics, operation, and use of the INA2191 evaluation module (EVM). This EVM is designed to evaluate the performance of the dual-channel, bidirectional, voltage-output, INA2191 current shunt monitor in a variety of configurations. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the INA2191EVM. This document also includes a schematic, reference printed circuit board (PCB) layouts, and a complete bill of materials (BOM).

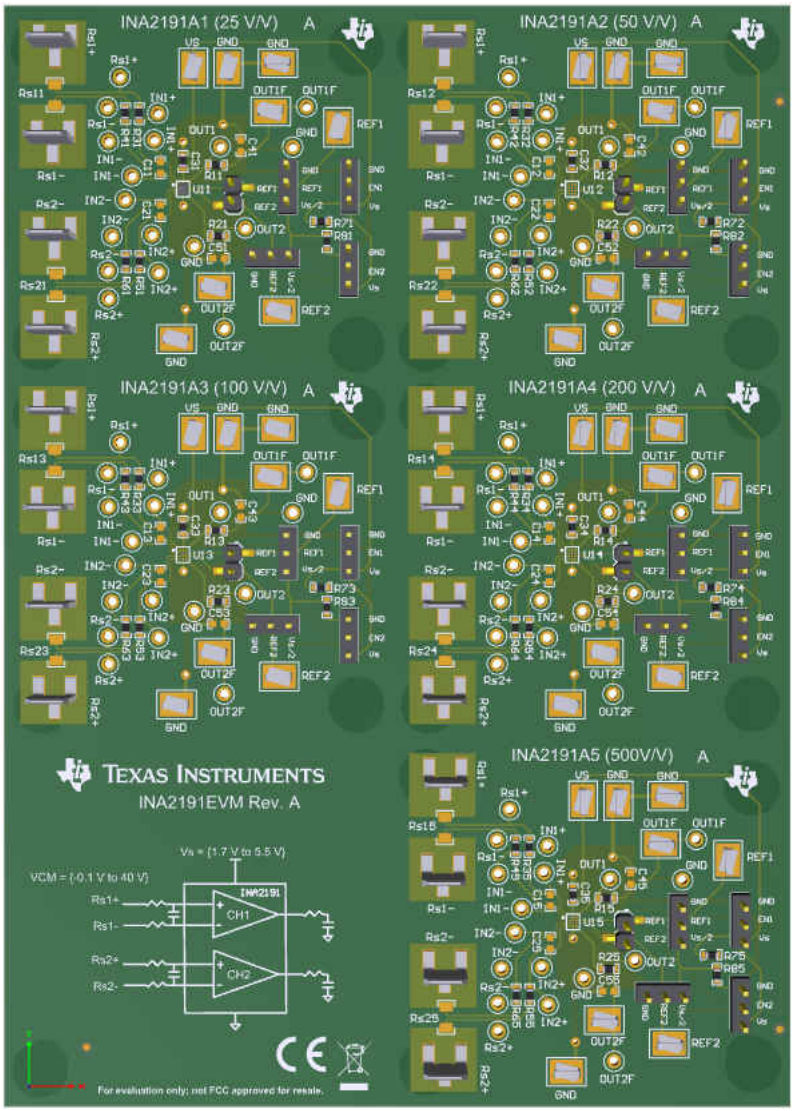

Table of Contents

List of Figures

List of Tables

Trademarks

All trademarks are the property of their respective owners.

1 Overview

The INA2191 device is a voltage-output, dual channel, bidirectional current sense amplifier in a DSBGA (12) package. As shown in Table 1-1, the INA2191 has gains that range from 25V/V to 500 V/V, depending on the gain option that is selected. The voltage developed across the device inputs is amplified by the corresponding gain of the specific device, and is presented at the output pin plus the bias voltage supplied to the corresponding reference pin. The device can accurately sense voltage drops across shunts at -0.1-V to +40-V common-mode voltages, independent of supply voltage. The device survives common-mode voltages from –0.3 V to +42 V. The device operates with supply voltages between 1.7 V and 5.5 V, and draws a typical of 48 µA per channel at room temperature.

Table 1-1. INA2191 Gain Option Summary

Product INA2191	Gain (V/V)
INA2191A1	25
INA2191A2	50
INA2191A3	100
INA2191A4	200
INA2191A5	500

1.1 EVM Kit Contents

Table 1-2 summarizes the contents of the INA2191EVM kit. Contact the nearest Texas Instruments Product Information Center if any component is missing.

Table 1-2. INA2191EVM Kit Contents

Item	Item Part Number	Quantity
INA2191EVM test board	INA2191EVM	1
Connector Pin receptacle	3-331272-8	10
Shunt, 100mil, gold plated, black	SNT-100-BK-G	20

1.2 Related Documentation From Texas Instruments

This document provides information regarding Texas Instruments' integrated circuits used in the assembly of the INA2191EVM.

Table 1-3. Related Documentation

Document	Literature Number
INA2191 product data sheet	SLYS020

2 Hardware

The INA2191EVM provides a basic functional evaluation of the INA2191. The fixture layout is not intended to be a model for the target circuit, nor is it laid out for electromagnetic compatibility (EMC) testing. The INA2191EVM is one PCB with five optional PCB cutouts the engineer can use to test each of the five gain options (1 to 5) listed in Table 1-1. Each PCB cutout has one INA2191A*n* device (where *n* is 1, 2, 3, 4, or 5), test points and sockets for external hardware connections, and pads to solder down optional circuitry.

2.1 Features

The INA2191EVM PCB provides the following features:

- Evaluation of all gain options through identical, scored panels
- Ease of access to device pins with test points
- Pads and sockets for optional filtering at the input pins and output pins
- Multiple input signal options, including a method to solder a shunt resistor (1206) and safely measure current up to 5 A.

See the device data sheet for comprehensive information about the INA2191 and the available gain options.

3 Operation

3.1 Quick Start Setup

Follow these procedures to set up and use one of the INA2191EVM panels. For these instructions, n is gain option 1, 2, 3, 4, or 5.

1. Choose the desired gain option by choosing the panel with the label showing the desired gain.
2. Choose the settings for the enable (EN1 and EN2) and reference (REF1 and REF2) pins using jumpers JA2n and JA1n for the enable pins and J5n and J6n for the reference pins.
3. Shorting an enable pin to the supply voltage (Vs) turns the device's corresponding channel on, while shorting the enable pin to ground turns this channel off.
4. Shorting the reference pin to ground biases the output of the corresponding channel to ground, while shorting the reference pin to Vs/2 pin biases the output of the corresponding channel to mid-supply. Note that the on-board Vs/2 voltage is available to easily bias the device with no extra source; however, it is best practice to drive the reference pin with a low-impedance voltage source and thus inserting a buffer in between Vs/2 and the reference pin will ensure performance according to device datasheet specifications.
5. Connect an external DC supply voltage (between 1.7 V and 5.5 V) to a VS test point. Connect the ground reference of that supply to a GND test point on the same panel.
6. Provide a differential input voltage signal across the input pins and ensure the common-mode voltage (V_{CM}) of this differential signal is within the operational V_{CM} rating of the device.
   a. The differential signal should be supplied across the input pins by driving the signal across J1n and J2n for channel 1 or J3n and J4n for channel 2 on the EVM, as explained in Section 3.2.
7. Check to make sure all grounds of the sources and EVM are common and connected with low-impedance connections.

3.2 Measurements

The user can either emulate the voltage developed across a sense resistor based on a given set of system conditions with the INA2191EVM, or connect the device inputs to an external shunt resistor. The user can also solder a surface-mount technology (SMT) shunt resistor across the Rs+ and Rs– pads, and these inputs can be connected in series with the external system and load.

Note the following where n is gain option 1, 2, 3, 4, or 5.

- Each device channel has its own pads for an optional shunt resistor
  - Rs1n is shunt resistor for channel 1, while Rs2n is the shunt resistor for channel 2.
  - When running current through Rs1 or Rs2, the user can connect the load and source to the shunt resistor using the quick-connect tabs J1n and J2n for Rs1n or J3n and J4n for Rs2n.
  - All shunt resistors will be referred to as Rshunt.
- Each device channel has its own input pins with test points
  - IN1+ and IN1– are the silkscreen markings for channel 1 input pins IN+1 and IN–1 respectively.
  - IN2 + and IN2– are the silkscreen markings for channel 2 input pins IN+2 and IN–2 respectively.
  - All input nodes will be referred to as IN+ and IN– or just as input pins.
- Input pins connect to shunt resistor pads for each channel on each gain variant panel
  - Rs1+ and Rs1– are the same nets as IN1+ and IN1– respectively for channel 1.
  - Rs2+ and Rs2– are the same nets as IN2+ and IN2– respectively for channel 2.
  - The shunt resistor and input pin nodes become different once the input resistors (R3n, R4n, R5n, R6n) are increased to resistance greater than 0 Ω.

To configure a measurement evaluation without a shunt resistor, follow this procedure:

1. Connect a positive differential voltage across the device channel inputs from IN+ to IN– (or Rs1+ to Rs–) using J1n and J2n tabs for channel 1 and J3n and J4n tabs for channel 2.
   a. For any unused channel, short the inputs and tie these inputs to ground or some other valid common-mode voltage (V_{CM}).
2. If the differential supply is floating, then connect a –0.1-V to 40-V V_{CM} to the inputs of the device channel. Connect the positive lead of the V_{CM} source to the IN– tab and V_{CM} source ground to a GND test point.

   a. This action effectively raises the absolute common-mode voltage of the input pins, while still retaining a positive input differential signal.
3. Provide the desired reference voltage to the REF1 node for channel 1 or REF2 node for channel 2.
4. Measure the output voltage at OUT1/OUT1F for channel or OUT2/OUT2F for channel 2 with respect to ground (GND) or with respect to the channel's reference voltage.

To configure a measurement evaluation with a shunt resistor, follow this procedure:

1. Solder a 1206 resistor at the Rshunt pads that connects to the IN+ and IN– inputs.
2. Connect the Rshunt tabs (J1n and J2n for channel 1 or J3n and J4n for channel 2) in series with the load and bus voltage sources while powered off.

WARNING

Make sure that the equipment (shunt resistor, wires, connectors, and so on) can support the amperage and power dissipation first before you measure the current. Also make sure that the current flowing through J1n, J2n, J3n, or J4n does not exceed 5 A. Failure to do so can result in hot surfaces (> 55 °C), damage to the EVM, or personal injury.

3. Power on the system and measure the output voltage at the OUT/OUTF test points for the correct channel. Output voltage with respect to ground is equal to the gain of the device multiplied by the differential voltage plus the reference voltage, where the differential voltage is the exact voltage from IN+ to IN– input pins.

4 EVM Components

This section summarizes the INA2191EVM components. For these instructions, n is gain option 1, 2, 3, 4, or 5.

4.1 R1n, R2n, R3n, R4n, R5n, R6n, C1n, C2n, C4n, C5n

R1n, R2n, R3n, R4n, R5n, R6n are factory-installed 0-Ω 0603 resistors.

C1n, C2n, C4n, C5n are not populated.

Collectively, these pads allow user-defined filters for the input pins (IN+ and IN–) and the output pins (OUT) of the INA2191. If a filter is desired, remove these resistors and replace them with > 0-Ω SMT resistors and populate the capacitor pads with capacitors.

4.1.1 J5n, J6n, JA1n, JA2n

These headers allow the user to quickly set voltage levels for the reference and enable pins.

4.2 C3n

C3n is a 0.1-µF, power-supply bypass capacitor for each INA2191 gain variant.

4.3 Rs1n and Rs2n (Rshunt)

Rshunt is unpopulated, but allows the user to solder down a surface-mount shunt resistor between the Rs+ and Rs– pads sensed by IN+ and IN– input pins. If used, make sure Rshunt has proper power dissipation for the selected current load and below 5 A. The chosen resistor must have a 1206 footprint.

4.3.1 R7n, R8n

These are populated 4.99 kΩ, 1%, 0603 resistors. They form a resistor divider network off the supply voltage (Vs) to give the user a simple mid-supply voltage (Vs/2) that can be tied directly to the device's reference pins.

4.4 U1n (INA2191)

U1n is the location for the INA2191An test device.

Consider these factors when selecting the appropriate device gain:

- The differential input voltage is either applied across the inputs or developed based on the load current that flows through the shunt resistor.
- Make sure that the output voltage does not exceed the supply voltage. This limiting factor requires attention to device selection.
- The selected device must allow the output voltage to remain within the acceptable range after the developed input voltage is amplified by the respective device gain. The output voltage must remain within the device-specified swing limitations for response in the linear range.
- An output below the minimum allowable output requires a device with a higher gain. Likewise, an output above the maximum allowable output requires a device with a lower gain.

4.5 S1n, S2n, S3n, S4n, S5n, S6n, S7n, S8n, S9n, SA1n, SA2n, SA3n, SA4n, SA5n, SA6n, SA7n, SA8n, SA9n

These are unpopulated single pin receptacle connectors provide on-board test points. They can be populated with solder termination as needed to allow for testing the INA2191 with various filters using through-hole components.

5 Schematic, PCB Layout, and Bill of Materials

Note

Board layouts are not to scale. These figures are intended to show how the board is laid out. They are not intended to be used for INA2191EVM PCB manufacturing.

5.1 Schematics

Figure 5-1 through Figure 5-5 show the schematics for the A pinout of the INA2191EVM PCB for all gain options.

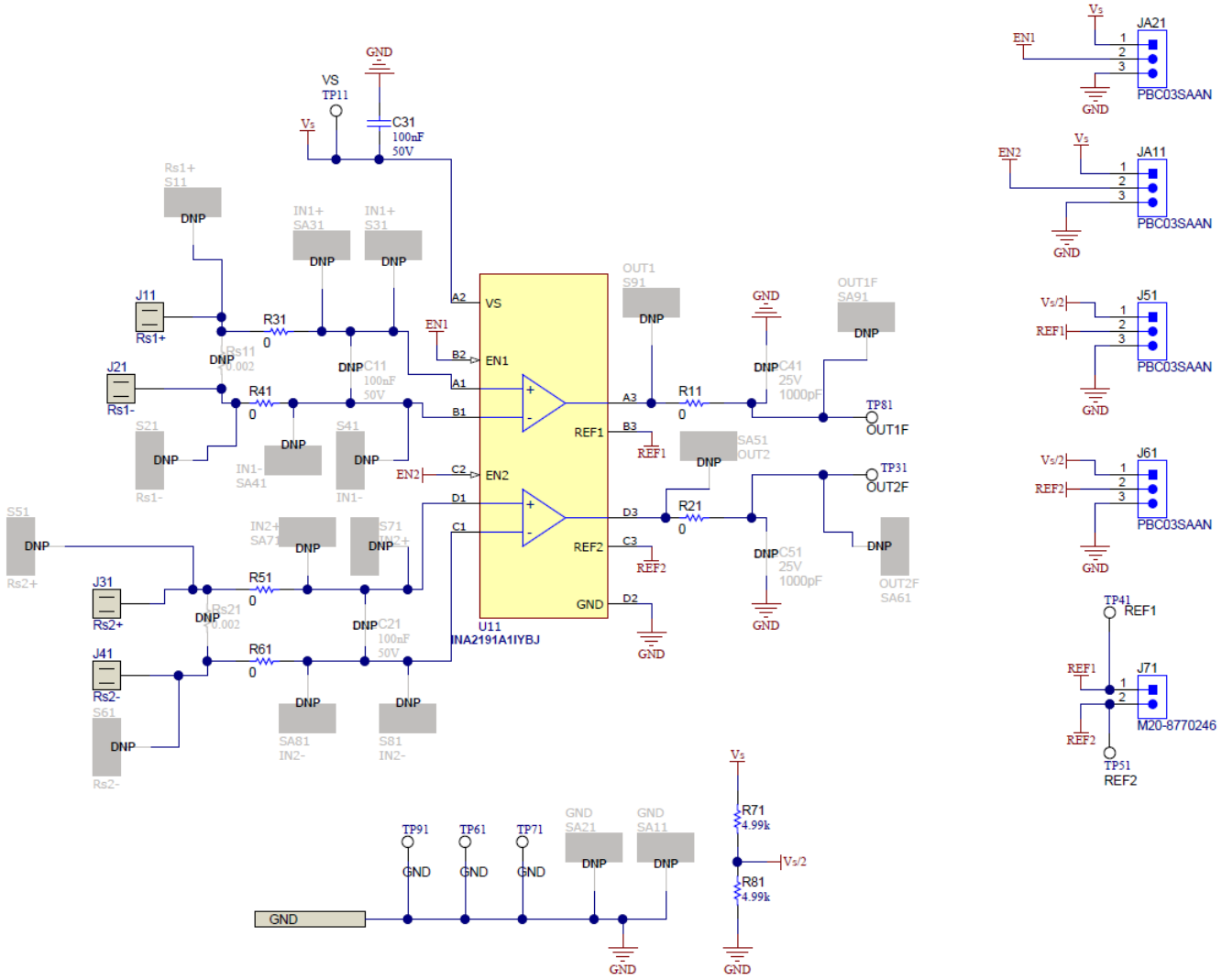

Figure 5-1. INA2191EVM Schematic: Gain A1 Panel

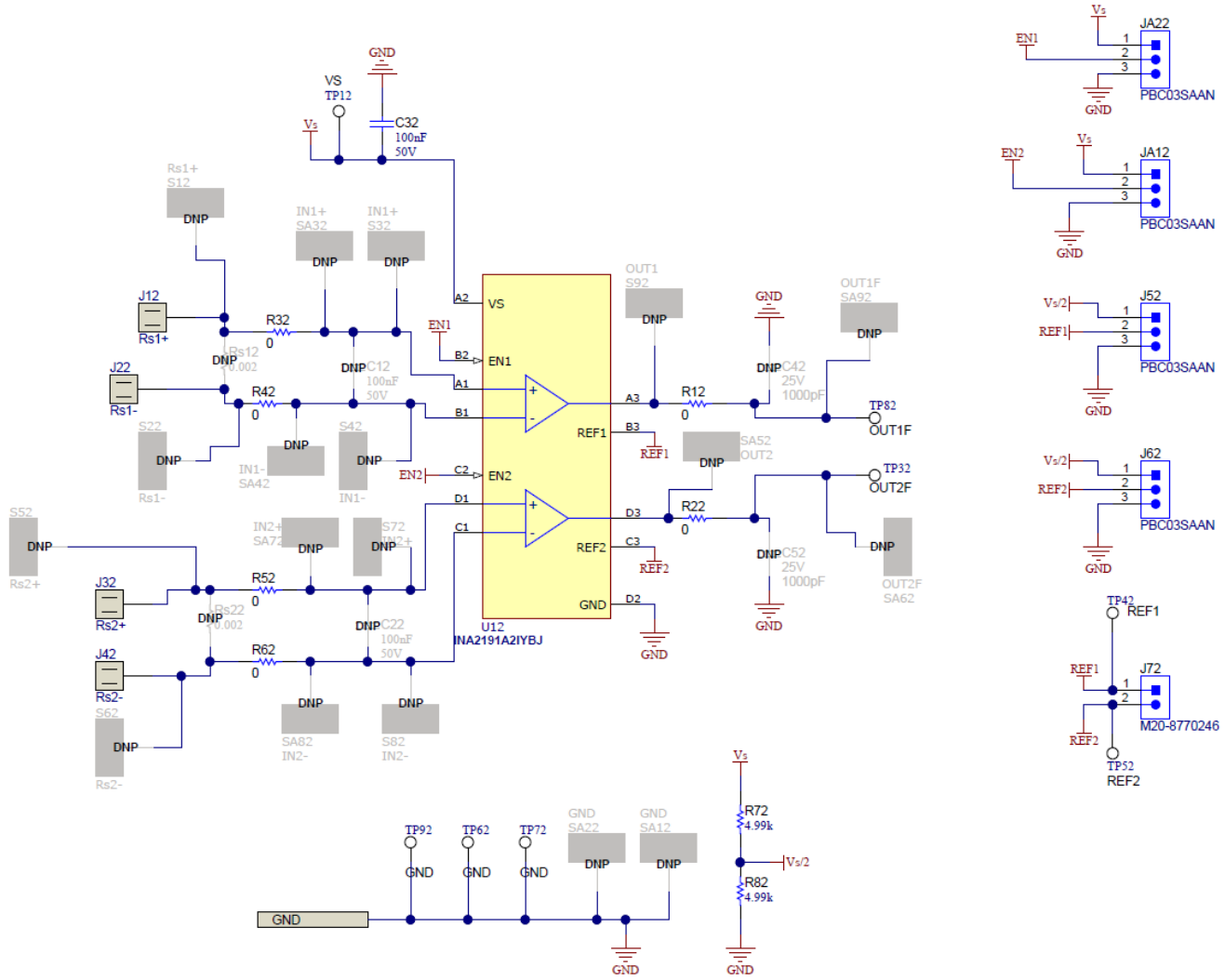

Figure 5-2. INA2191EVM Schematic: Gain A2 Panel

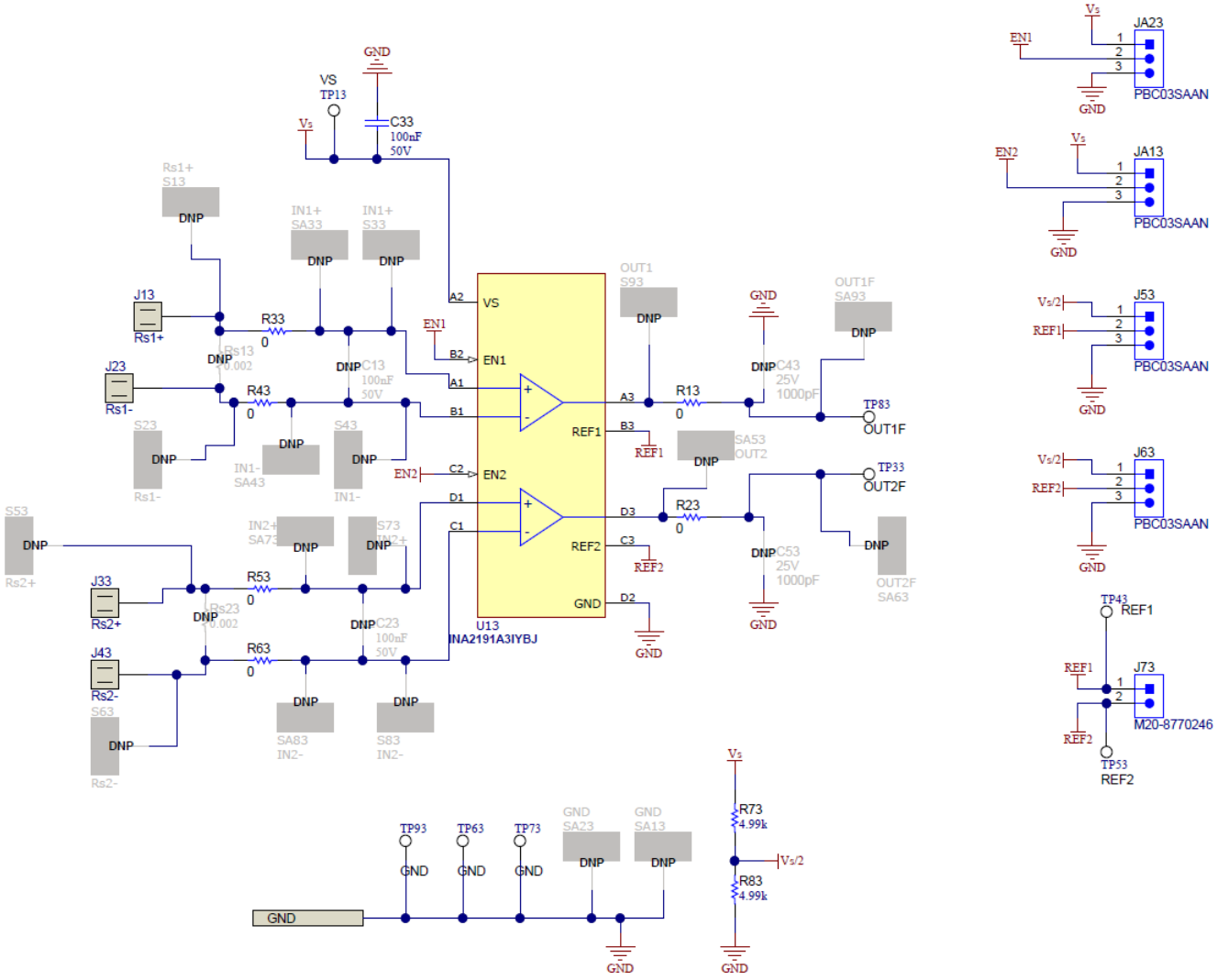

Figure 5-3. INA2191EVM Schematic: Gain A3 Panel

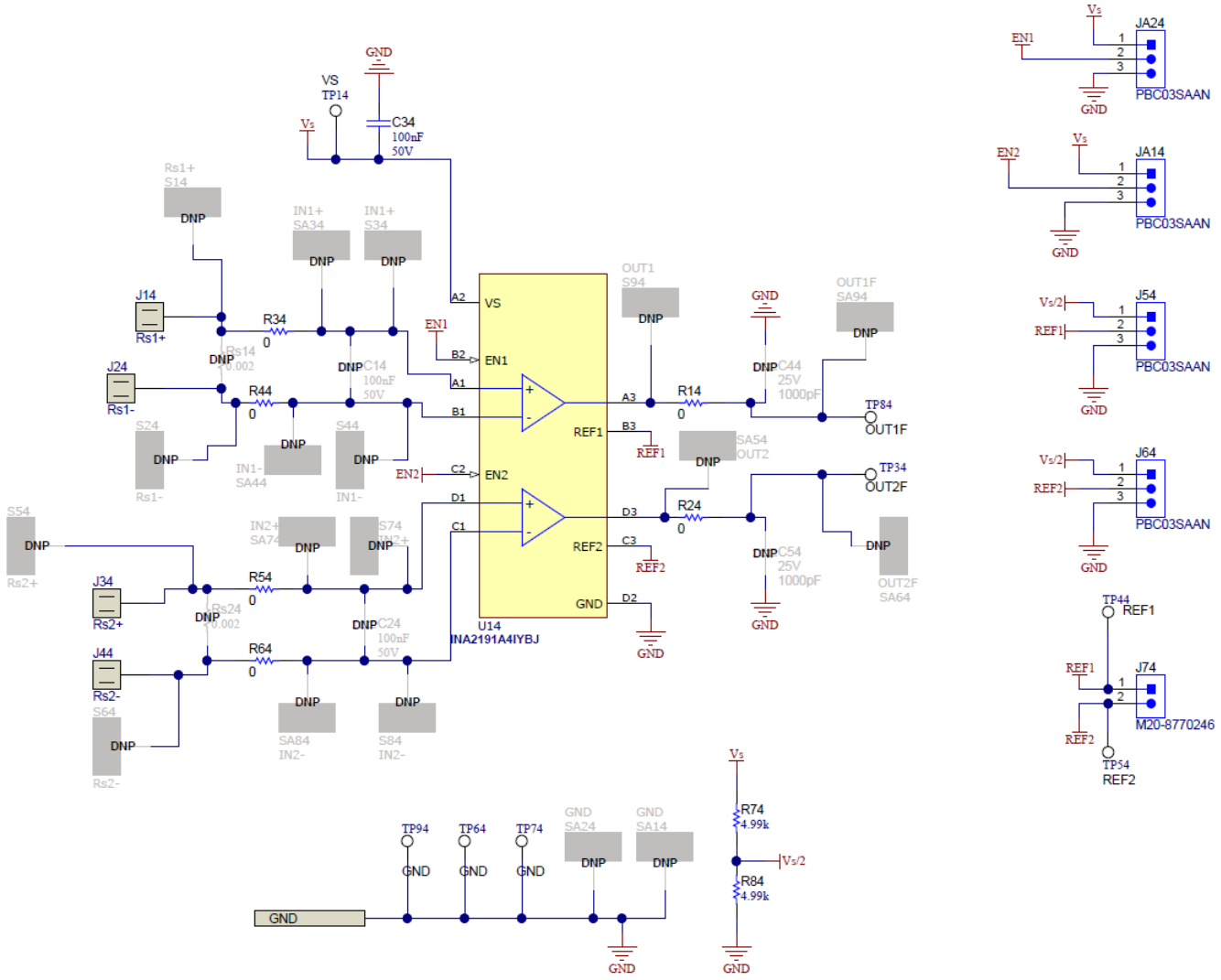

Figure 5-4. INA2191EVM Schematic: Gain A4 Panel

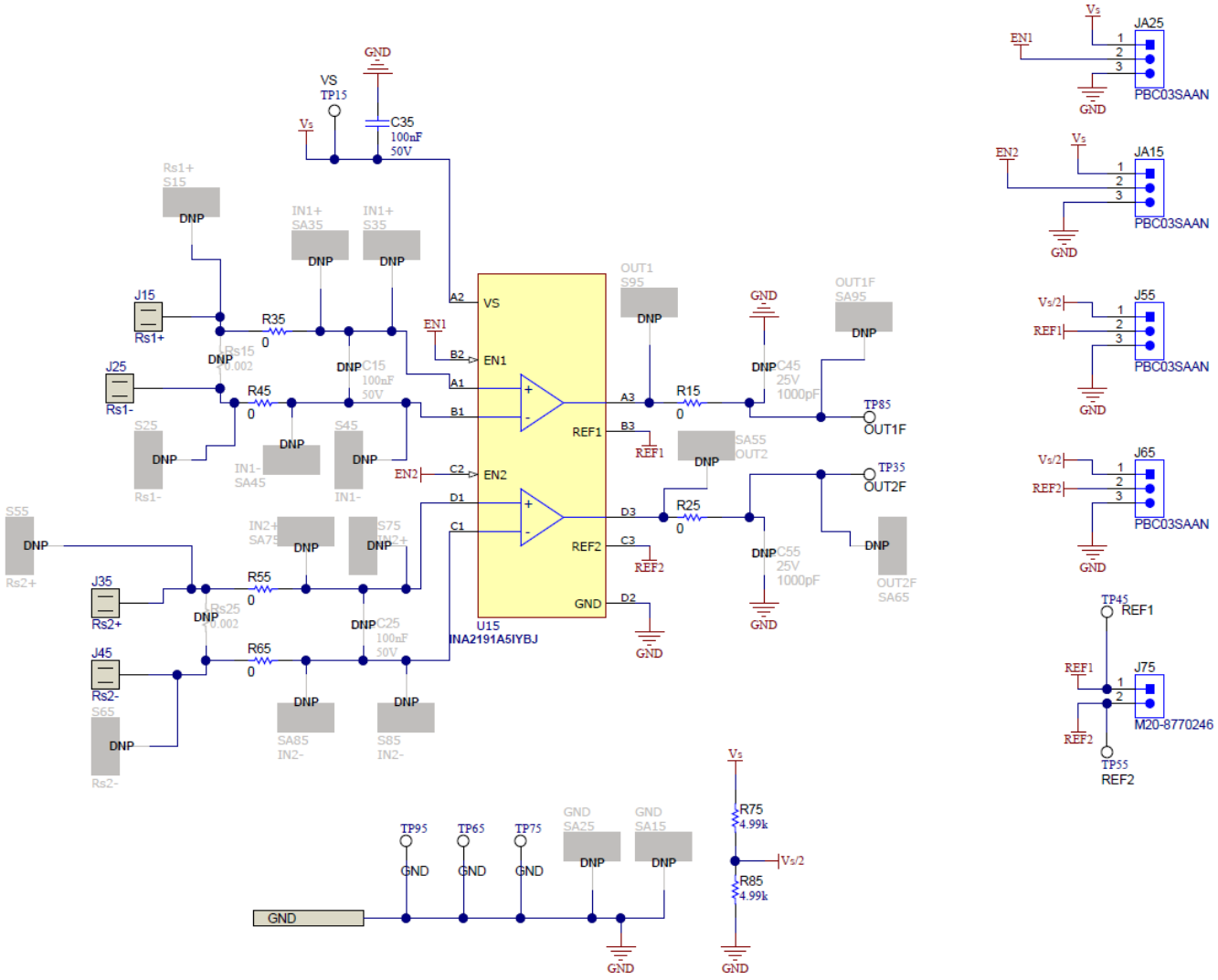

Figure 5-5. INA2191EVM Schematic: Gain A5 Panel

5.2 PCB Layout

Figure 5-6 through Figure 5-12 show the PCB layout for the INA2191EVM.

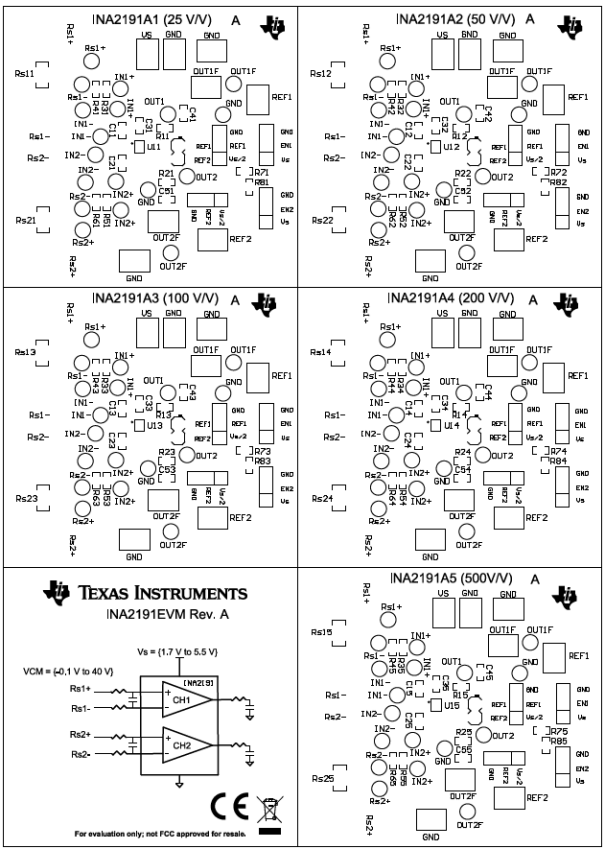

Figure 5-6. INA2191EVM Top Overlay

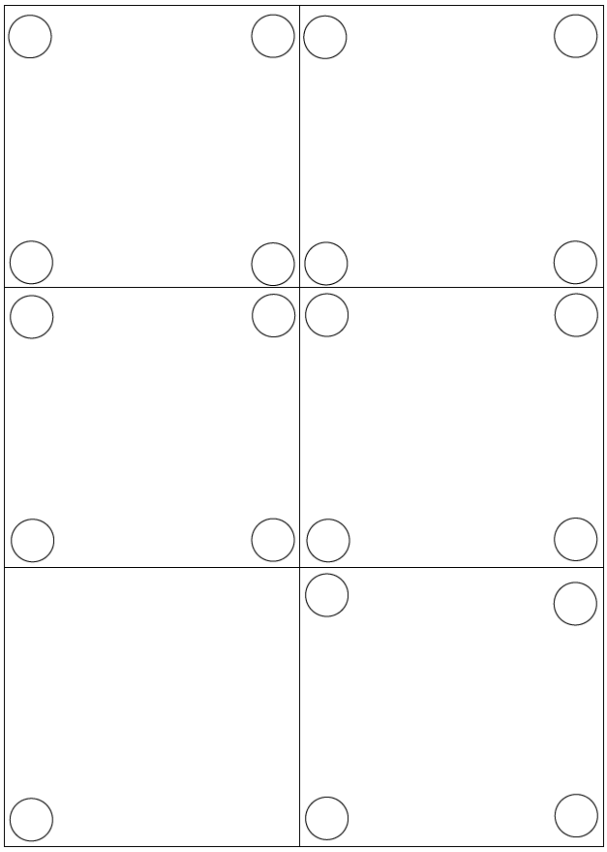

Figure 5-7. INA2191EVM Bottom Overlay

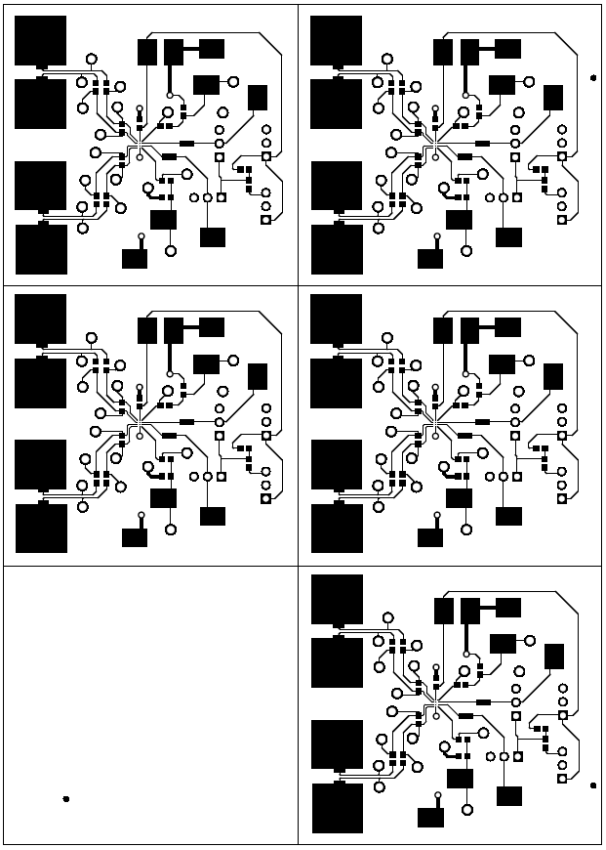

Figure 5-8. INA2191EVM Top Layer

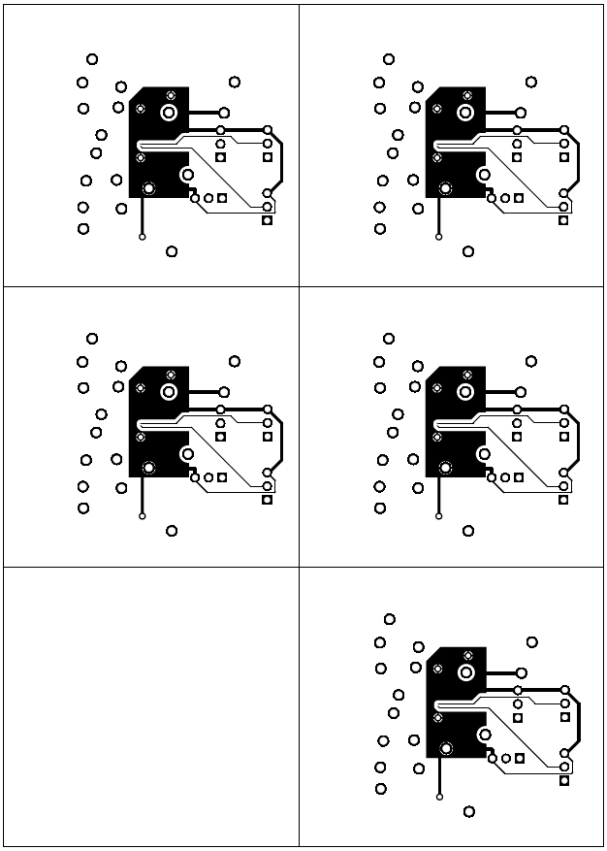

Figure 5-9. INA2191EVM Bottom Layer

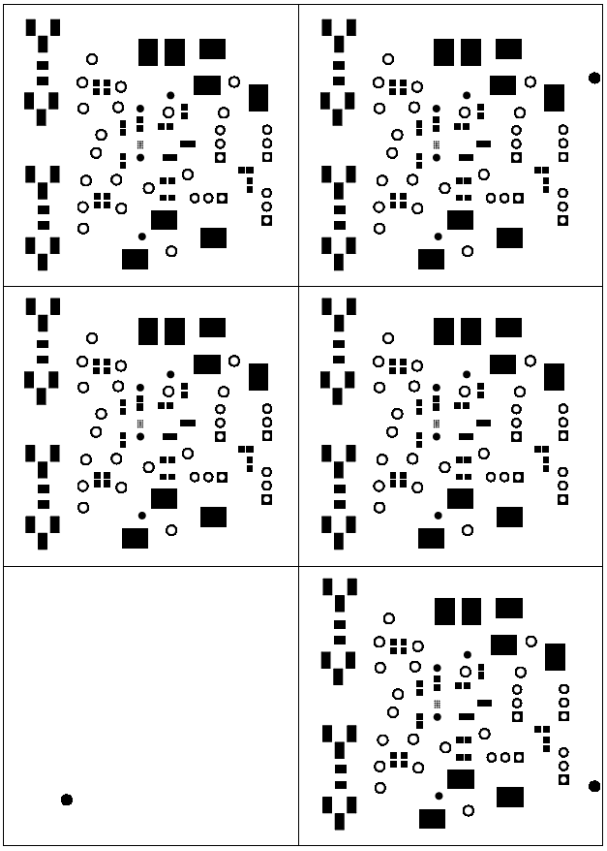

Figure 5-10. INA2191EVM Top Solder

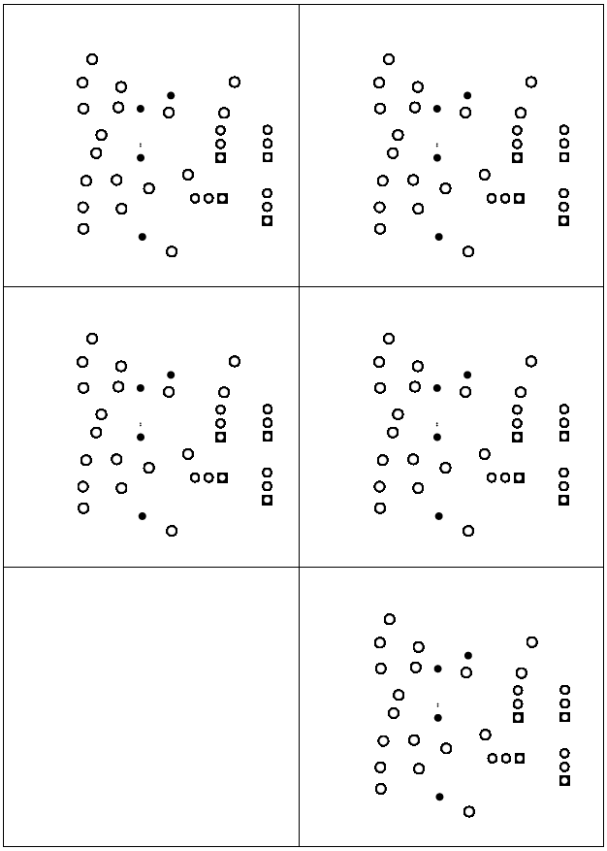

Figure 5-11. INA2191EVM Bottom Solder

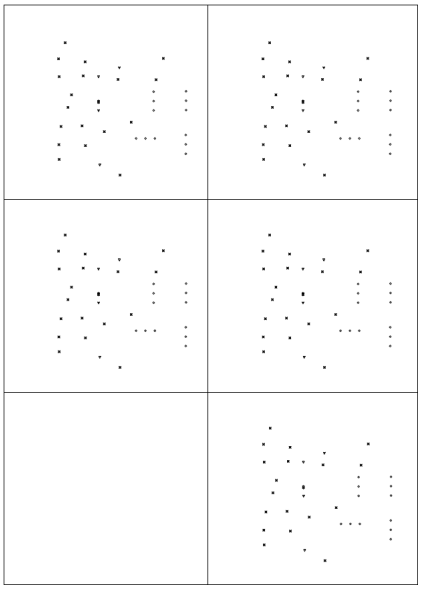

Figure 5-12. INA2191EVM Drill Drawing

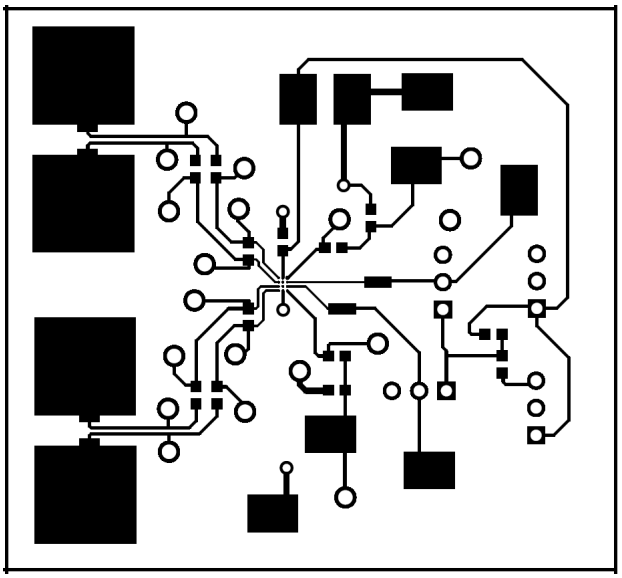

Figure 5-13. INA2191EVM Top Layer Single Panel

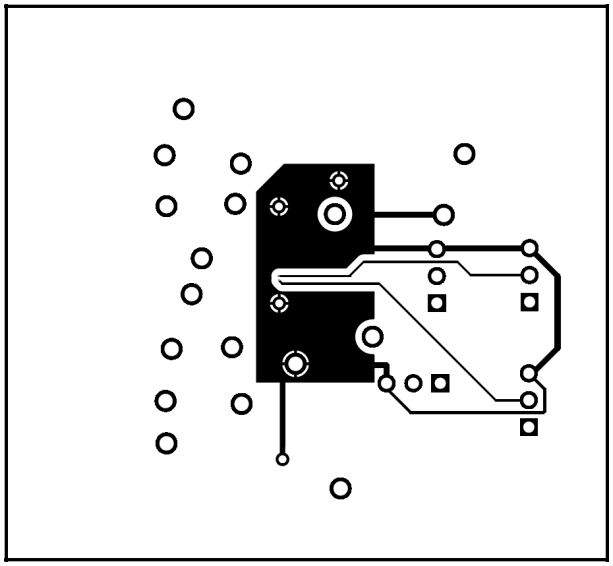

Figure 5-14. INA2191EVM Bottom Layer for Single Panel

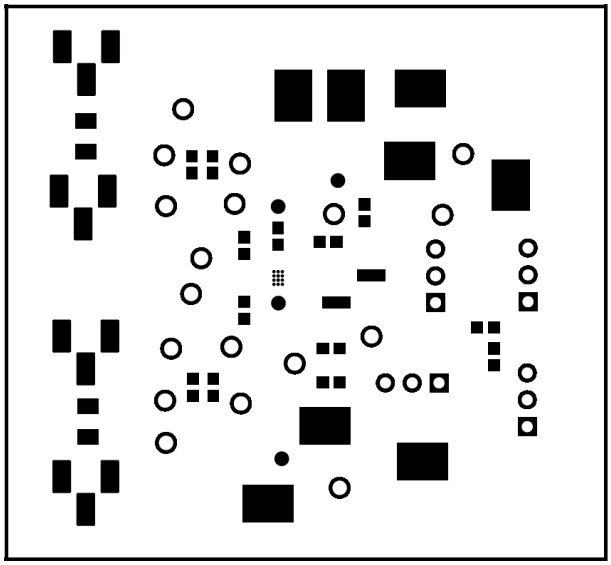

Figure 5-15. INA2191EVM Top Solder for Single Panel

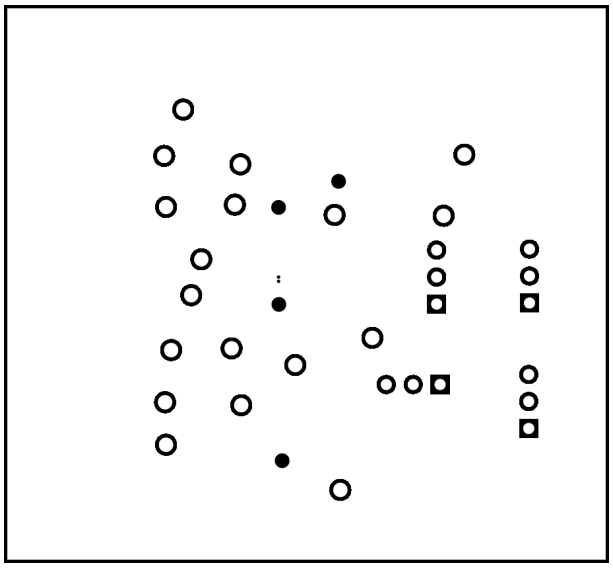

Figure 5-16. INA2191EVM Bottom Solder for Single Panel

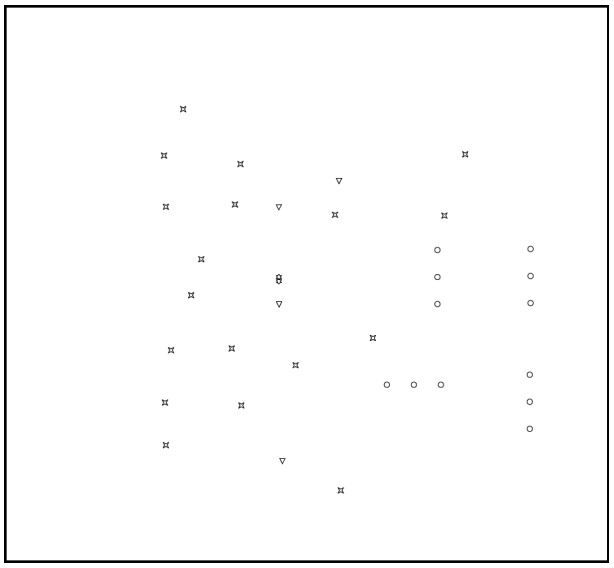

Figure 5-17. INA2191EVM Drill Drawing for Single Panel

5.3 Bill of Materials

Table 5-1 provides the parts list for the INA2191EVM.

Table 5-1. Bill of Materials

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
C31, C32, C33, C34, C35	5	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603	06035C104KAT2A	AVX
H1, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H19, H20, H21	21		Bumpon, Cylindrical, 0.312 X 0.200, Black	Black Bumpon	SJ61A1	3M
J11, J12, J13, J14, J15, J21, J22, J23, J24, J25, J31, J32, J33, J34, J35, J41, J42, J43, J44, J45	20		Quick-Fit 0.240 Tab	Quick-Fit 0.240 Tab	4928TR	Keystone
J51, J52, J53, J54, J55, J61, J62, J63, J64, J65, JA11, JA12, JA13, JA14, JA15, JA21, JA22, JA23, JA24, JA25	20		Header, 100mil, 3x1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
J71, J72, J73, J74, J75	5		Header, 2.54mm, 2x1, Tin, SMT	Header, 2.54mm, 2x1, SMT	M20-8770246	Harwin
R11, R12, R13, R14, R15, R21, R22, R23, R24, R25, R31, R32, R33, R34, R35, R41, R42, R43, R44, R45, R51, R52, R53, R54, R55, R61, R62, R63, R64, R65	30	0	RES, 0, 5%, 0.125 W, 0603	0603	MCT06030Z0000ZP500	Vishay/Beyschlag
R71, R72, R73, R74, R75, R81, R82, R83, R84, R85	10	4.99k	RES, 4.99 k, 1%, 0.1 W, 0603	0603	RC0603FR-074K99L	Yageo

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
TP11, TP12, TP13, TP14, TP15, TP31, TP32, TP33, TP34, TP35, TP41, TP42, TP43, TP44, TP45, TP51, TP52, TP53, TP54, TP55, TP61, TP62, TP63, TP64, TP65, TP71, TP72, TP73, TP74, TP75, TP81, TP82, TP83, TP84, TP85, TP91, TP92, TP93, TP94, TP95	40		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone
U11	1		Low-Power, Zero-Drift, Wide Dynamic Range, Precision Current-Sense Amplifier	DSBGA12	INA2191A1IYBJ	Texas Instruments
U12	1		Low-Power, Zero-Drift, Wide Dynamic Range, Precision Current-Sense Amplifier	DSBGA12	INA2191A2IYBJ	Texas Instruments
U13	1		Low-Power, Zero-Drift, Wide Dynamic Range, Precision Current-Sense Amplifier	DSBGA12	INA2191A3IYBJ	Texas Instruments
U14	1		Low-Power, Zero-Drift, Wide Dynamic Range, Precision Current-Sense Amplifier	DSBGA12	INA2191A4IYBJ	Texas Instruments
U15	1		Low-Power, Zero-Drift, Wide Dynamic Range, Precision Current-Sense Amplifier	DSBGA12	INA2191A5IYBJ	Texas Instruments
C11, C12, C13, C14, C15, C21, C22, C23, C24, C25	0	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603	06035C104KAT2A	AVX
C41, C42, C43, C44, C45, C51, C52, C53, C54, C55	0	1000pF	CAP, CERM, 1000 pF, 25 V, +/- 10%, C0G/NP0, 0603	0603	C0603C102K3GACTU	Kemet

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
Rs11, Rs12, Rs13, Rs14, Rs15, Rs21, Rs22, Rs23, Rs24, Rs25	0	0.002	RES, 0.002, 1%, 1 W, 1206	1206	CSNL1206FT2L00	Stackpole Electronics Inc
S11, S12, S13, S14, S15, S21, S22, S23, S24, S25, S31, S32, S33, S34, S35, S41, S42, S43, S44, S45, S51, S52, S53, S54, S55, S61, S62, S63, S64, S65, S71, S72, S73, S74, S75, S81, S82, S83, S84, S85, S91, S92, S93, S94, S95, SA11, SA12, SA13, SA14, SA15, SA21, SA22, SA23, SA24, SA25, SA31, SA32, SA33, SA34, SA35, SA41, SA42, SA43, SA44, SA45, SA51, SA52, SA53, SA54, SA55, SA61, SA62, SA63, SA64, SA65, SA71, SA72, SA73, SA74, SA75, SA81, SA82, SA83, SA84, SA85, SA91, SA92, SA93, SA94, SA95	0		CONN PIN RCPT .018-.021 SOLDER	PIN_RCPT	3-331272-8	TE Connectivity
SH1, SH2, SH3, SH4, SH5, SH6, SH7, SH8, SH9, SH10, SH11, SH12, SH13, SH14, SH15, SH16, SH17, SH18, SH19, SH20	0	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2021) to Revision A (June 2021)	Page
• Removed preview notice for the INA2191	3

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265