Application Report
SBVA061–March 2020

Programmable Push-Button, Pulse Detector, and Pulse Generator Solutions

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ABSTRACT

This application note describes how to create a programmable push-button, pulse detector, and pulse generator using the voltage supervisor family: TPS3895, TPS3896, TPS3897, and TPS3898. This application note also covers the fixed delay push-button options: TPS3420, TPS3421, and TPS3422. Lastly, this application note provides alternative wide Vin, low-power with TPS3840 and low-cost with TLV840 device alternatives to accomplish programmable push-button functionality. Push-button functionality is useful in many personal electronics or space constrained applications in which there are a limited number of buttons so the timing of how long the button is held or released is used to create different actions in the system. Other industrial applications use push-buttons to force a system restart but use specific timing to prevent accidental restarts or to allow certain actions to occur before the system shuts down such as enabling or disabling a device for a certain period of time before shutting down. Another use case is using a certain duration pulse to disable a subsystem upon power up before starting the entire system. Pulse detector and pulse generator functionality is useful in applications that require error checking or verifying a specific sequence of power levels for a certain duration of time have occurred. This application note is not limited to specific end equipments but can be applied to any application that requires push-buttons, pulse detectors, or pulse generators.

Contents

List of Figures

List of Tables

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1 Introduction

This application note discusses the fixed timing push-button devices offered by TI and also how to create programmable push-buttons, pulse detectors, and pulse generators. The integrated TI solutions provided in this application note are then compared to the discrete implementation using logic devices with resistors and capacitors.

2 Fixed Timing Push-Button Devices: TPS3420, TPS3421, TPS3422

These devices are nano power (250 nA typical), small SON package (1.45 mm x 1 mm), fixed timing push-button devices.

TPS3420 requires both push-button inputs (PB1, PB2) to be pressed logic low for t_{timer} = 7.5 or 12.5 seconds before the active-low reset output ($\overline{RST}$) asserts to logic low until either of the push-button inputs are released. For TPS3420 only, t_{timer} can be set to 7.5 seconds by connecting TS to GND or 12.5 seconds by connecting TS to VCC.

TPS3421 requires both push-button inputs (PB1, PB2) to be pressed logic low for t_{timer} = 7.5 seconds before the active-low reset output ($\overline{RST}$) asserts to logic low for a fixed t_{rst} = 400 ms or 80 ms. For TPS3421 only, the tRST can be set to 400 ms by choosing the TPS3421x**G** variant, or set to 80 ms by choosing the TPS3421x**C** variant.

TPS3422 requires the single push-button input (PB1) to be pressed logic low for t_{timer} = 7.5 seconds before the active-low reset output ($\overline{RST}$) asserts to logic low for a fixed t_{rst} = 400 ms.

The functionality of these devices are summarized by the timing diagrams shown in Figure 1, Figure 2, and Figure 3.

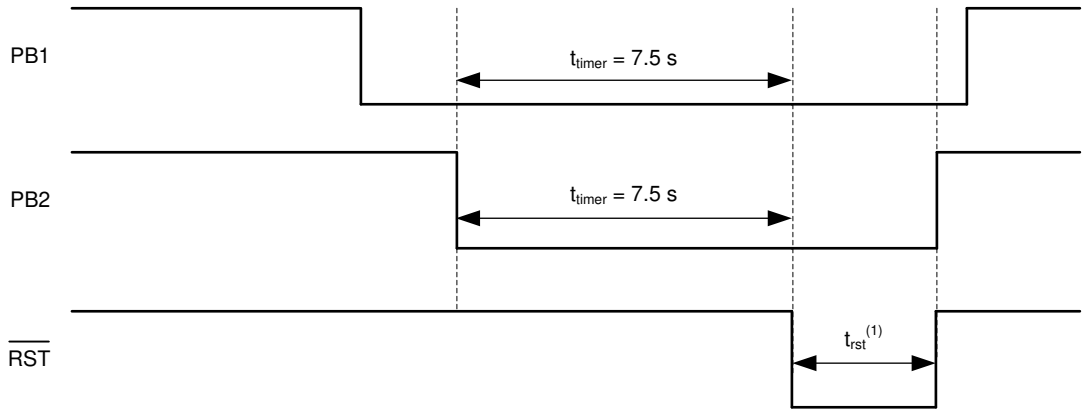

Figure 1. TPS3420 Timing Diagram (t_{timer} Selectable: 7.5 seconds or 12.5 seconds)

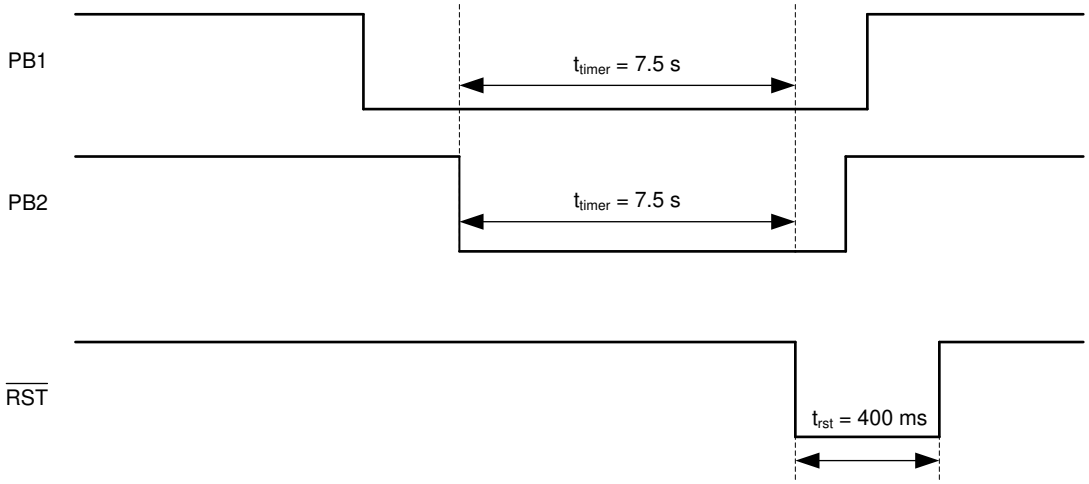

Figure 2. TPS3421 Timing Diagram (t_{rst} Selectable: 400 ms or 80 ms)

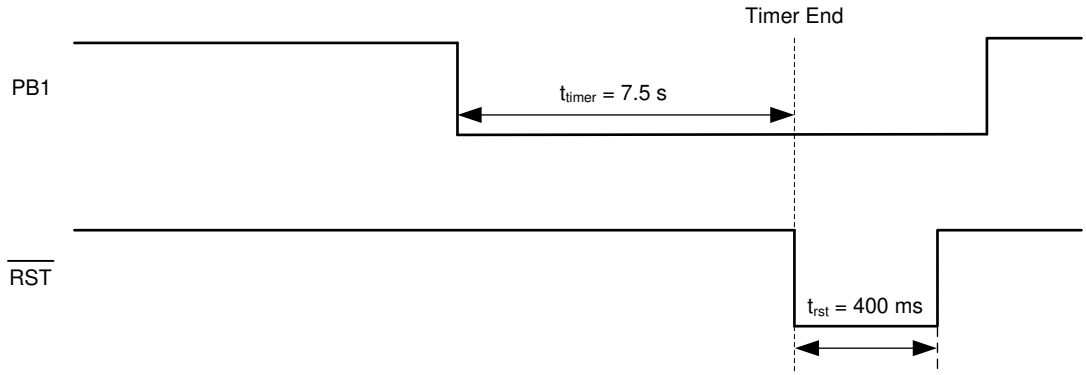

Figure 3. TPS3422 Timing Diagram

3 Programmable Push-Button: TPS3895A, TPS3896A, TPS3897A, TPS3898A

The TPS389x family of devices are low power (6 µA), small USON package (1.45 mm x 1 mm), programmable delay voltage supervisors that monitor an analog input voltage and include an enable digital input. To create a programmable push-button, the sense pin that monitors an analog voltage is not used so can be tied to VCC. Only the enable pin as a digitial input is used to create the programmable push-button. The TPS389x**A** variant of the device is required for creating the programmable push-button because only the TPS389x**A** variant has programmable delay on the enable pin.

The programmable delay is set by the capacitor on the CT pin. By leaving CT pin floating, the delay defaults to the minimum value of 40 µs. See Equation 1 programmable delay equation. Note $t_{pd(r)}$ is in units of seconds and C_{CT} is in units of µF.

$$t_{pd(r)}\ [s] = (C_{CT}\ [\mu F] * 4) + 40\ \mu s \quad (1)$$

TPS3895A has an active-high ENABLE and active-high, push-pull OUTPUT. This device requires the ENABLE pin to be asserted logic high for programmable time delay ($t_{d(A)}$) before the OUTPUT asserts to logic high.

TPS3896A has an active-low $\overline{\text{ENABLE}}$ and active-low, push-pull $\overline{\text{OUTPUT}}$. This device requires the $\overline{\text{ENABLE}}$ pin to be asserted logic low for programmable time delay ($t_{d(A)}$) before the $\overline{\text{OUTPUT}}$ asserts to logic low.

TPS3897A has an active-high ENABLE and active-high, open-drain OUTPUT. This device requires the ENABLE pin to be asserted logic high for programmable time delay ($t_{d(A)}$) before the OUTPUT asserts to logic high. A pull-up resistor is required for the open-drain output of this device.

TPS3898A has an active-low $\overline{\text{ENABLE}}$ and active-low, open-drain $\overline{\text{OUTPUT}}$. This device requires the $\overline{\text{ENABLE}}$ pin to be asserted logic low for programmable time delay ($t_{d(A)}$) before the $\overline{\text{OUTPUT}}$ asserts to logic low. A pull-up resistor is required for the open-drain output of this device.

The functionality of these devices are summarized by the timing diagrams shown in Figure 4 and Figure 5.

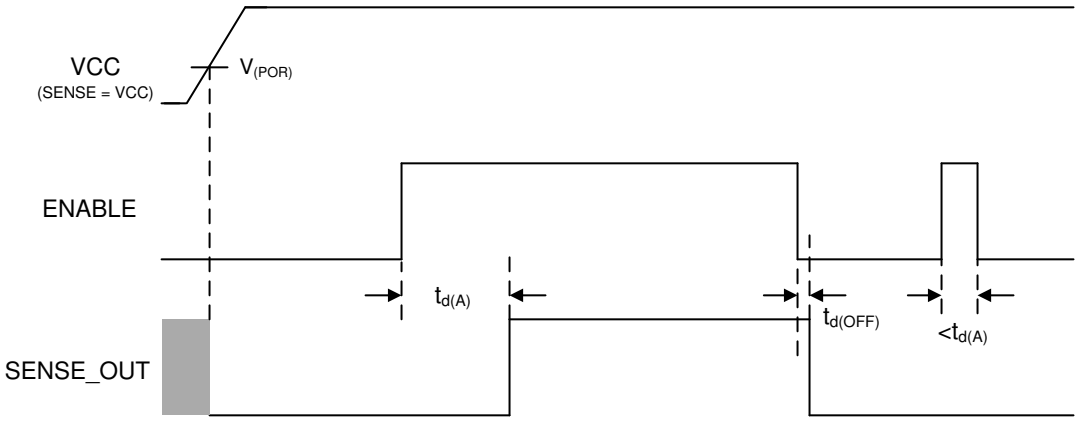

Figure 4. TPS3895A and TPS3897A Timing Diagram

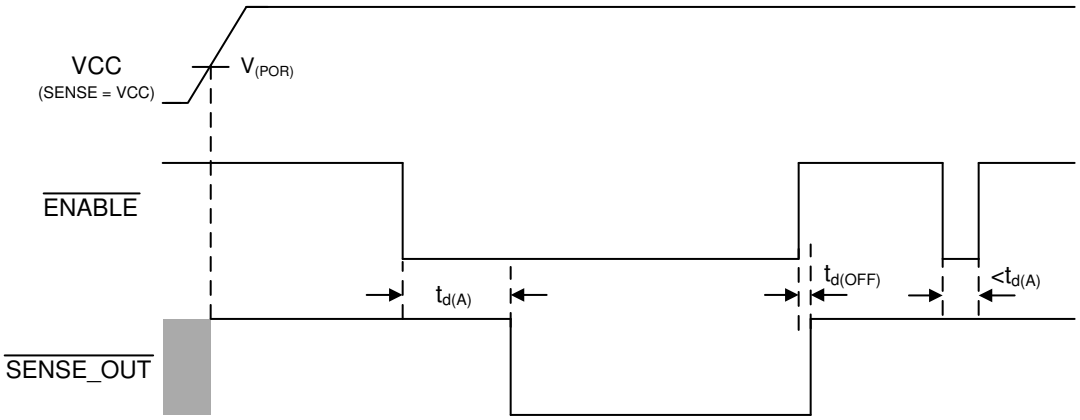

Figure 5. TPS3896A and TPS3898A Timing Diagram

4 Programmable Push-Button with Programmable Reset Delay

Some applications not only require a delay after the push-button is pressed, as shown in the previous section, but also requires the output to remain asserted for a certain duration of time before deasserting. This is similar to the functionality of TPS3422 shown inFigure 3 except both the push-button delay and the reset delay are both programmable. This section uses two TPS389x devices together to create a programmable push-button similar to the previous section but also with a programmable reset delay set by the other TPS389x device. Figure 6 shows the simulation circuit of this application using TPS3898A to set the programmable push-button with C2 and TPS3897A to set the programmable reset delay with C1. Note that for this application, the open-drain devices (TPS3897, TPS3898) or the push-pull devices (TPS3895, TPS3896) can be used as long as both devices used have oppositive output polarity. In this application, TPS3898 (or TPS3896) uses C2 to program the length of time before the output asserts to logic low after the sense input rises above the voltage threshold which is the eqivalent of the button being pressed. Then TPS3897 (or TPS3895) uses C1 to set the time the output asserts for before disabling the other device causing the output to deassert back to logic high.

NOTE: The programmable reset delay set by C1 must be a larger value than the push-button delay set by C2 because C1 must include the delay of C2. For example, if C1 = 1 nF and C2 = 1 nF, the output never asserts. If C1 = 10 nF and C2 = 5 nF, the push-button delay and the reset delay will be equal since the push-button delay results from C2 = 5 nF and the reset delay results from C1 - C2 = 5 nF

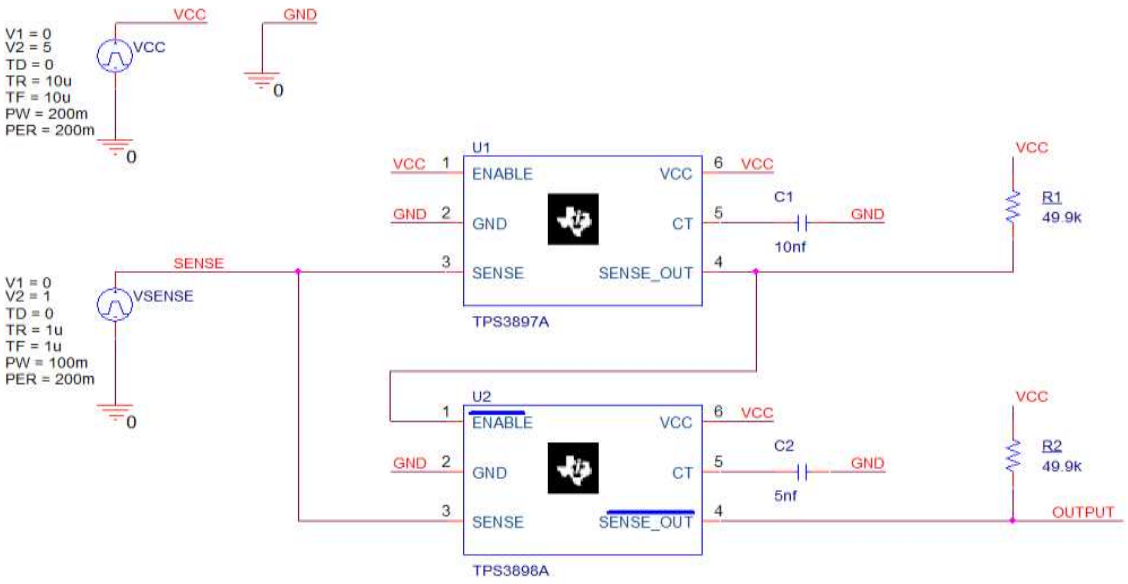

Figure 6. Programmable Push-Button With Programmable Reset Delay Simulation Circuit

The programmable push-button delay follows Equation 1. The programmable reset delay is calculated from the differece between C1 and C2 as shown in Equation 2.

Programmable Reset Delay [s] = ((C_{CT1} [µF] - C_{CT2} [µF])* 4) + 40 µs (2)

Figure 7 shows the simulation results when C2 = 5 nF and C1 = 10 nF. The programmable push-button delay ~20 ms from Equation 1 and the reset delay is also ~20 ms because C1 - C1 = 5 nF.

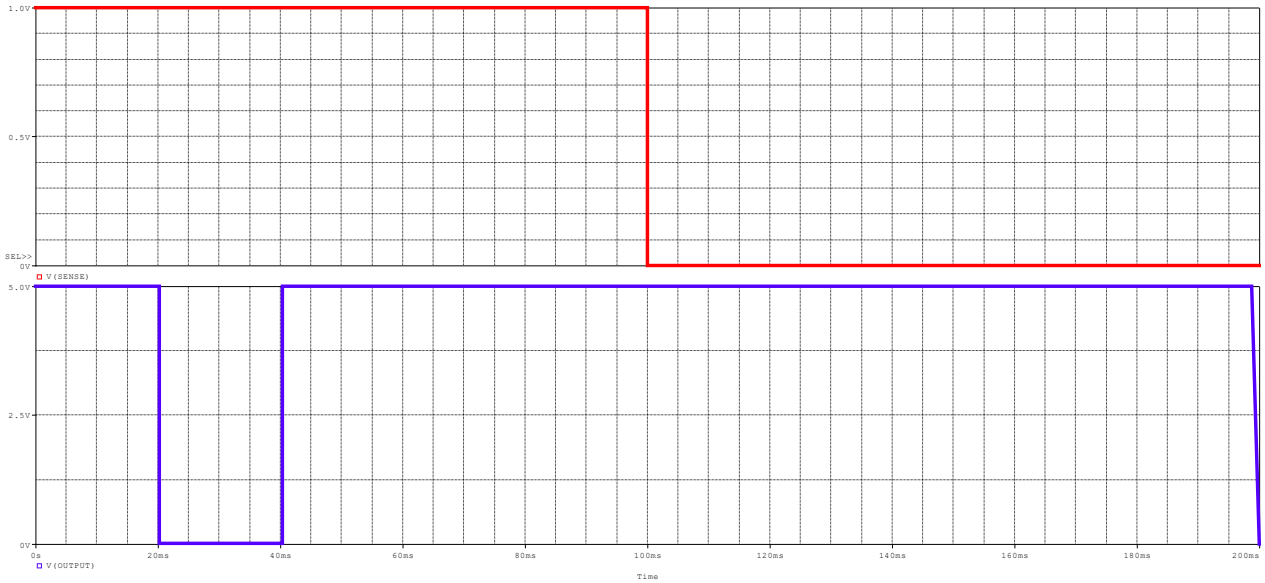

Figure 7. Programmable Push-Button (C2 = 5 nF) with Programmable Reset Delay (C1 = 10 nF) Simulation Results

Figure 8 shows the simulation results when C2 = 10 nF and C1 = 11 nF. The programmable push-button delay ~40 ms from Equation 1 and the reset delay is also ~4 ms because C1 - C1 = 1 nF.

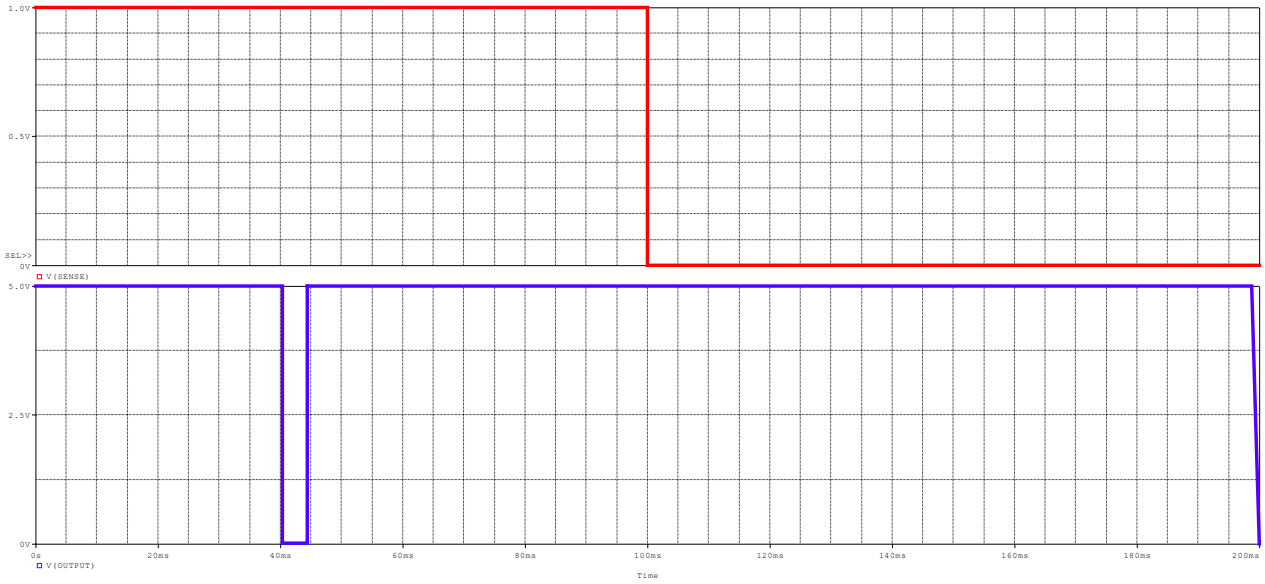

Figure 8. Programmable Push-Button (C2 = 10 nF) with Programmable Reset Delay (C1 = 11 nF) Simulation Results

5 Programmable Pulse Detector

In this section, the TPS389xA family of devices are used to create a circuit that monitors an analog signal and when the input signal rises above a defined threshold for a programmable amount of time, the output asserts and immediately returns to inactive regardless of the monitored voltage. Any of the TPS389xA devices will work for this application and the choice depends on the output polarity (active-low, active-high) and output topology (push-pull, open-drain) required for the application. This application uses the sense pin for monitoring and the enable pin for returning the device back to inactive state. The programmable pulse detector circuit consists of a TPS389xA device, a capacitor to set the delay, and an inverter with active-high enable. The open-drain devices, TPS3897A and TPS3898A also require a pull-up resistor at the output.

The programmable pulse detector circuits are shown in Figure 9 and Figure 10.

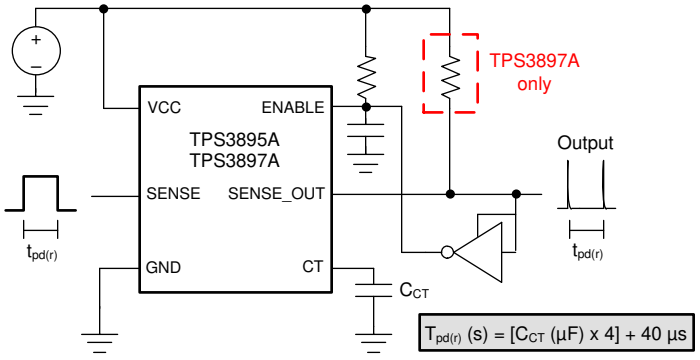

Figure 9. Active-High Programmable Pulse Detector Using TPS3895A or TPS3897A

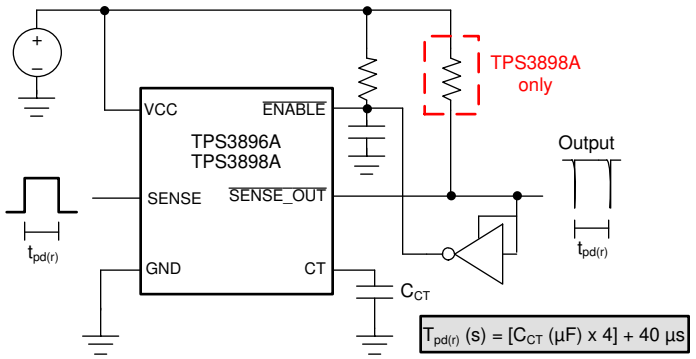

Figure 10. Active-Low Programmable Pulse Detector Using TPS3896A or TPS3898A

The only difference between Figure 9 and Figure 10 is the output polarity. Figure 9 is simulated in PSpice using Figure 11 and Figure 10 are simulated using Figure 13. The simulations use the push-pull variants (TPS3895A and TPS3896A) thus no pull-up resistor is required on the sense output. Note that the circuits are the same with the only difference being the device. The programmable pulse detect delay ($t_{pd(r)}$) using Equation 1 is set for ~20 ms using C_{CT} = 5 nF. This means that if SENSE is above the V_{IT+} threshold of the device for 20 ms, the sense output asserts active then immediately asserts inactive regardless of the sense voltage. For simulation results for this application, refer to Figure 12 for TPS3895A pulse detector and Figure 14 for TPS3896A pulse detector.

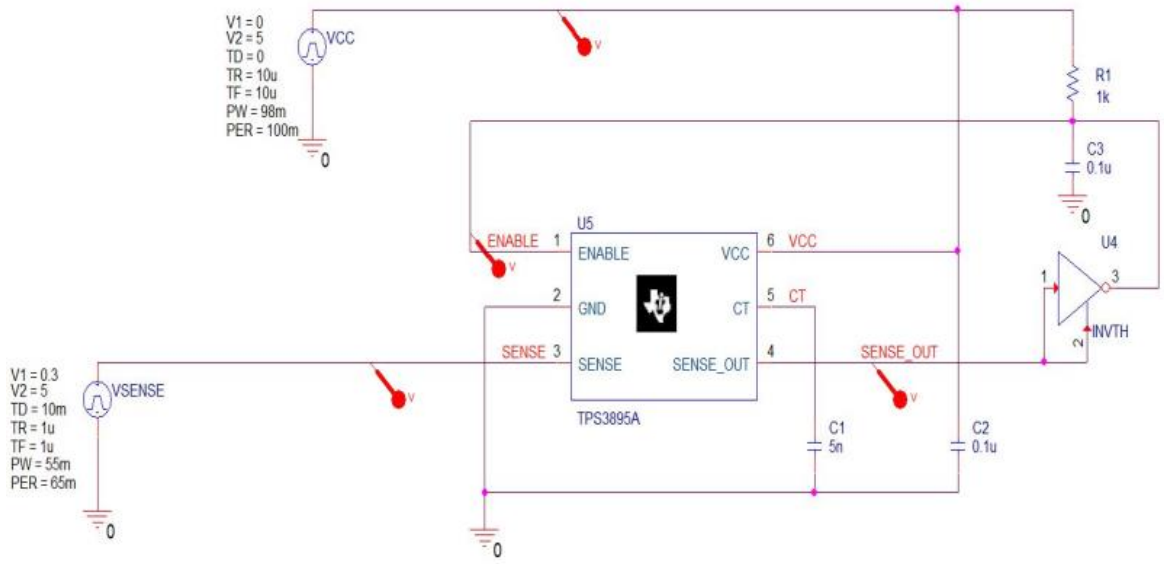

Figure 11. TPS3895A Programmable Pulse Detector Simulation Circuit

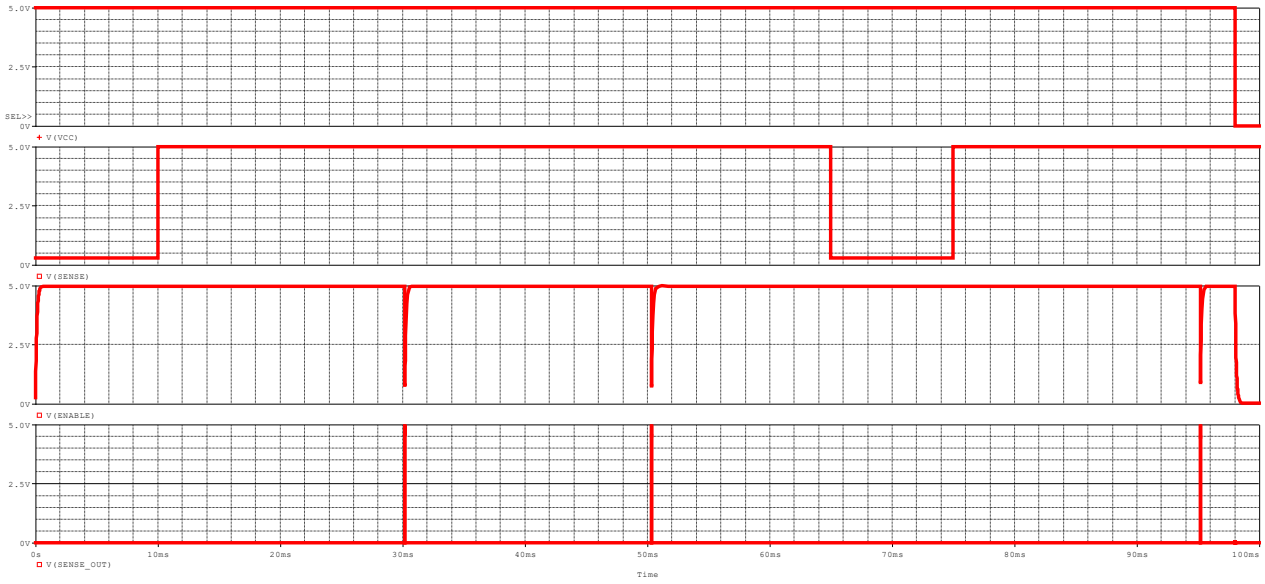

Figure 12. TPS3895A Programmable Pulse Detector Simulation Results

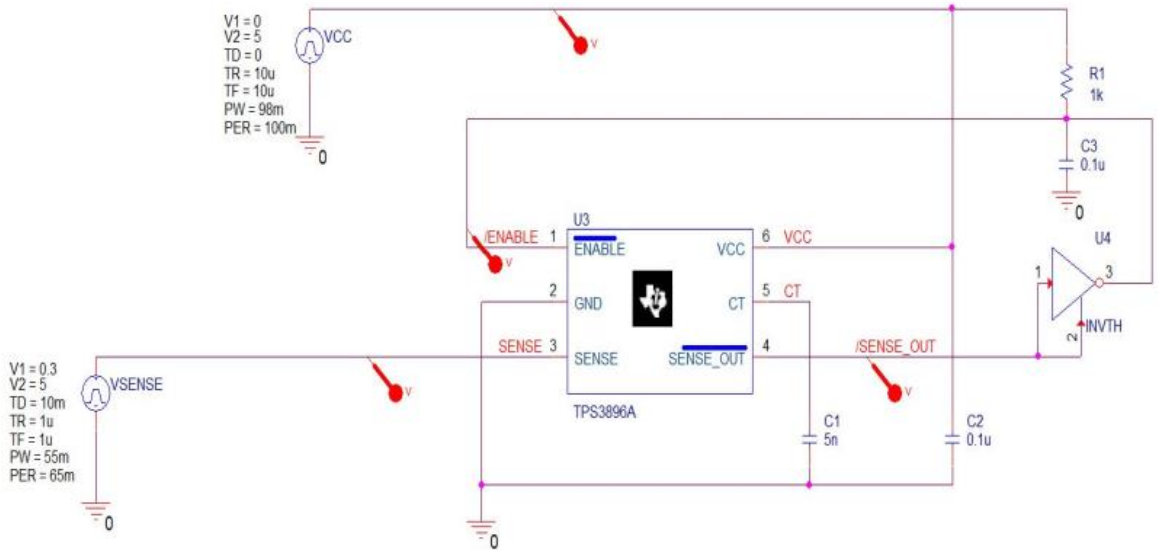

Figure 13. TPS3896A Programmable Pulse Detector Simulation Circuit

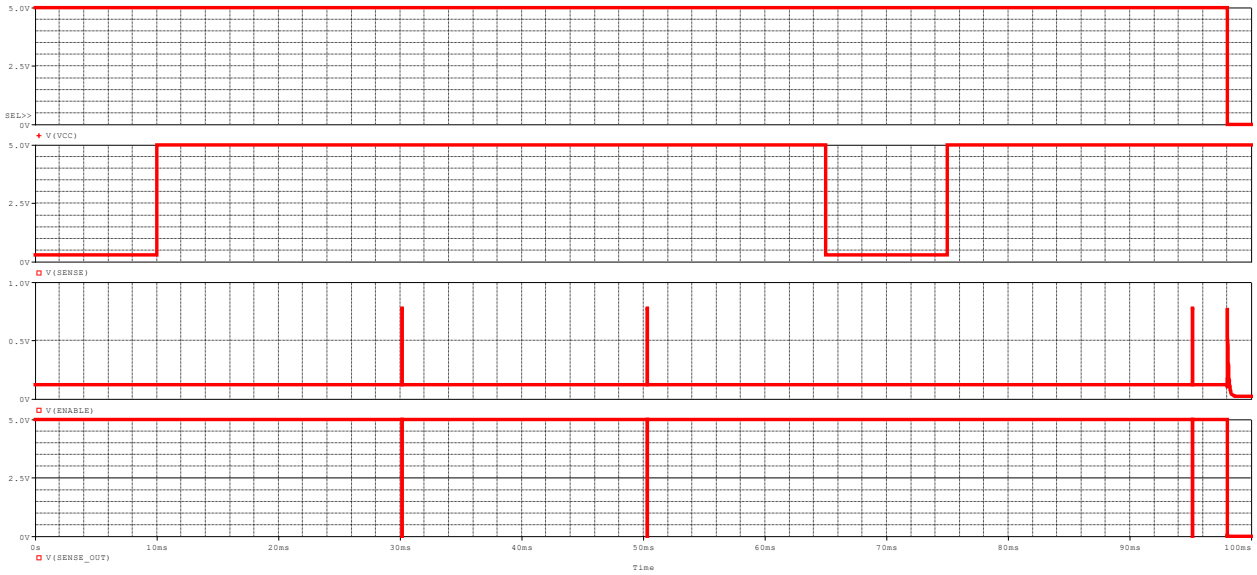

Figure 14. TPS3896A Programmable Pulse Detector Simulation Results

6 Programmable Pulse Generator

In this section, a programmable pulse generator is created using two TPS389x devices. Similar to the programmable pulse detector, the detection timing is programmable but the programmable pulse generator also allows programming the pulse width in addition. This circuit is useful in applications that require a specific pulse width signal for performing a special task such as enabling or disabling a subsystem for a certain amount of time. This circuit can also create a programmled timing pulse before returning back to default state to be used for initialization or timing dependent start up conditions.

The programmable pulse generator circuit requires a TPS3897 and TPS3898. The "A" variant and "P" variant with both work for this application because the enable delay is not being used. If the application requires adding extra functionality to utlize the enable delay, use the "A" variant. The TPS3897 creates the initial "wait" delay before the output asserts to logic high by selecting the capacitor value connected to the CT pin on TPS3897. The TPS3898 creates the pulse width delay that the output remains asserted logic high for by selecting the capacitor value connected to the CT pin on TPS3898. The open-drain devices are chosen so the outputs of each device can be tied directly together with a single pull-up resistor.

Figure 15 shows the programmable pulse button circuit used for simulation. The initial "wait" delay is set by C1 and the pulse width delay is set by C2 - C1. The delays are described by Equation 3 and Equation 4.

Wait Delay [s] = (C_{CT1} [µF] * 4) + 40 µs (3)

Pulse Width Delay [s] = ((C_{CT2} [µF] - C_{CT1} [µF])* 4) + 40 µs (4)

NOTE: The pulse width is set by subtracting the C2 value from C1 because the C2 delay must also account for the delay set by C1. For example, if C1 = 1 nF and C2 = 1 nF, there is no pulse. If C1 = 1 nF and C2 = 2 nF, the pulse width is equal to the initial wait delay because C1 = 1 uF and C2 - C1 = 1 uF.

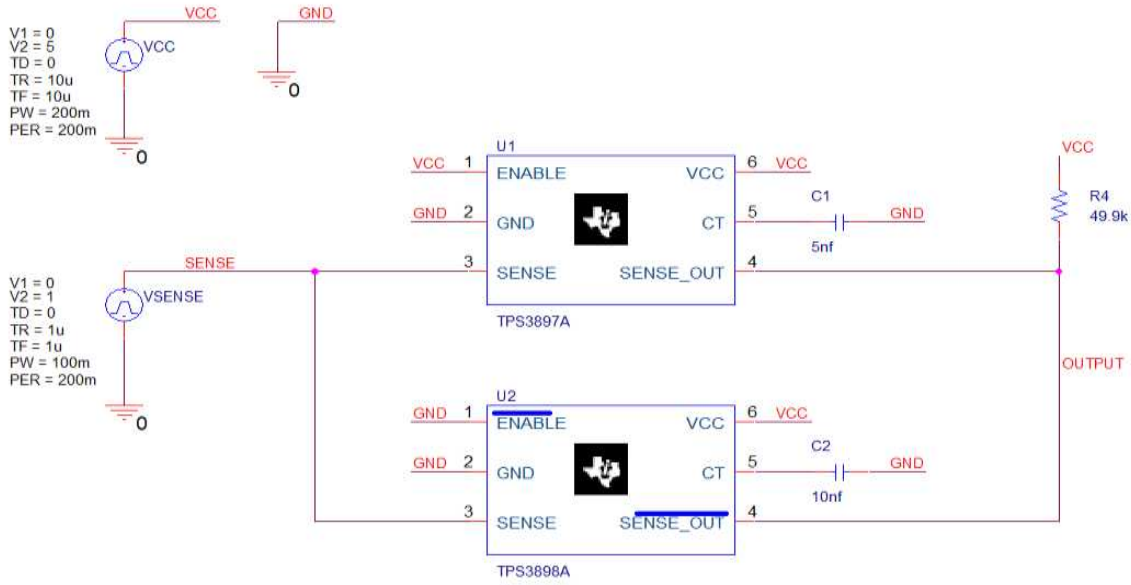

Figure 15. Programmable Pulse Generator Using TPS3897 and TPS3898

The programmable pulse generator functionality is shown by simulating Figure 15. The results are shown in Figure 16, Figure 17, and Figure 18.

Figure 16 shows the simulation results with CT1 = 5 µF and CT2 = 10 µF. Using Equation 3, the wait delay ~20 ms and using Equation 4, the pulse width delay is also ~20 ms. Since the CT1 value and the difference between CT2 and CT1 are the same value, the initial wait delay is equal to the pulse width delay.

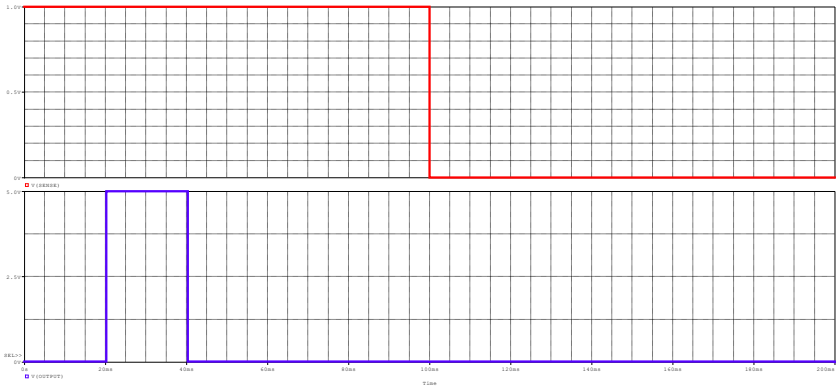

Figure 16. Programmable Pulse Generator Simulation with CT1 = 5µF and CT2 = 10µF

Figure 17 shows the simulation results with CT1 = 5 µF and CT2 = 15 µF. Since the difference between CT2 and CT1 has doubled, the pulse width delay is twice as long. The initial wait delay remains unchanged.

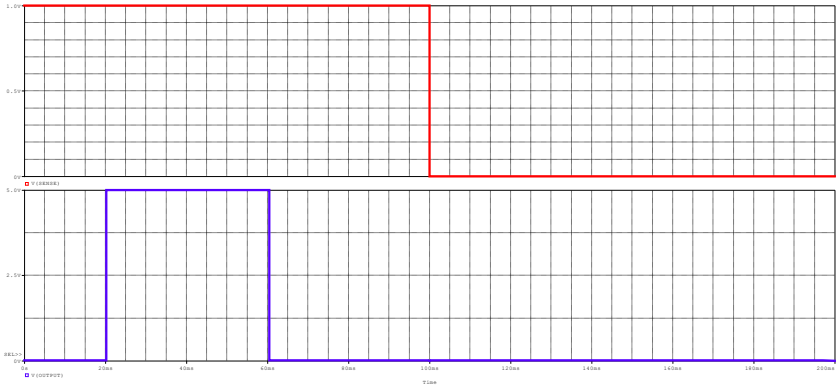

Figure 17. Programmable Pulse Generator Simulation with CT1 = 5µF and CT2 = 15µF

Figure 18 shows the simulation results with CT1 = 10 µF and CT2 = 15 µF. Since CT1 has doubled, the initial wait delay is twice as long. The pulse width delay deceased since CT1 increased.

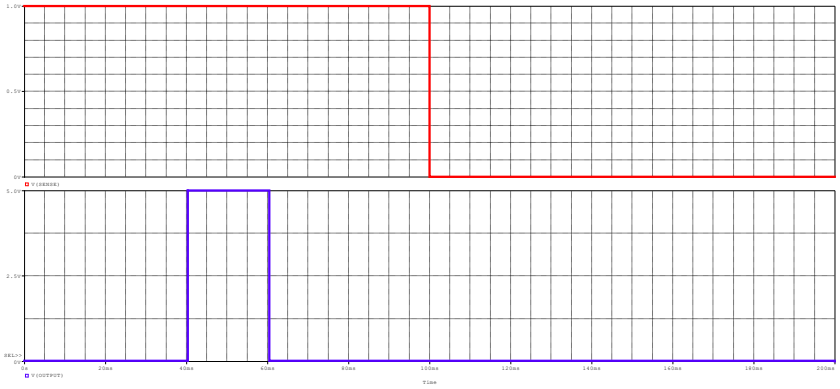

Figure 18. Programmable Pulse Generator Simulation with CT1 = 10µF and CT2 = 15µF

7 Discrete Push-Button

The discrete push-button solution is implemented with a resistor, capacitor, and either a buffer or inverter depending on the desired output logic. The push-button timing is set by charging the capacitor (or discharging the capacitor) through the resistor at the input of the logic device such that the capacitor chargers to VIH (or discharges to VIL) of the logic device in the desired duration of time. Choosing to charge the capacitor or discharge the capacitor depends on the desired input logic and timing. For example, the timing to charge from 0 V to VIH will likely be much quicker than discharging from a higher voltage such as 3.3 V to VIL for a given resistor, capacitor, and logic device.

Figure 19 shows the discrete push-button circuit diagram that uses a resistor and charging capacitor to create a delay.

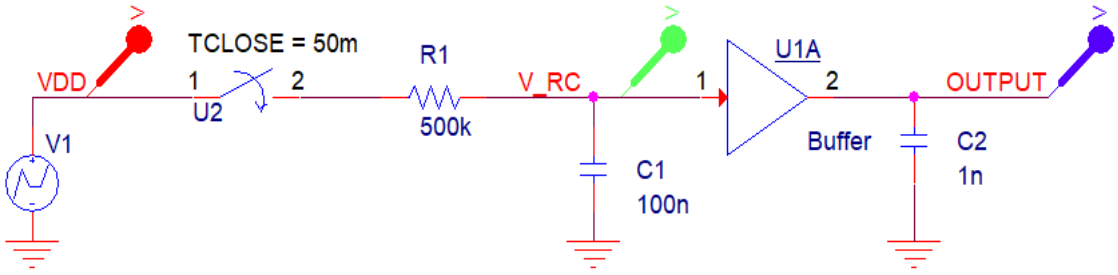

Figure 19. Disrete RC Charging Delay Circuit

In Figure 19, the switch or push-button U2 closes after 50 ms directly shorting the voltage supply to the RC network to charge the capacitor C1. The buffer has an input voltage threshold of 0.8 V meaning when the capacitor charges to 0.8 V, the OUTPUT transistions to logic high. C2 is added to filter the output and help with the propagation delay. The charging capacitor delay is derived from the voltage-charge relationship of an RC circuit:

$$V(t) = V_0(1 - e^{-t/(RC)}) \quad (5)$$

Solving for the charging delay time in seconds:

$$t = -\log((V_{DD} - V_C) / V_{DD})\ R * C \quad (6)$$

Figure 20 shows the simulation results of Figure 19.

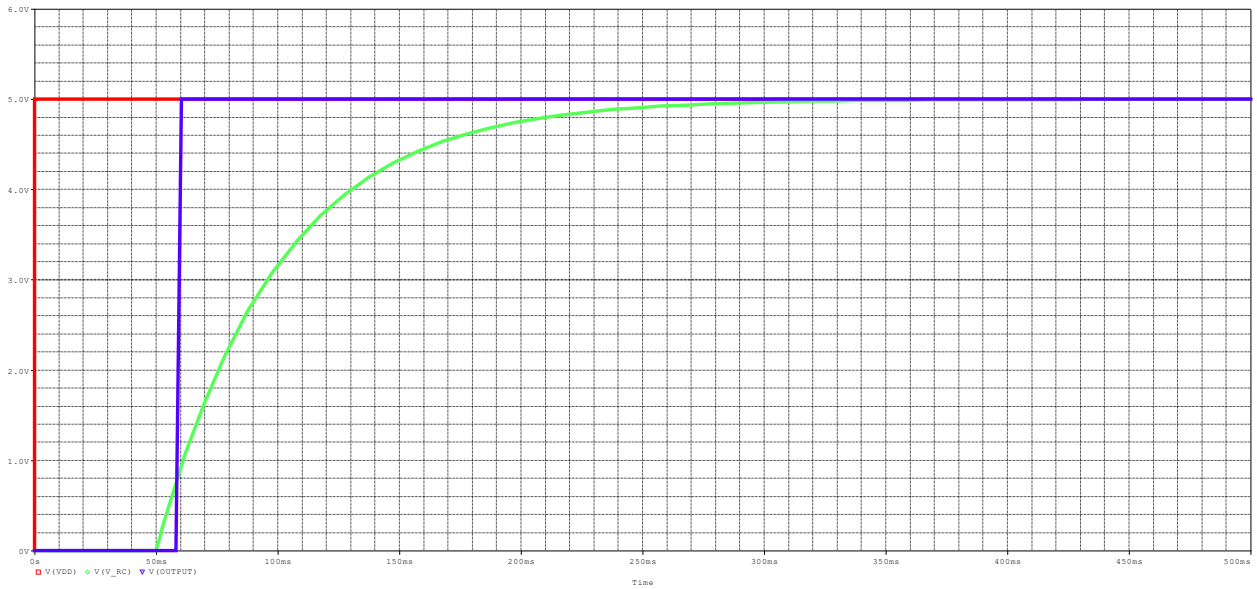

Figure 20. RC Delay With 500 KΩ Charging 100 nF

In Figure 21, the capacitor is increased to 2 µF to increase the delay.

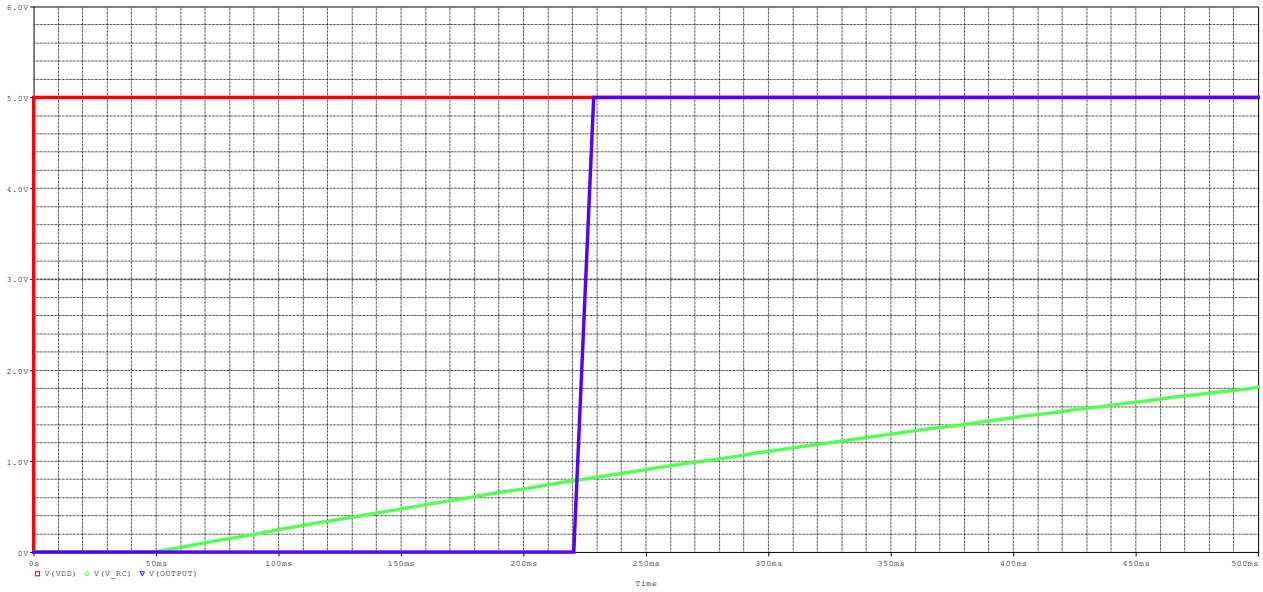

Figure 21. RC Delay With 500 KΩ Charging 2 µF

As previously mentioned, the RC delay can also be configured to utilize the capacitor discharging to trigger the output rather than the capacitor charging in the previous case. shows the the discrete push-button circuit diagram that uses a resistor and discharging capacitor to create a delay. Notice the discharging circuit uses a buffer just as the charging circuit thus the OUTPUT polarity is inverted since V_RC starts at VDD and discharges down to the input voltage threshold of the buffer which is 0.8 V before the OUTPUT transistions to logic low. If the buffer is replaced by an inverter for the discharging capacitor RC circuit, the OUTPUT polarity would match the charing capacitor RC circuit that uses a buffer. The charging capacitor delay is derived from the voltage-charge relationship of an RC circuit:

$$V(t) = V_0(e^{-t/(RC)}) \quad (7)$$

Solving for the discharging delay time in seconds:

$$t = -\log(V_C) / V_{DD}) R * C \quad (8)$$

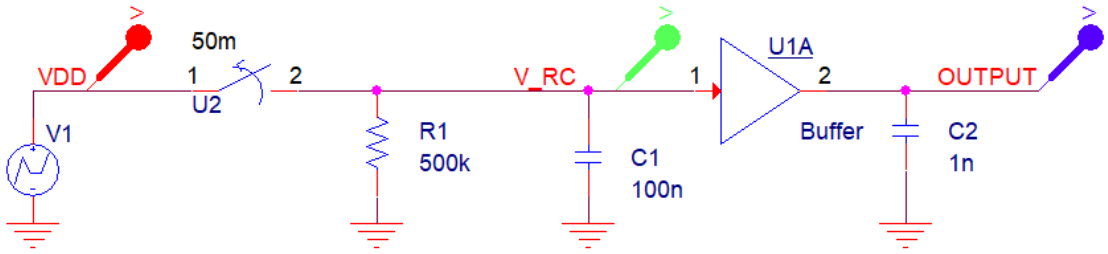

Figure 22. Disrete RC Discharging Delay Circuit

Figure 23 shows the simulation results of Figure 22

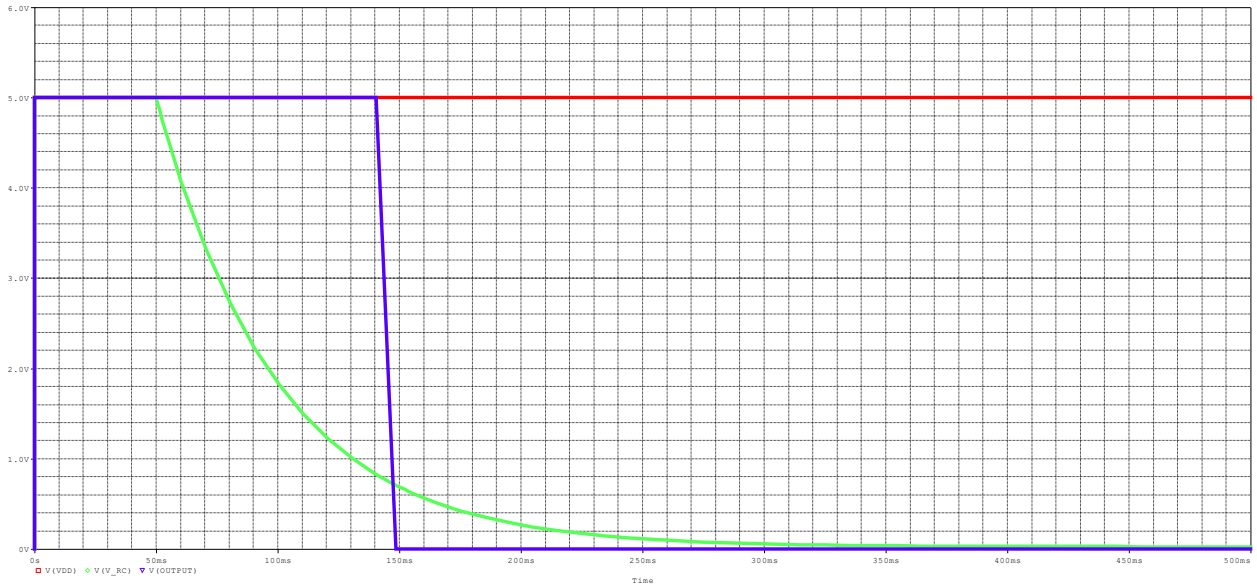

Figure 23. RC Delay With 500 KΩ Discharging 100 nF

In Figure 24, the capacitor is increased to 2 µF to increase the delay.

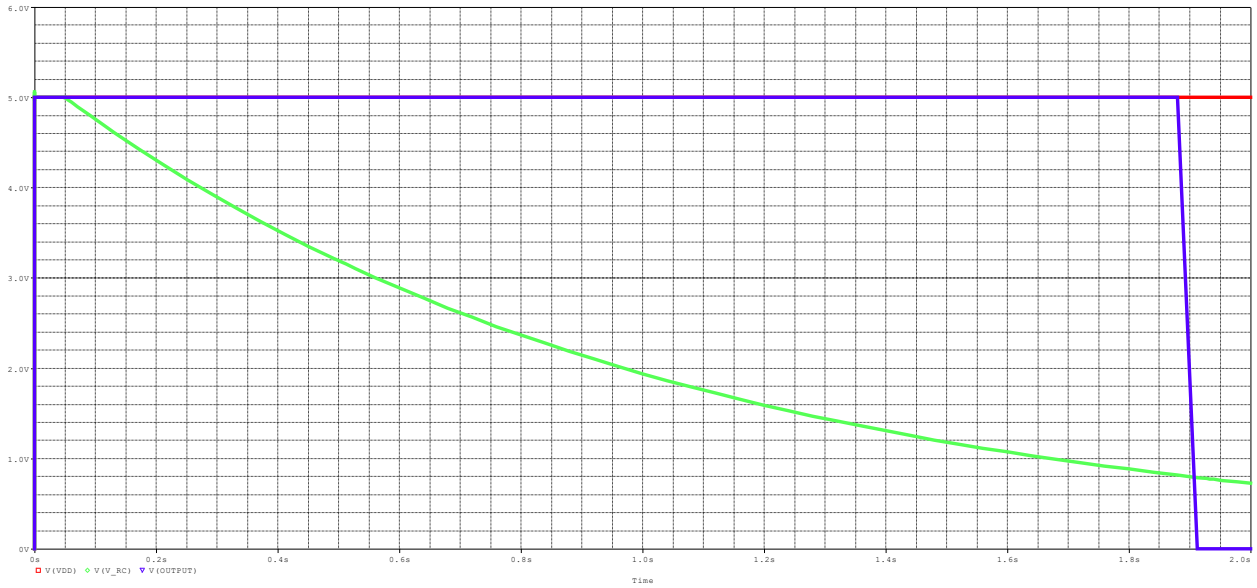

Figure 24. RC Delay With 500 KΩ Discharging 2 µF

With both buffers and inverters, there is usually a single input voltage threshold that causes the output to transistion. This can be an issue if the voltage input has ringing or is very close to the input voltage threshold of the device. In these cases, the buffer or inverter can be replace with a Schmitt trigger or Schmitt trigger inverter that uses hysteresis to create a low input voltage threshold (VIL) and a high input voltage threshold (VIH) such that there isn't a single common input threshold to cause the device to transistion. The benefit of the Schmitt trigger is that there is more immunity to ringing because there is significant difference between the input threshold that is consider logic low vs logic high. This can also increase propagation speed because the design can utilize a lower charging or higher discharging value before the output transistions.

8 Comparison Between Solutions

8.1 TPS342x Fixed Push-Button Solution

The advantages of the TPS3420, TPS3421, and TPS3422 family is the nano-Iq at 250 nA typical, two push-button input option, and the option of either a fixed reset delay or a reset delay that is depended on the release of the push-button inputs. These devices are also very small footprint at 1.45 mm x 1 mm and only require a pull-up resistor.

The disadvantages of the TPS3420, TPS3421, and TPS3422 family is the limited reset delay options of 7.5 seconds or 12.5 seconds, and the lack of analog voltage monitoring capability. Both of the other push-button solutions have programmability via external capacitor unlike this family of devices.

8.2 TPS389x Programmable Push-Button Solution

The advantage of the TPS3895, TPS3896, TPS3897, TPS3898 family is the programmable delay time using an external capacitor on the CT pin in addition to the ability to monitor analog signals, if needed, with a 1% voltage threshold monitoring accuracy. The delay accuracy for this family of devices is calculated using the CT pin charge current ($I_{(CT)}$) tolerance ~16% and the CT pin comparator threshold voltage ($V_{(CT)}$) tolerance ~4.6% for a total delay accurary ±20.6%. Like the TPS342x family, these devices are also very small footprint at 1.45 mm x 1 mm and only require a delay capacitor as shown in Figure 25. A pull-up resistor is required at the output for the open-drain variants (TPS3897 and TPS3898). This device family has low Iq at 6 µA typical and has all output logic polarities available.

The only disadvantage with this push-button solution is that the output logic depends on the status of the input once the programmed push-button timeout occurs which may not be desireable if the output is to remain asserted once the button is released after the push-button timeout expires.

8.3 Discrete RC Delay Push-Button Solution

The advantages of the discrete RC delay push-button is the low cost of the discrete components.

The main disadvantage of the discrete RC delay push-button is the dependency on the resistor, capacitor, and buffer/inverter input threshold accuracy which can significantly vary depending on tolerance grade and characteristics of the devices chosen. A rough example of the total accuracy assuming a ±5% resistor, ±10% capacitor, an a low-cost single Schmitt-trigger buffer (SN74LVC1G17) operating at 3 V is calculated as follows: 5% + 10% + ~12.9% = ~28% delay accuracy. The RC network also takes up more board space compared to the integrated push-button solution as shown in Figure 26. Similar to the TPS389x programmable push-button solution, the output after the RC delay time expires also depends on the status of the input but there is also a delay once the button is released before the output can transistion which may or may not be suitable for a given application.

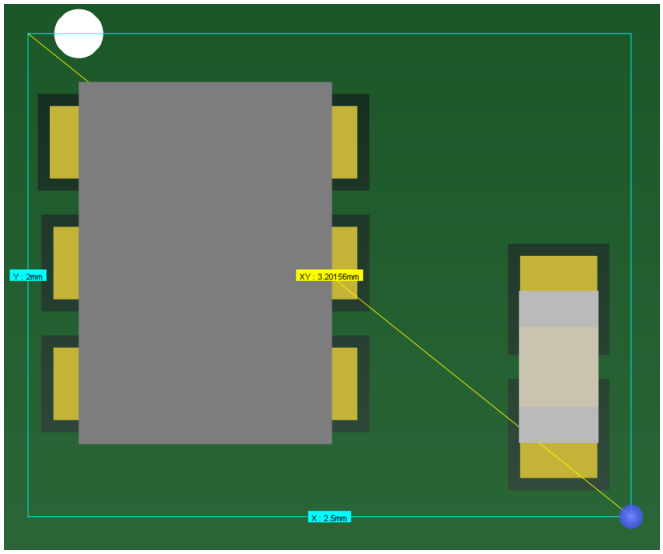

Figure 25. Integrated Push-Button Solution With TPS389x

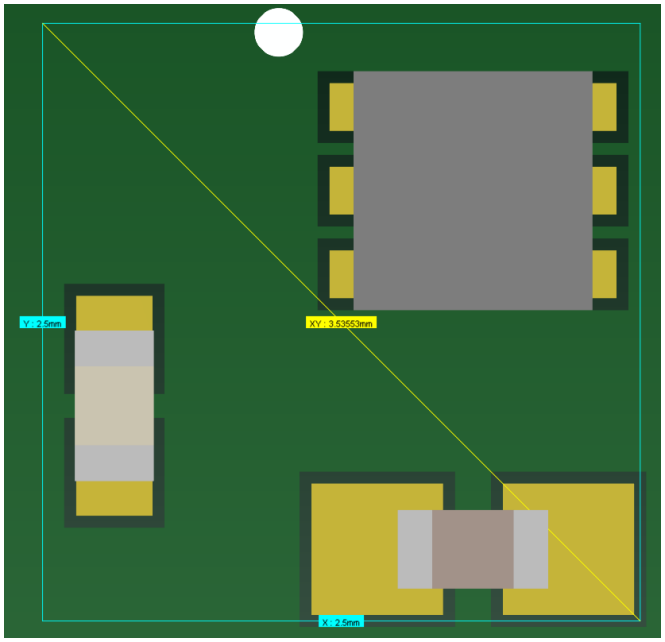

Figure 26. Discrete Push-Button Solution With RC Delay Circuit

9 TPS3840: Wide Input Voltage, Nano-Iq Alternate Device Option

In this application note, the fixed push-button family TPS3420, TPS3421, and TPS3422 are used because of their push-button functionality and the programmable reset delay voltage supervisor family TPS3895, TPS3896, TPS3897, and TPS3898 are used because the family includes both open-drain and push-pull output topologies, active-low and active-high output polarities, and they include an enable/disable pin making this family very flexible for various applications. The portion of this application note that uses the TPS389x family can also use alternate device options depending on the requirements of the application and how the devices are being used. The most basic push-button functionality can be accomplished with a voltage supervisor that features manual reset ($\overline{MR}$) pin and has a programmable reset time delay. A wide input voltage, nano-Iq device alternative is TPS3840 as this device is available in push-pull and open-drain, active-low and active-high, and includes programmable delay and a manaul reset ($\overline{MR}$) pin which is equivalent to ENABLE. The TPs3840 doesn't have a SENSE pin however so the TPS3840 only works for analog inputs that don't fall below $VDD_{(min)}$ = 1.5 V or digital inputs and push-buttons using the manual reset pin. TPS3840 offers VDD maximum up to 10 V however allowing this device to be used in wider voltage range applications.

If using the manual reset for the push-button functionality similar to the TPS3895A and TPS3897A solutions from Section 3 above, the TPS3840 push-button circuit requires the $\overline{MR}$ pin to be in a logic low state during normal operation. This keeps the TPS3840 in a reset condition. Then using a push-button that either causes $\overline{MR}$ to pull to logic high or float allowing the internal pull-up resistor to pull $\overline{MR}$ to logic high for the reset time delay duration, the device will release from reset condition and the output will transistion to logic high indicating the push-button has been activated until the reset time delay expired. An example circuit and timing diagram are shown below in Figure 27 and Figure 28

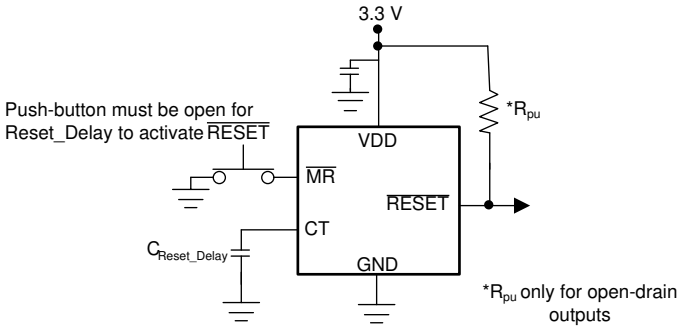

Figure 27. Typical Push-Button Circuit

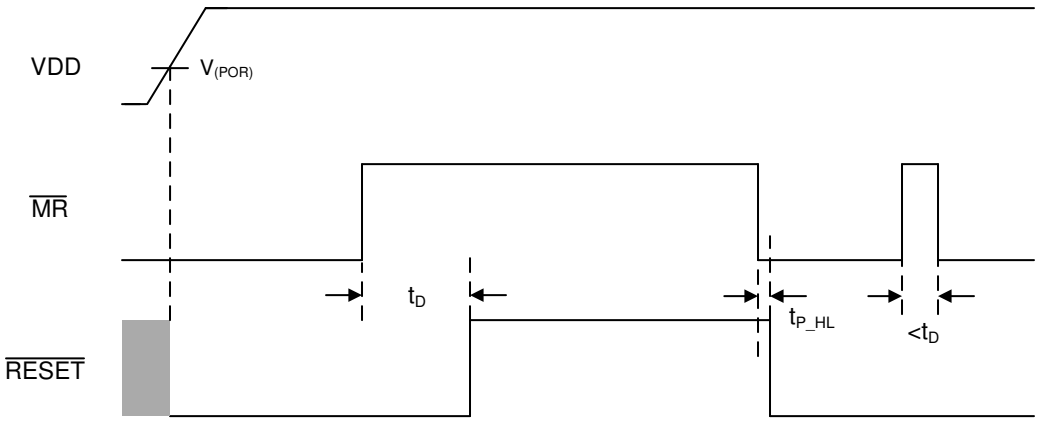

Figure 28. Typical Push-Button Timing Diagram

10 TLV840: Low-Cost Alternative Device Option

One of the lowest cost voltage supervisor in the industry with manual reset and programmable reset delay is TLV840. The main difference between TLV840 and TPS3840 from is that TPS3840 operates at an input voltage up to 10 V and TLV840 only operates at an input voltage up to 6 V. This could be a big difference if using the VDD pin for the push-button functionality or if the power supply is at a higher voltage. If the application does not require input voltage beyond 6 V, the lower cost TLV840 may be more suitable. The circuit and timing diagram follow that of TPS3840 as shown in Figure 27 and Figure 28. The disadvantage when compared to the TPS3895, TPS3896, TPS3897, and TPS3898 family push-button solutions is the output logic is fixed to logic low during normal operation and logic high once the push-button has been activated for the reset time delay. TLV840 doesn't have all of the output topologies offered by TPS3895, TPS3896, TPS3897, and TPS3898 family.

11 References

These references related to the devices mentioned in the application note.

- TPS342x Datasheet
- TPS389x Datasheet
- TPS3840 Datasheet
- SN74LVC1G17 Single Schmitt-Trigger Buffer
- Voltage Supervisors (Reset ICs) FAQ

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