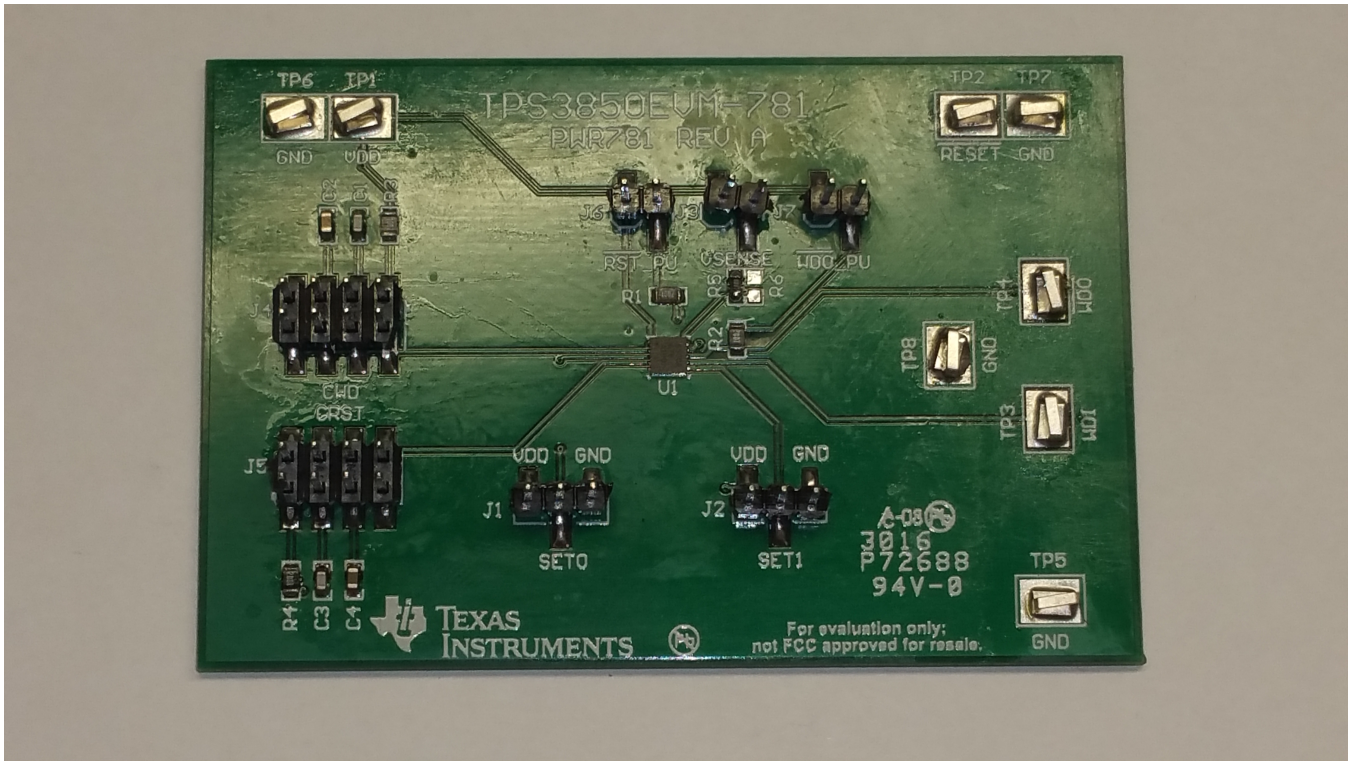
User's Guide
SBVU032–October 2016

TPS3850EVM-781 Evaluation Module



This user's guide describes the operational use of the TPS3850EVM-781 evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS3850, low quiescent current, 0.8% accurate supervisor with programmable-delay. Included in this user's guide are setup instructions, a schematic diagram, printed circuit board (PCB) layout drawings, and a bill of materials for the evaluation module.

Throughout this document, the terms *EVM*, *demonstration kit*, *evaluation board*, and *evaluation module* are synonymous with the *TPS3850EVM-781* evaluation module.

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1 Introduction

TI's TPS3850EVM-781 helps design engineers evaluate the operation and performance of the TPS3850 family of supervisors for possible use in their own circuit application. This particular EVM configuration contains the TPS3850H01 in a DRC (3 mm × 3 mm) package. This document describes the configuration and set up of the TPS3850EVM-781 EVM board.

2 Hardware

This section describes the jumpers and connectors on the EVM as well as how to properly connect, setup, and use the TPS3850EVM-781.

2.1 Input and Output Connector and Jumper Descriptions

2.1.1 TP1: VDD

This connector is for the input power supply. The operating range of this supervisor is 1.6 V to 6.5 V.

2.1.2 TP2: $\overline{\text{RESET}}$

This connector is the $\overline{\text{RESET}}$ output. Connect this output to a multimeter, oscilloscope, or external circuit to verify that $\overline{\text{RESET}}$ goes low when the monitored voltage goes below the threshold.

2.1.3 TP3: WDI

This test point allows the user to connect an external WDI signal to the TPS3850EVM.

2.1.4 TP4: $\overline{\text{WDO}}$

This connector is the $\overline{\text{WDO}}$ output. Connect this output to a multimeter, oscilloscope, or external circuit to verify that $\overline{\text{WDO}}$ goes low when the WDI signal is not issued within the correct window.

2.1.5 TP5 through TP8: GND

These connectors are GND and are electrically connected to each other.

2.1.6 J1: SET0

The TPS3850EVM-781 is designed with an external SET0 pin to allow the user to program different watchdog and reset timing options. Table 1 shows the connections for choosing between the timing ratios and options. If the shorting jumper is removed, an external voltage can be placed on pin 2, labeled SET0 in Figure 1.

Table 1. Connector JP1 Selections

Short Pins	SET0 Voltage
1 and 2	VDD
2 and 3	GND
OPEN	Externally applied voltage on pin 2

2.1.7 J2: SET1

The TPS3850EVM-781 is designed with an external SET1 pin to allow the user to program different watchdog and reset timing options. Table 2 shows the connections for choosing between the timing ratios and options. If the shorting jumper is removed, an external voltage can be placed on pin 2, labeled SET1 in Figure 1.

Table 2. Connector JP2 Selections

Short Pins	SET1 Voltage
1 and 2	VDD
2 and 3	GND
OPEN	Externally applied voltage on pin 2

2.1.8 J3: SENSE

The TPS3850EVM-781 is designed to monitor VDD or an external sense voltage, which is placed on pin 2 of J3. Table 3 shows the connections for choosing between the two monitoring options.

Table 3. Connector JP3 Selections

Short Pins	Voltage Monitored
1 and 2	VDD
OPEN	Externally applied voltage on pin 2

2.1.9 J4: CWD

For convenience, the TPS3850EVM-781 is designed to allow the CWD to be tied to VDD through a pullup resistor, connected through a capacitor to GND, or left floating. Table 4 shows the connection options, assuming the SET0/SET1 pins are both tied to GND.

Table 4. Connector JP4 Selections

Short Pins	Capacitor	$t_{WDL(max)}$ (ms)	$t_{WDU(min)}$ (ms)
1 and 2	10 kΩ to VDD (R3)	10.4	92.7
3 and 4	100 pF (C1)	19.0	112.5
5 and 6	Blank pads (C2)	User programmable	User programmable
7 and 8	OPEN	25.9	46.8

2.2 J5: CRST

For convenience, the TPS3850EVM-781 is designed to allow the CRST to be tied to VDD through a pullup resistor, connected through a capacitor to GND, or left floating. Table 5 shows the connection options.

Table 5. Connector JP5 Selections

Short Pins	Capacitor	Delay
1 and 2	10kΩ to VDD (R4)	10
3 and 4	100 pF (C3)	0.703
5 and 6	Blank pads (C4)	User programmable
7 and 8	OPEN	200

2.3 J6: $\overline{\text{RESET}}$ Pullup

The TPS3850EVM-781 is designed with an open-drain $\overline{\text{RESET}}$ output, which needs to be pulled up to either VDD or an externally supplied voltage. Table 6 shows the connections for choosing between the two monitoring options.

Table 6. Connector JP6 Selections

Short Pins	Pullup Voltage
1 and 2	VDD
OPEN	External voltage supplied on pin 2

2.4 J7: $\overline{\text{WDO}}$ Pullup

The TPS3850EVM-781 is designed with an open-drain Watchdog Output ($\overline{\text{WDO}}$) output, which needs to be pulled up to either VDD or an externally supplied voltage. Table 7 shows the connections for choosing between the two monitoring options.

Table 7. Connector JP7 Selections

Short Pins	Pullup Voltage
1 and 2	VDD
OPEN	External voltage supplied on pin 2

3 Board Layout

Figure 1 through Figure 3 show the board layouts.

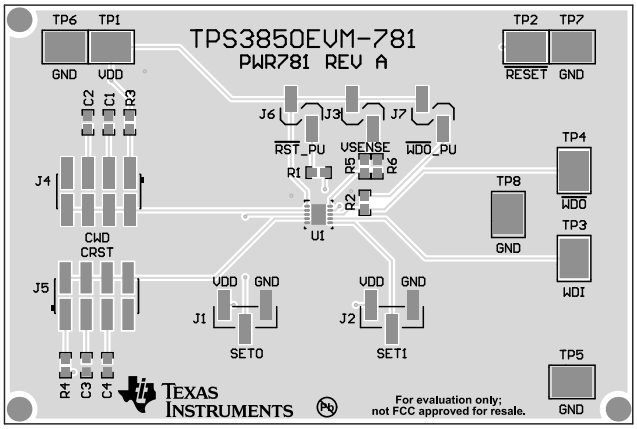

Figure 1. Top Overlay

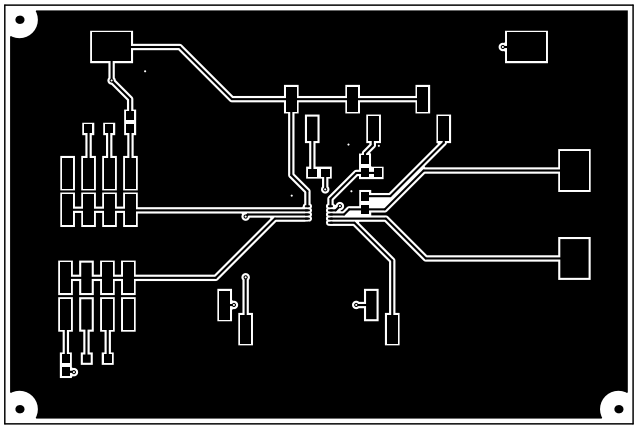

Figure 2. Top Layer

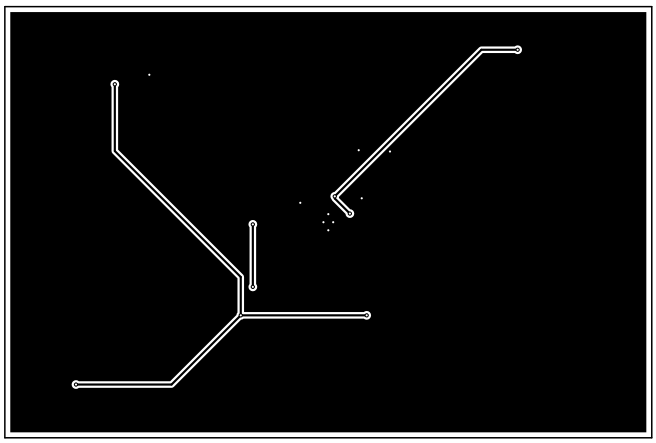

Figure 3. Bottom Layer

4 Schematic

Figure 4 illustrates the EVM schematic.

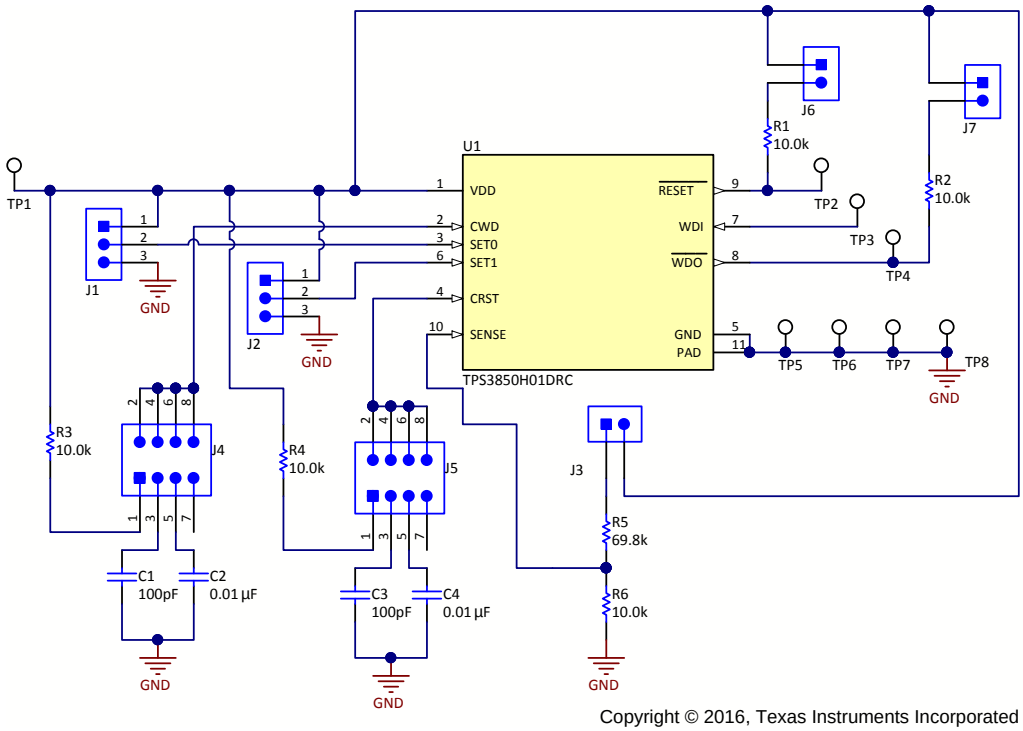

Figure 4. TPS3850EVM-781 Schematic

5 Bill of Materials

Table 8 lists the EVM BOM.

Table 8. TPS3850EVM-781 BOM

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		PWR781	Any	-	-
C1, C3	2	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	06035A101JAT2A	AVX		
J1, J2	2		Header, 100mil, 3x1, Gold, SMT	Samtec_TSM-103-01-X-SV	TSM-103-01-L-SV	Samtec		
J3, J6, J7	3		Header, 2.54 mm, 2x1, Gold, R/A, SMT	Header, 2.54 mm, 2x1, R/A, SMT	87898-0204	Molex		
J4, J5	2		Header, 2.54 mm, 4x2, Tin, SMT	Header, 2.54mm, 4x2, SMT	0015912080	Molex		
R1, R2, R3, R4, R6	5	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo America		
R5	1	69.8k	RES, 69.8 k, 1%, 0.1 W, 0603	0603	CRCW060369K8FKEA	Vishay-Dale		
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7	7	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	8	SMT	Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone		
U1	1		High Accuracy Voltage Supervisor with Integrated Watchdog Timer, DRC0010J	DRC0010J	TPS3850H01DRC	Texas Instruments		Texas Instruments
C2, C4	0	0.01uF	CAP, CERM, 0.01 µF, 25 V, +/- 5%, C0G/NP0, 0603	0603	C1608C0G1E103J	TDK		
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A		

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      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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Concernant les EVMs avec antennes détachables

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3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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