Texas Instruments

TSW2000

Receive Clock Jitter Cleaning Evaluation Module (EVM)

User's Guide

2004

Clock Drivers

SCAU011

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 3.6 V (or differential voltage range of 0 V to 1.4 V on ports RXN / RXP), the output voltage range of 0 V to 4.1 V and power supply of 6 V maximum.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This user's guide describes the usage and construction of the receive clock jitter cleaning evaluation module (EVM) containing the TLK1201A gigabit ethernet 0.6-Gbps to 1.3-Gbps transceiver and CDC7005 low phase noise clock synchronizer. The design of this EVM supports usage of all TLK1201 and TLK2201 gigabit ethernet transceivers.

This document provides guidance on proper use by showing possible test configurations. In addition, design, layout, and schematic information are provided to the user. Information in this user's guide can be used to assist the customer in choosing the optimal design methods and materials in designing a complete system.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1—Introduction
- ❏ Chapter 2—Quick Start
- ❏ Chapter 3—EVM Hardware
- ❏ Chapter 4—Test and Setup Configurations
- ❏ Chapter 5—PCB Construction and Characteristics
- ❏ Chapter 6—Bill of Materials, Board Layouts, and Schematics

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This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

- TLK1201A data sheet
- TLK2201 SerDes EVM Kit Setup and Usage user's guide (SLLU011)
- CDC7005 data sheet
- CDC7005 EVM manual (SCAU005)
- General Guidelines: CDC7005 as a Clock Synthesizer and Jitter Cleaner application note (SCAA063)
- Phase Noise (Jitter) Performance of the CDC7005 With Different VCXOs application note (SCAA067)

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Contents

Figures

Tables

Chapter 1

Introduction

The Texas Instruments receive clock jitter cleaning evaluation module (EVM) is used to test the functionality and the performance of the CDC7005 clock synchronizer device using the TLK1201A serializer/ deserializer (SerDes) recovered clock output (RBC0) as a reference input.

The jitter performance of the RBC0 clock output may fail the requirements of systems where this clock is used for further data processing, particularly in data converter circuits (i.e., radio remote unit). This EVM shows a way of solving this problem by using the CDC7005 to synchronize a clock signal of a voltage controlled crystal oscillator (VCXO) to the RBC0. Thus, the clean output clock of the CDC7005 can be used for data conversion.

The TLK1201A gigabit ethernet (IEEE802.3z) transceiver performs parallel-to-serial and serial-to-parallel data conversion and supports a serial interface speed of 0.6 to 1.3 Gbps. The transmitter latches 10-bit 8B/10B-encoded parallel data (TD[9:0]) at a rate based on the supplied reference clock (REFCLK). The 10-bit parallel data is internally serialized and then transmitted differentially at 10 times the REFCLK rate. The receiver section performs the serial-to-parallel conversion on the input data, synchronizing the resulting 10-bit wide parallel data to the extracted reference clock (RBC0). The parallel output data is present on terminals RD[9:0]. The primary application of the TLK1201A transceiver is to provide high-speed I/O data channels compliant to the IEE802.3z gigabit ethernet specification for point-to-point data transmission over controlled impedance media of approximately 50 Ω (cable or PCB) or optical links.

The CDC7005 is a high-performance, low phase noise and low skew clock synchronizer that synchronizes a VCXO frequency to an external reference clock. The device operates up to 800 MHz. The PLL loop bandwidth and dampening factor can be adjusted to meet different system requirements by selecting the external VCXO, loop filter components, frequency for PFD, and charge pump current. Each of the five differential LVPECL outputs can be programmed by a serial peripheral interface (SPI) allowing individual control of the frequency and enable/disable state of each output. As the system requires external components like a loop filter and VCXO, this EVM provides an excellent way to evaluate and modify the performance and parameters of the clock system in conjunction with the specific customer application. Loop

bandwidth can be selected as low as 10 Hz or less, allowing this device to clean the system’s clock jitter.

Chapter 2
Quick Start

In order to setup the EVM quickly and to perform some measurements at default settings, the following actions are required (also see the *Jitter Performance Comparison Test Setup* section):

1) Supply 5 V to J2 and ground to J1.

2) Apply a single-ended reference clock signal of 61.44 MHz to the reference clock input of the TLK1201A (J24: REFCLK_EXT).

3) Apply a differential pseudo random bit stream (PRBS 2^7-1) with a frequency of 614.4 Mbps (10 x 61.44 MHz) ±61.44 kbps (±100 ppm which is the specified maximum frequency deviation between 1/10 of the incoming serial data speed and the receiver reference clock frequency) to the serial data inputs RXN/P (J7 and J8) of the TLK1201A. The more the PRBS speed deviates from the REFCLK_EXT frequency (within the given range), the easier it is to recognize the negative effects on the RBC0 of the TLK (see the step 4).

4) Connect RBC0_CLK (J9) and Y4_CLK/Y4B_CLK (J15/J16) outputs of the CDC to an oscilloscope or spectrum analyzer in order to compare the quality of both signals. RBC0_CLK signal will imply a certain amount of phase noise (jitter) dependent on the difference between the REFCLK_EXT frequency and 1/10 of the PRBS data speed. The quality of the clock output of the CDC corresponds to the quality of the VCXO output.

After power up, the STATUS_VCXO LED will be on if the VCXO works properly (default). After providing REFCLK to the TLK, the STATUS_REF LED will be on, indicating a valid reference signal at the CDC. If the reference clock and the VCXO clock are phase locked, the STATUS_LOCK LED will be on.

Note:

Be aware of the default settings of the CDC7005 (described in SCAS685), i.e., if you use a 61.44-MHz VCXO, the Y3 output divider has to be set to Div by 1 (default: Div by 8). If you use a 122.88-MHz VCXO, the Y3 output divider should be set to Div by 2 in case of a 614.4Mbps serial data stream or to Div by 1 in case of a 1.2288 Gbps ±100-ppm serial data stream (see also section 4.1 and section 4.2).

Chapter 3

EVM Hardware

This chapter shows the features of the EVM and explains the board interfaces along with the default settings.

Topic **Page**

3.1 High-Speed Design Considerations

The board can be used to evaluate device parameters while acting as a guide for high-speed board layout. As the frequency of operation increases, the board designer must take special care to ensure that the highest signal integrity is maintained. To achieve this, the board's impedance is controlled to 50 Ω for the high-speed differential serial and low-speed parallel data and all clock connections. In addition, board impedance mismatches are reduced by designing the component's pad size to be as close as possible to the width of the connecting transmission lines. Number and size of vias are minimized. Care was taken to control trace length mismatch (board skew) within corresponding signal pairs and buses. Overall, the board layout is designed and optimized to support high-speed operation.

Some of the advanced features offered by this board include:

- A printed circuit board (PCB) that is designed for high-speed signal integrity
- SMA and parallel fixtures are easily connected to test equipment
- All input/output signals are accessible for rapid prototyping
- All power supplies are designed as copper pours on a separate power layer in order to lower the inductance of the power connections, while supporting better current distribution; ferrites are used for separating analog and digital supplies of a certain device.
- On-board capacitors provide ac-coupling of high-speed and clock signals

3.2 TSW2000 EVM Board Configuration

The EVM provides developers with some operational modes, most of which are selectable via jumpers. Other options can be selected using the serial peripheral interface (SPI) of the CDC7005. The EVM needs a 5-V power supply, which can be provided using banana jacks.

3.2.1 Interfaces

The EVM provides two 38-pin headers for connecting the parallel transmit/receive buses of the TLK1201A (J3 and J4); the headers consist of data signals with adjacent grounds and corresponding transmit/receive byte clocks (REFCLK_EXT and RD_CLK).

Note:

The EVM is designed to support all TLKx201x devices.

The TLK1201A provides 10-bit wide LVTTL (TBI) parallel input data interface TD[9:0] (J3) latched on rising edge of the device's reference clock REFCLK. There are two ways to apply a clock signal to the REFCLK input selectable via J17 (which has to be soldered properly):

- External clock signal via REFCLK_EXT on SMA connector J24 or
- CDC7005 Y0B output; ac coupled

The receive parallel data RD[9:0], along with the corresponding receive clock RD_CLK, can be verified via header J4. The RD_CLK on J4 is a jitter cleaned version of TLK's recovered clock (Y0 output signal of the CDC7005) and its phase might be shifted comparing to the data phase. Using the programmable delay feature of the CDC, this offset can be compensated.

The original recovered clock RBC0 of the TLK can be accessed via the SMA connector RBC0_CLK (J9), after being buffered by the CDCV304 device (U12). Another output of the CDCV304 buffer is used by the CDC7005 as a reference clock.

The high-speed serial data for the TLK can be provided via SMA connectors RXP/N (J7 and J8); serial data output of the TLK is applied to SMA connectors TXP/N (J5 and J6). Since the serial transmit signals TXP/N are ac-coupled, a direct or attenuated connection to the test equipment is possible resulting in a voltage swing around zero. Additionally, the serial receive signals RXP/N are also ac-coupled and biased to provide the correct common-mode dc-level and enabling easy connection to test equipment.

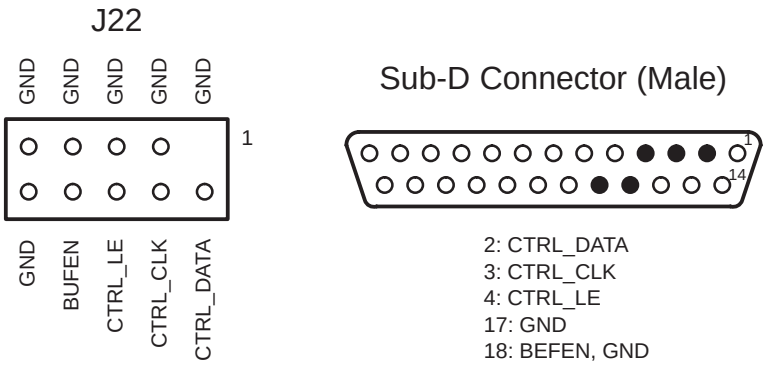
The EVM allows also testing of following CDC7005 output signals via SMA connectors:

- Y4 differential PECL output: directly on Y4_CLK and Y4B_CLK (J15 and J16)
- Y2 or Y3 outputs via SN65LVCP22 cross-point switch (U4) on OUT0± (J13 and J14)

This allows additional testing of the Texas Instruments cross-point switch output signal performance in order to evaluate their usability in applications with redundant clock sources.

The jitter cleaning evaluation board can be configured using control headers described in Figure 3−1 or externally through a serial peripheral interface (SPI) via port J22. The SPI port provides greater flexibility and control of the CDC7005 device. The SPI signals are interfaced through the J22 supplying the SPI load enable (CTRL_LE), buffer enable (for U6), SPI data (CTRL_DATA), and SPI clock (CTRL_CLK) signals plus ground.

Figure 3−1. SPI Connector (J22) and 25-Pin Sub-D Male Connector (For PC Parallel Port)



Note:

The BUFEN signal is hard-wired to ground within the parallel port connector thus the on-board buffer will be enabled as soon as the connector is plugged and automatically disenabled whenever the SPI cable is disconnected (on-board pullup).

3.2.2 Power Supply

The TLK1201A needs three 2.5-V (±0.2 V) power supplies to work properly: VDD (digital logic power), VDDA (analog power), and clean VDDPLL (PLL power supply). The CDC7005 needs two 3.3-V (±0.3 V) power supplies: VCC (digital power) and AVCC (analog power). This prevents coupling of the switching noise between the analog and digital sections within the both devices.

The EVM is supplied over banana jack J2 (5 V). 3.3 V and 2.5 V for the on-board devices are generated by Texas Instruments dual low-dropout (LDO) voltage regulator TPS70258 (U7). For new designs, however, using Texas Instruments single TPS796xx LDOs is recommended. Those LDOs do not need low ESR capacitors as the TPS70258.

In all sections of the board, the ground planes are common and each ground plane is tied together at every component ground connection and additional ground vias spread throughout the whole EVM. A ground connection to the board is provided via J1 (GND). For a detailed schematic and layout, see Chapter 6.

Warning:

Keep the power supply for the EVM below 6 V to avoid damage of the on-board LDO.

3.2.3 Default EVM Delivery Settings

The board is delivered in a default configuration that requires external clock and data inputs. Table 3−1 shows the default settings.

Table 3−1. TSW2000 EVM Default Board Settings (As Shipped)

Designator	Function	Condition
J17	REF_CLK SELECTOR	TLK reference clock selector − set to REFCLK_EXT (J24) using a 10-nF capacitor. Another option is Y0B output of CDC7005.
J18/19	VCXO SELECTOR	No connection: set to use on-board VCXO. Shortening this solder bridge allows to test external VCXO connected to J10−12. On-board VCXO has to be removed.
J20	V_CTRL_VCXO	Voltage control selector − set to use CDC7005 to control the on-board VCXO. External voltage control can be achieved via J10 (V_CTRL_EXT). Tying the outer pins of this header together allows controlling external VCXO by CDC7005 via J10 (see section 4.3).
J21	POWER_RESET	Using a jumper, the on-board LDO can be reset via this header.
J23 (**TLK status**)	SYNC/PASS	Synchronous detect. The SYNC output is asserted high upon detection of the comma pattern in the serial data path. SYNC pulses are output only when SYNCEN is activated (asserted high). In PRBS test mode (PRBSEN = high), SYNC/PASS outputs the status of the PRBS test results (high = pass).
	LOS	Loss of signal If magnitude of RXP–RXN > 150 mV, LOS = 1, valid input signal If magnitude of RXP–RXN < 150 mV and > 50 mV, LOS is undefined If magnitude of RXP–RXN < 50 mV, LOS = 0, loss of signal
J25 (CDC control)	NRESET (input)	No jumper (Logic 1) – device enabled When low, resets all internal dividers of the CDC7005.
	NPD (input)	No jumper (Logic 1) – normal operation When low, the device is put in power down mode. All current sources are off; internal dividers are reset and all outputs high-Z.
J26 (**CDC status**)	STATUS_LOCK	When high, this terminal indicates locked PLL.
	STATUS_REF	When high, this terminal indicates valid reference input (frequency above 3.5 MHz).
	STATUS_VCXO	When high, this terminal indicates valid VCXO clock (frequency above 10 MHz).

Designator	Function	Condition
J28 (TLK control)	ENABLE	No jumper (Logic 1) – device enabled Putting a jumper on this header disables the TLK device.
	SYNCEN	Jumper set (Logic 0) − synchronous function disabled When this function is activated, the transceiver detects the K28.5 comma character (0011111 − negative running disparity) in the serial data stream and realigns data on byte boundaries, if required.
J31 (TLK control)	LOOPEN	No jumper (Logic 0) – loop-back disabled When high, the internal loop-back path is activated. The transmitted serial data is routed internally to the inputs of the receiver.
	PRBSEN	Jumper set (Logic 1) – PRBS enabled Internal PRBS generator is activated and results of the PRBS test on receive path can be monitored on the PASS pin (J23). When low, PRBS functions are disabled.
R49/50	Termination resistors	These resistors are not assembled by default. They can be assembled if DC-offset on the RD_CLK (J4) is needed.
R69	Termination resistor	This resistor is not assembled by default. It can be assembled if a high-Z probe is used to measure the quality of RBC0 (J9).
R65−68 / 70 / 72−74	Termination resistors	These resistors are not assembled by default. They can be used as termination resistors for the LVPECL outputs if a high-Z probe is used to measure the quality of those signals (J13−16).

Chapter 4

Test and Setup Configurations

The following configurations are used to evaluate and test the TLK1201A along with the CDC7005.

Topic **Page**

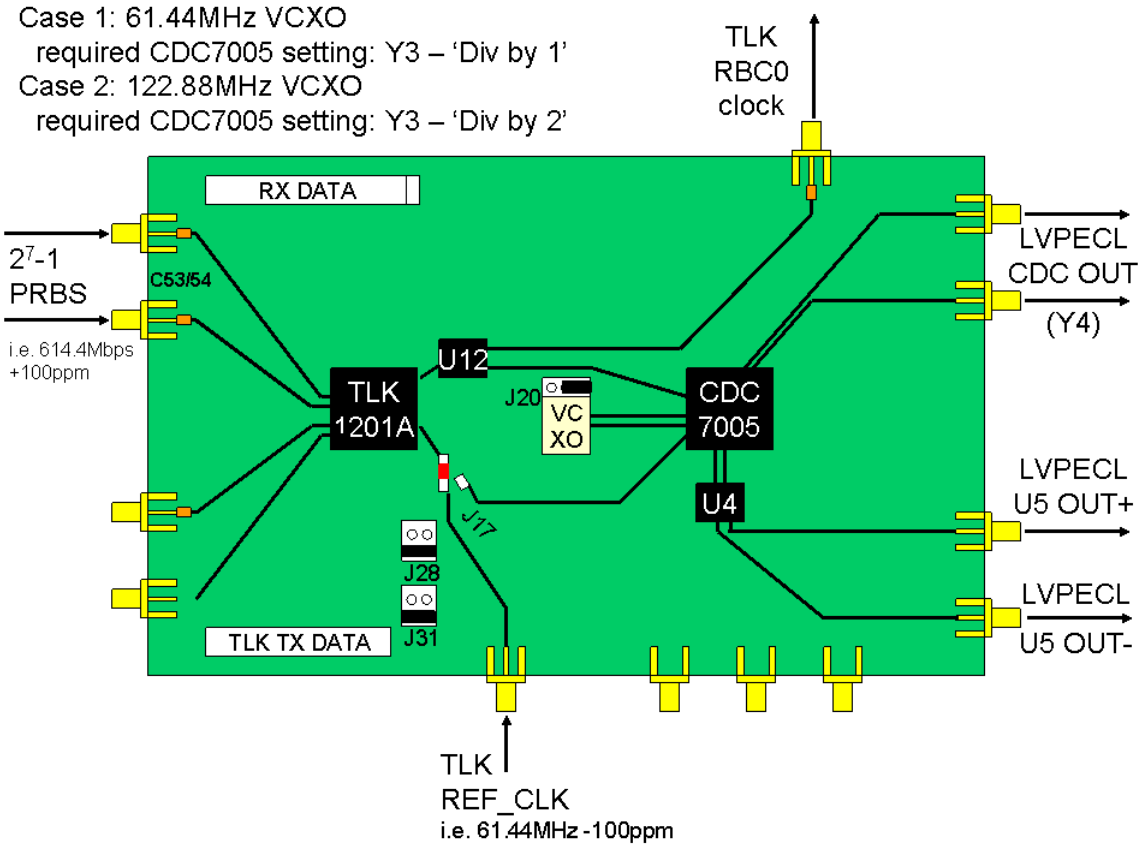
4.1 Jitter Performance Comparison Test Setup

The first configuration allows a jitter performance comparison between the recovered clock (RBC0) of the TLK transceiver and one of the LVPECL outputs of the CDC7005 after jitter cleaning. To perform this test, steps 1 through 4 have to be completed as described in Chapter 2.

Note:

With an 122.88-MHz VCXO, you may provide i.e., 1.2288-Gbps +100 ppm serial PRBS stream and 122.88-MHz −100 ppm REF_CLK. The CDC7005 Y3 divider has to be set to Div by 1.

Figure 4−1. Jitter Performance Comparison Test Configuration



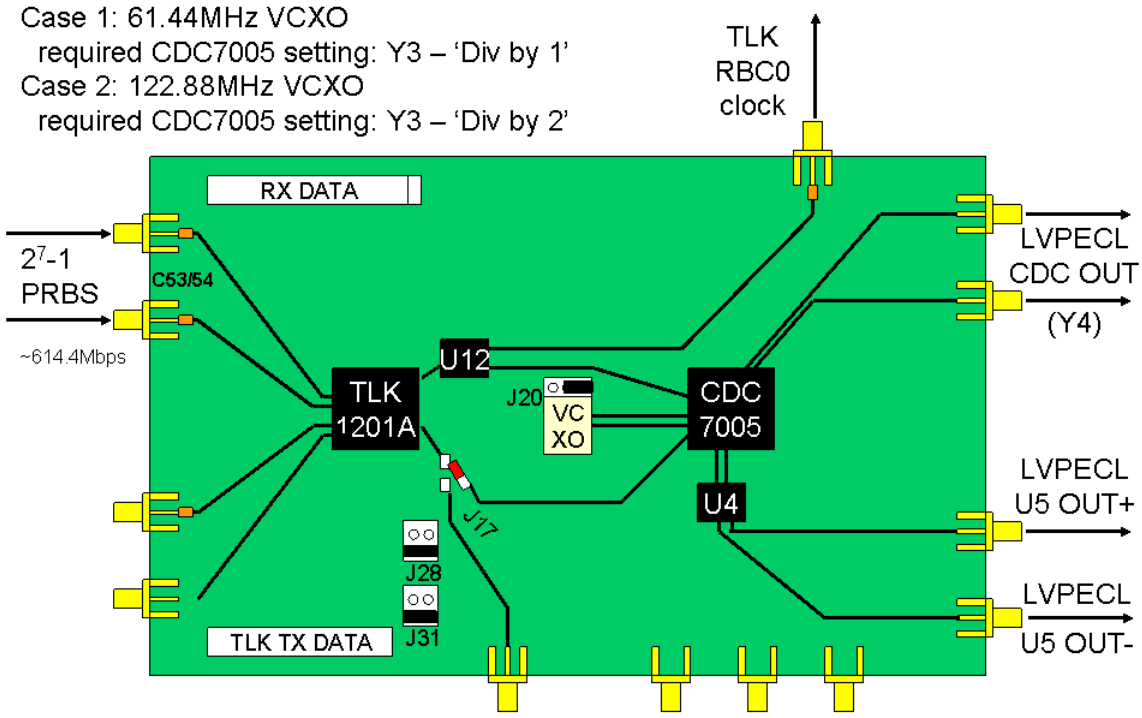
4.2 Jitter Cleaning and Synchronization Test Setup

This test setup allows evaluation of the synchronization feature of the CDC7005. Feeding back one of the CDC7005 outputs to the TLK as a reference clock, the transmitting path of the TLK will be synchronized to the frequency of the far-end system providing the serial data to the TLK.

Note:

With an 122.88-MHz VCXO, you may provide i.e., 1.2288-Gbps +100 ppm serial PRBS stream and 122.88-MHz −100 ppm REF_CLK. The CDC7005 Y3 divider has to be set to Div by 1.

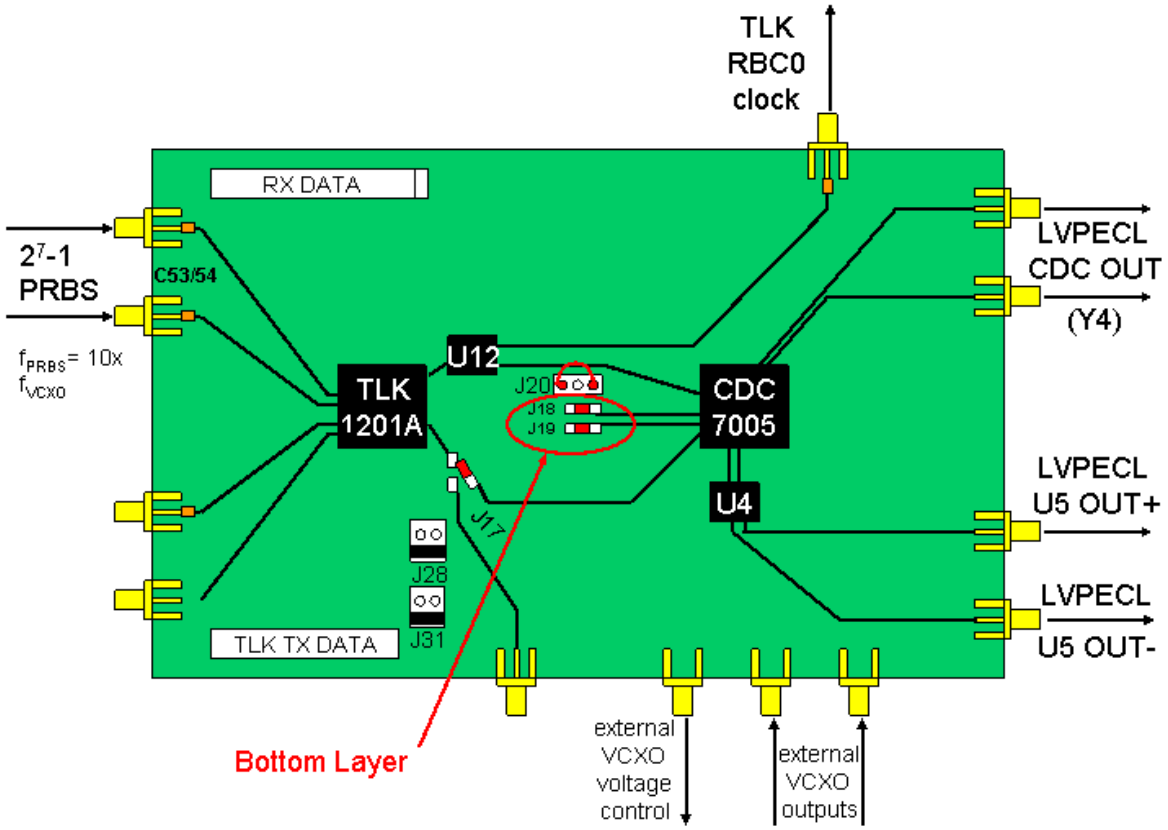
Figure 4−2. Jitter Cleaning and Synchronization Test Configuration



4.3 External VCXO Test Setup

The EVM allows testing of different VCXOs by providing an interface for an external VCXO clock signal for the CDC via VCXO_IN_EXT and VCXO_INB_EXT (J11 and J12), plus voltage control connection V_CTRL_EXT (J20). To use an external VCXO, jumpers J18/19/20 should be set properly (see Figure 4−3).

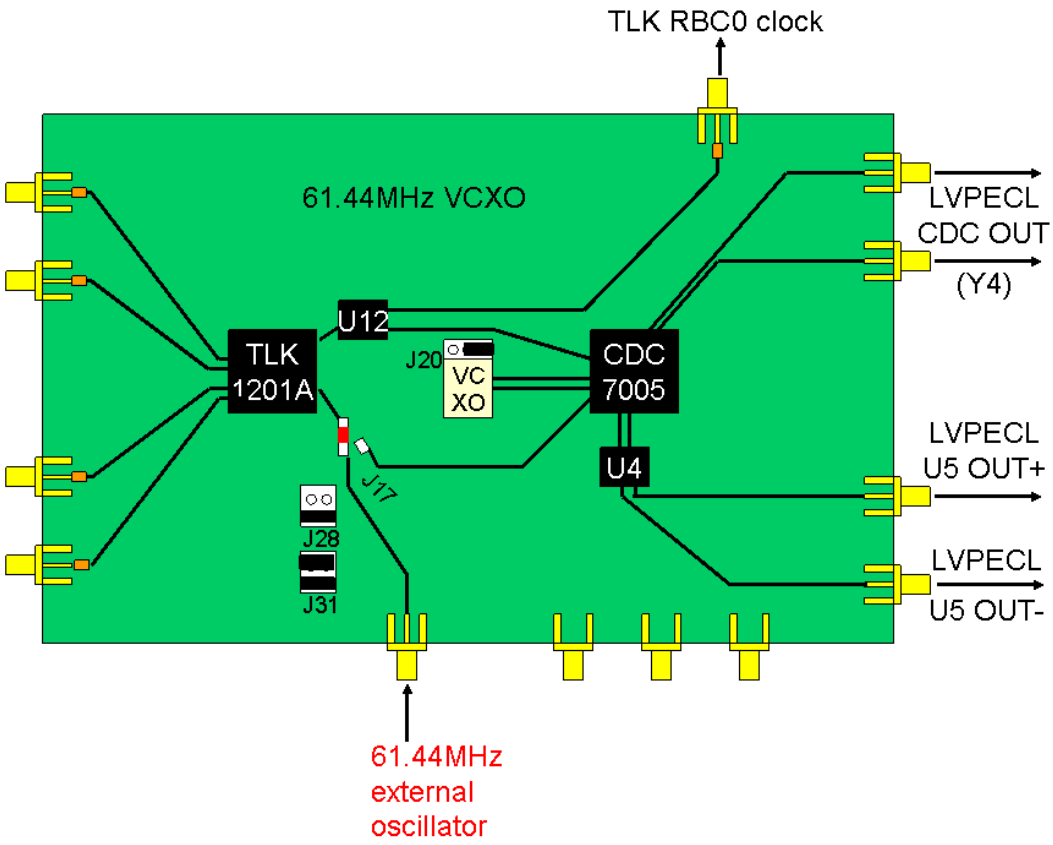
Figure 4−3. External VCXO Test Configuration



4.4 Stand Alone Test Setup

The TLK1201A provides an internal 2^7-1 PRBS generator and verification function which can be used along with the internal loop back for stand alone testing (no need for an external signal generator). Figure 4−4 shows the basic test configuration for this case (J28 and J31 have to be set accordingly).

Figure 4−4. Stand Alone Test Configuration



Chapter 5

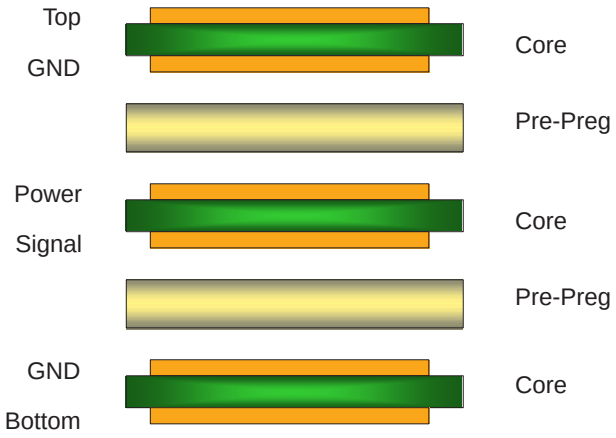
PCB Construction and Characteristics

Overall board thickness is ~1,59 mm (62.5 mil), board material is FR−4.

Copper thickness is 0.18 µm (~0.708 mil).

High-speed and clock lines impedance is 50 Ω ±10%, their width is 0,508 mm (20 mil).

Figure 5−1. TSW2000 EVM Layer Construction



Chapter 6

Bill of Materials, Board Layouts, and Schematics

This chapter contains the bill of materials, board layouts, and schematics.

Topic **Page**

6.1 Bill of Materials

Table 6−1. TSW2000 EVM Bill of Materials

Item #	Qty	Mfg/Dist	Part No.	Ref Des	Description	Value
1	2	Newark	39N867	J1, J2	Power supply banana jack	
2	5	Digi-Key	146220−2−ND	J3, J4, J20−J23, J25, J26, J28, J29, J31	AMP 2 x 11 header	0.1” x 0.1” Centers
3	13	Digi-Key	J629−ND	J5−J16, J24	Johnson components SMA connectors	End launch
4	1	Digi-Key	PCS6106CT−ND	C1	SMT tantal capacitor, case D	10 µF
5	1	Digi-Key	P11317CT−ND	C55	SMT tantal capacitor, case C	22 µF
6	2	Sanyo	8TPC33M	C5, C6	SMT ceramic capacitor, case C, low ESR	33 µF
7	13	Digi-Key	PCC1807CT−ND	C21, C23, C34−C38, C45, C62, C68, C70−C72	SMT ceramic capacitor, 0805	1 µF
8	7	Digi-Key	PCC1812CT−ND	C3, C4, C8, C11, C15, C56, C57	SMT ceramic capacitor, 0805	100 nF
9	5	Digi-Key	PCC1911CT−ND	C7, C12−C14, C30	SMT ceramic capacitor, 0603	0.47 µF
10	5	Digi-Key	PCC1731TR−ND	C28, C31, C58−C60	SMT ceramic capacitor, 0402	100 nF
11	34	Digi-Key	PCC1738CT−ND	C2, C9, C16, C18, C19, C22, C24, C27, C32, C39−C44, C49−C54, C61, C63−C67, C69, C73−C78	SMT ceramic capacitor, 0402	10 nF
12	5	Digi-Key	PCC101CQCT−ND	C10, C17, C20, C29, C33	SMT ceramic capacitor, 0402	100 pF
13	3	Digi-Key	ECJ−0EC1H100D	C46−C48	SMT ceramic capacitor, 0402	10 pF
14	1	Digi-Key	P33.2LCT_ND	R71	SMT RES, 0402	33.2 Ω
15	3	Digi-Key	Y7330CT−ND	R2−R4	SMT RES array, 0402x4	33 Ω
16	4	Digi-Key	P49.9LCT_ND	R90, R91, R97, R98	SMT RES, 0402	49.9 Ω
17	5	Digi-Key	P100LCT_ND	R35−R37, R46, R47	SMT RES, 0402	100 Ω
18	10	Digi-Key	P150LCT−ND	R10, R19, R20, R25, R45, R48, R51, R53, R55, R57	SMT RES, 0402	150 Ω
19	1	Digi-Key	P162LCT−ND	R95	SMT RES, 0402	162 Ω
20	5	Digi-Key	P681LCT−ND	R6, R7, R32−R34	SMT RES, 0402	681 Ω
21	1	Digi-Key	P820JCT−ND	R44	SMT RES, 0402	820 Ω
22	1	Digi-Key	P4.75KLCT−ND	R94	SMT RES, 0402	4.75 kΩ
23	23	Digi-Key	P10.0KLCT−ND	R5, R8, R9, R11−R18, R21−R24 R26, R27, R42, R43, R96, R100−R102	SMT RES, 0402	10 kΩ

Table 6−1. TSW2000 EVM Bill of Materials (Continued)

Item #	Qty	Mfg/Dist	Part No.	Ref Des	Description	Value
24	3	Digi-Key	P100KLCT−ND	R38−R40	SMT RES, 0402	100 kΩ
25	2	Digi-Key	P267KLCT_ND	R28, R29	SMT RES, 0402	267 kΩ
26	3	Digi-Key	HZ1206E601R−00	L1, L2, L3	SMT F-Bead, 1206	600 Ω at 100 MHz, 500 mA
27	1	Texas Instruments	TLK1201AIRCP	U1	0.6 to 1.3 Gbps SerDes	DUT
28	1	Texas Instruments	CDC7005ZVAR	U2	Clock synchronizer	DUT
29	1	Toyocom	TCO−2111T6144	U3	VCXO	66.44 MHz, spec# TN4−21509
30	1	Texas Instruments	SN65LVCP22PW	U4	LVPECL crosspoint switch	
31	1	Texas Instruments	SN74LV125AD	U6	Quad bus buffer	
32	1	Texas Instruments	TPS70258PWP	U7	Dual LDO	
33	6	Digi-Key	67−1552−1−ND	U8−U11, U13, U14	SMT LED, 0805	Red
34	1	Digi-Key	CDCV304PW	U12	1:5 clock buffer	
35			Optional termination or biasing resistors	R41, R49, R50, R65−70, R72−74	SMT RES, 0402	See schematics
36	3	N/A	N/A	J17−J19	Solder jumpers	

6.2 Board Layers

Figure 6−1. TSW2000 EVM Layout, Top Silk Layer

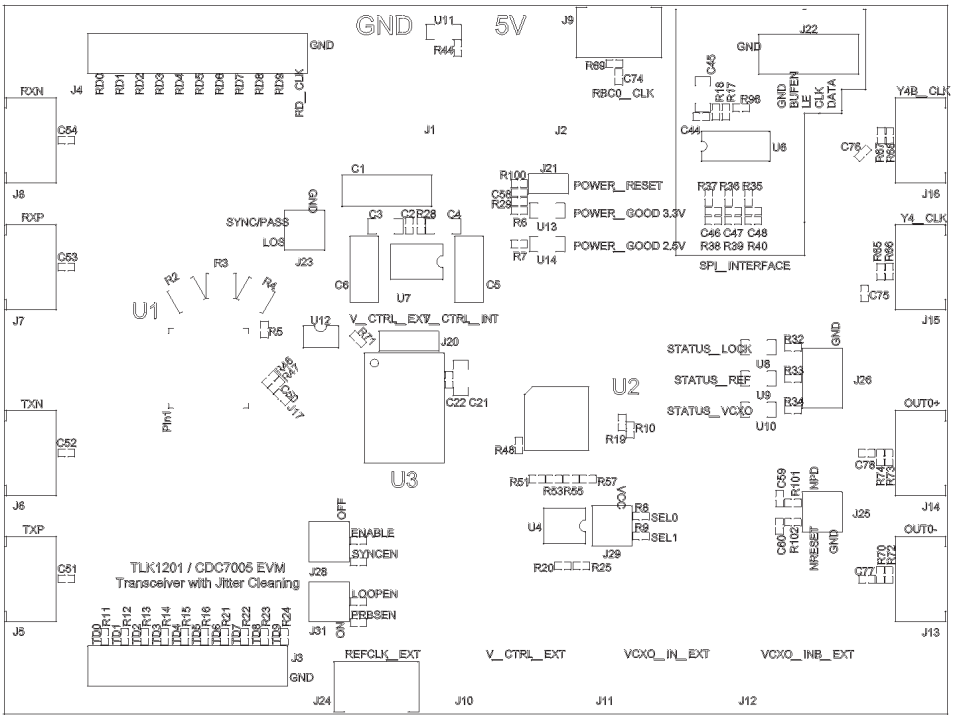


Figure 6−2. TSW2000 EVM Layout, Top Layer (Layer 1)

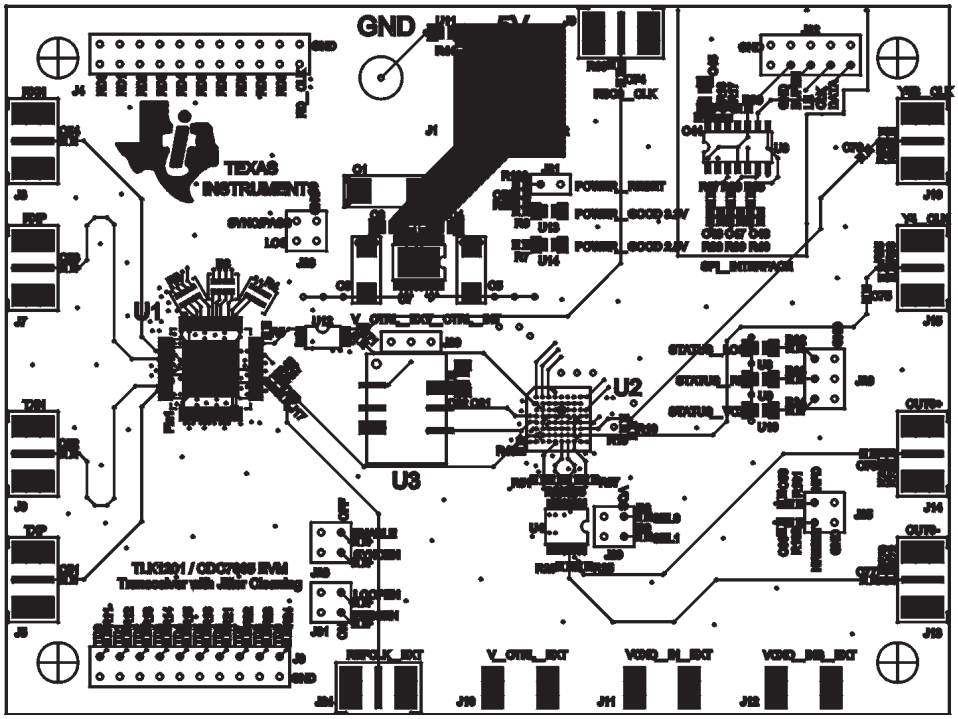


Figure 6−3. TSW2000 EVM Layout, Ground/Power Supply Layers (Layers 2/5, Layer 3)

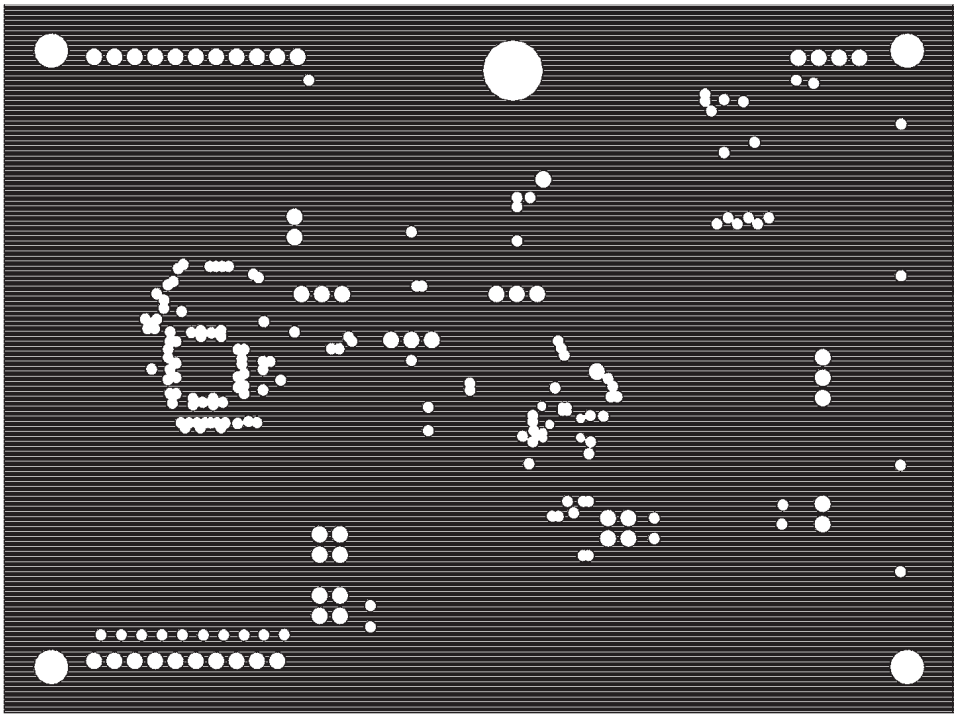


Figure 6−4. TSW2000 EVM Layout, Ground/Power Supply Layers (Layers 2/5, Layer 3)

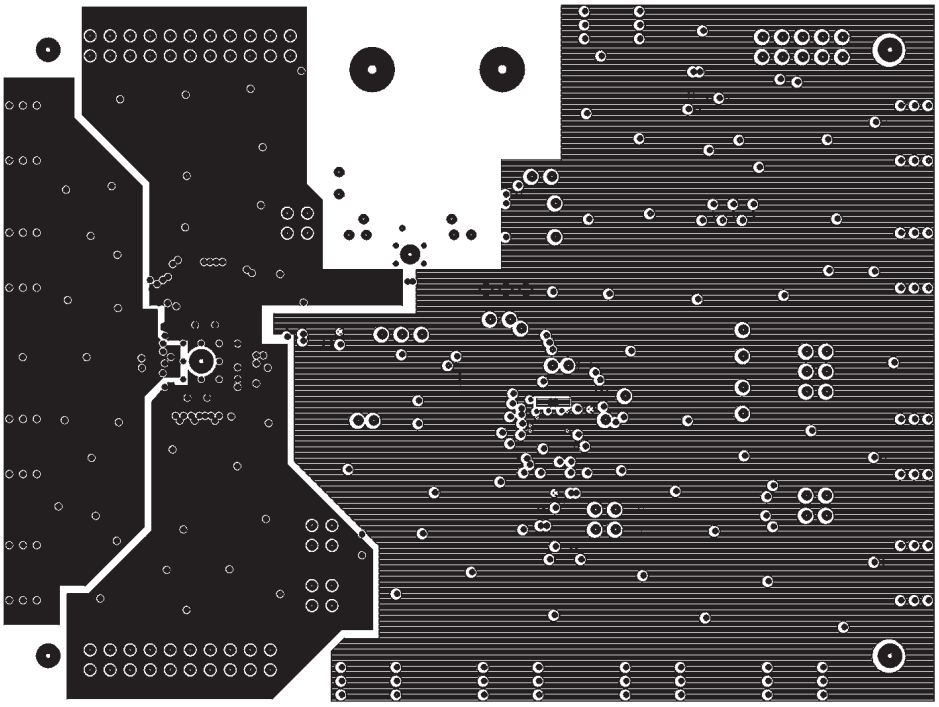


Figure 6−5. TSW2000 EVM Layout, Signal Layer (Layer 4)

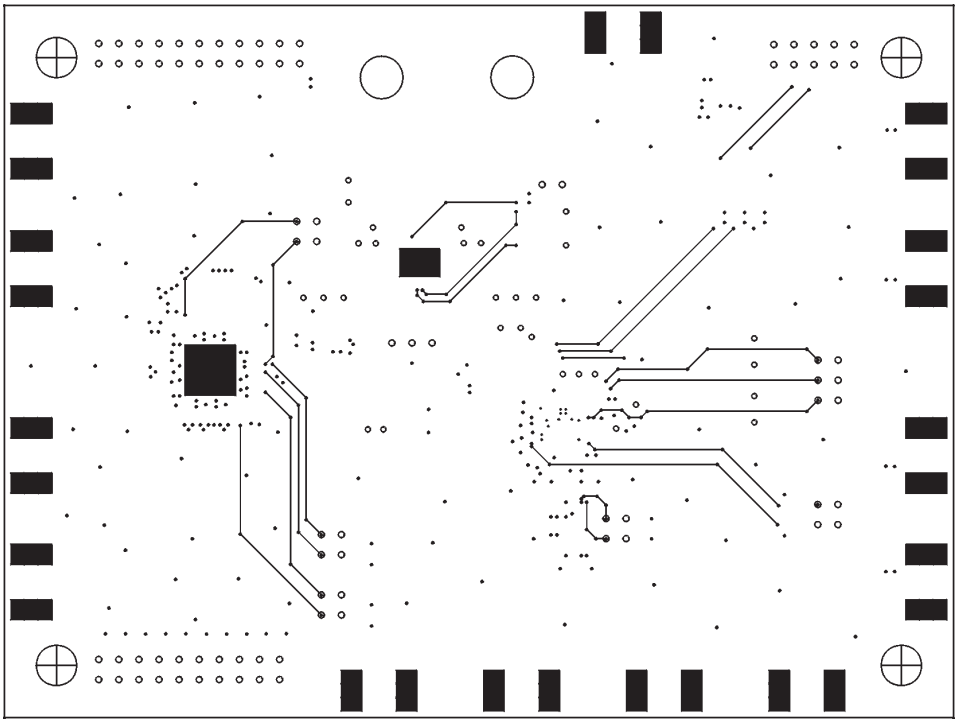


Figure 6−6. TSW2000 EVM Layout, Bottom Layer (Layer 6)

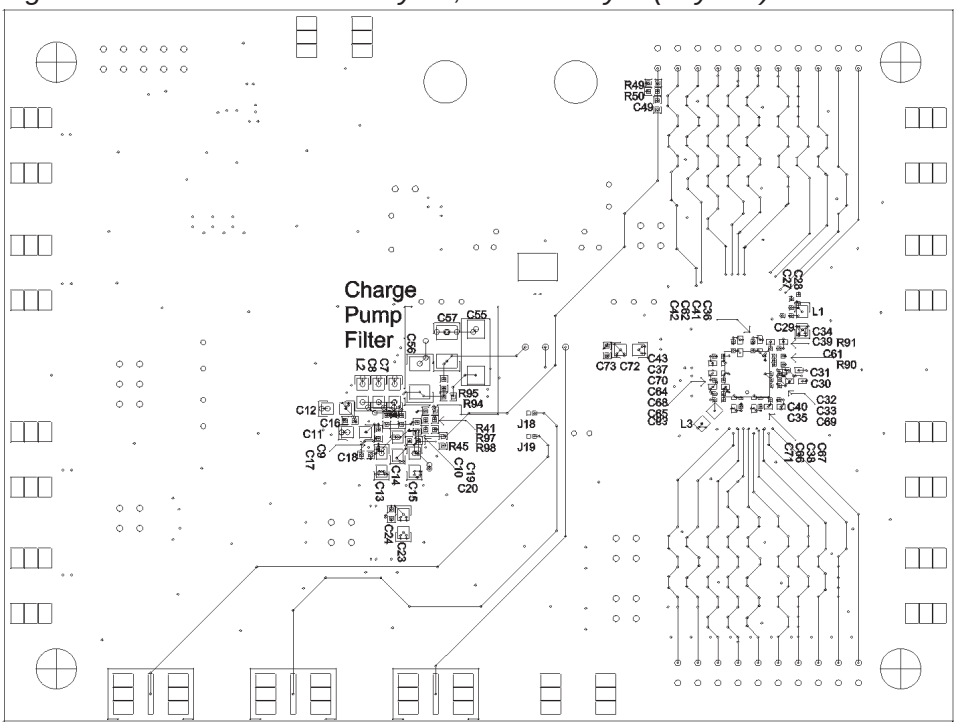
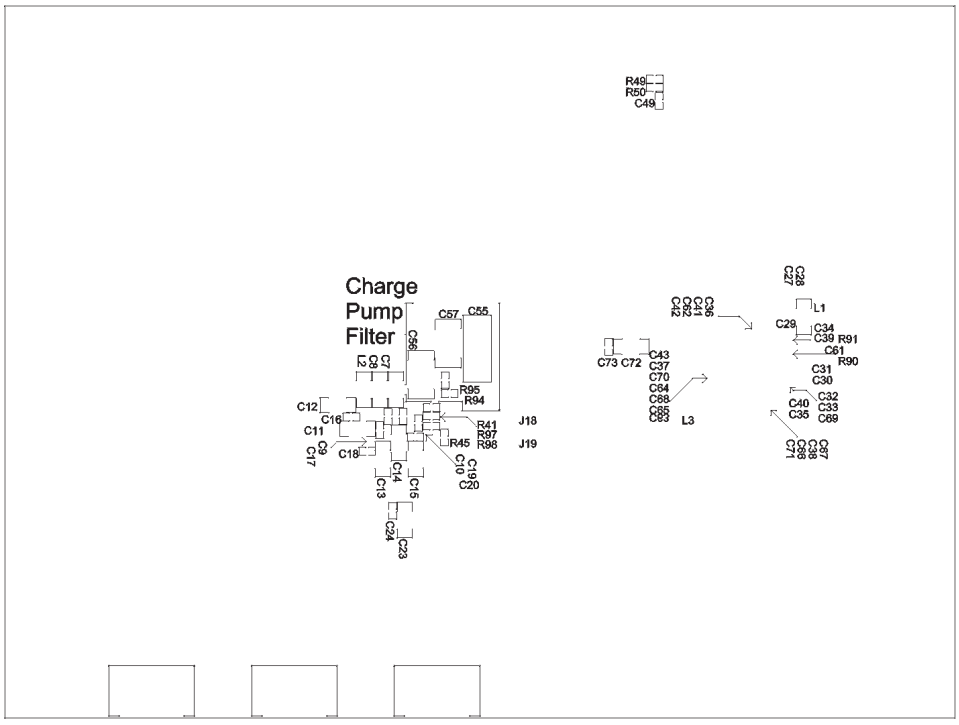


Figure 6−7. TSW2000 EVM Layout, Bottom Silk Layer



6.3 Schematics

Figure 6−8. TSW2000 EVM Schematics, TLK1201 Section

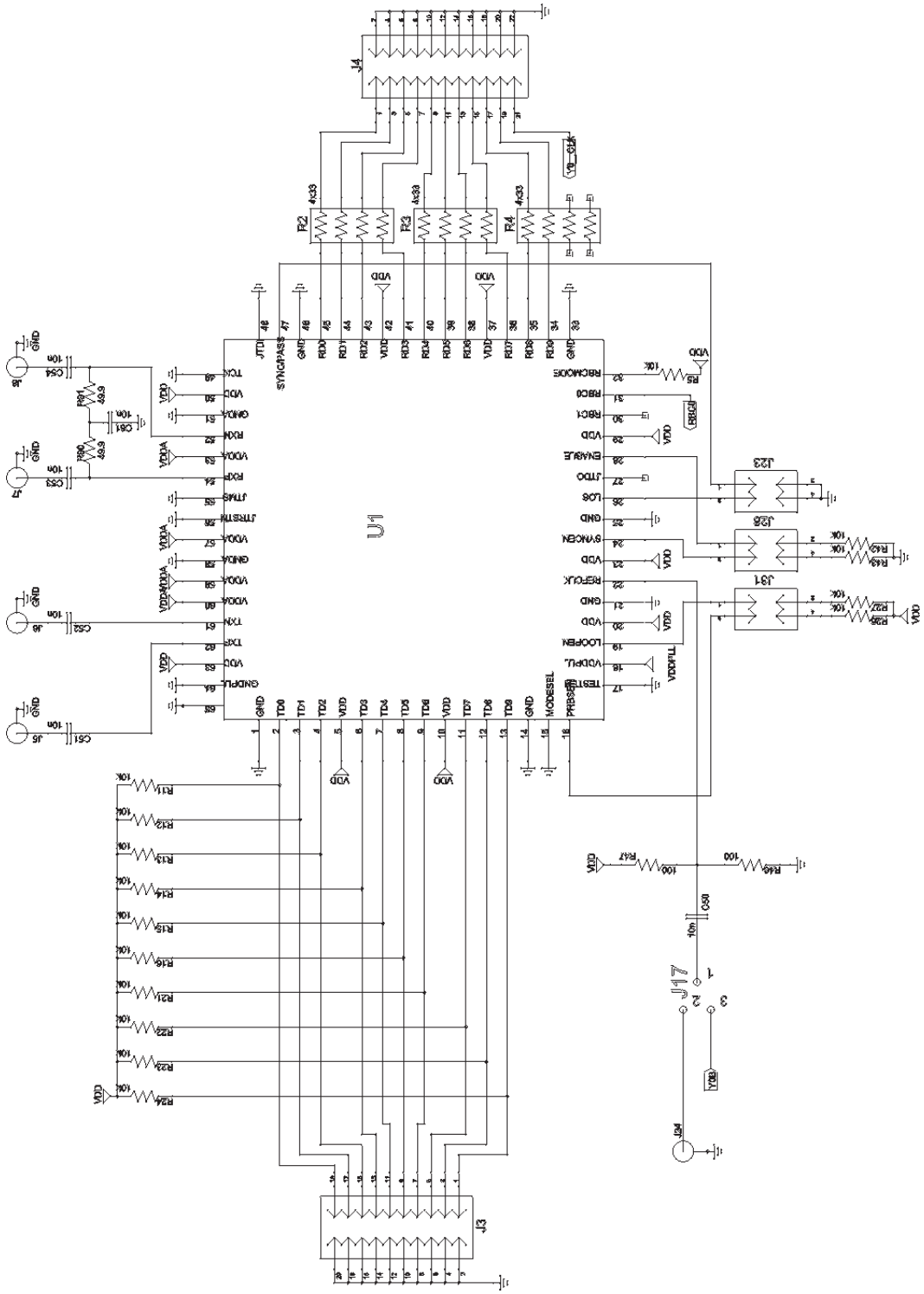


Figure 6−9. TSW2000 EVM Schematics, CDC7005 Section

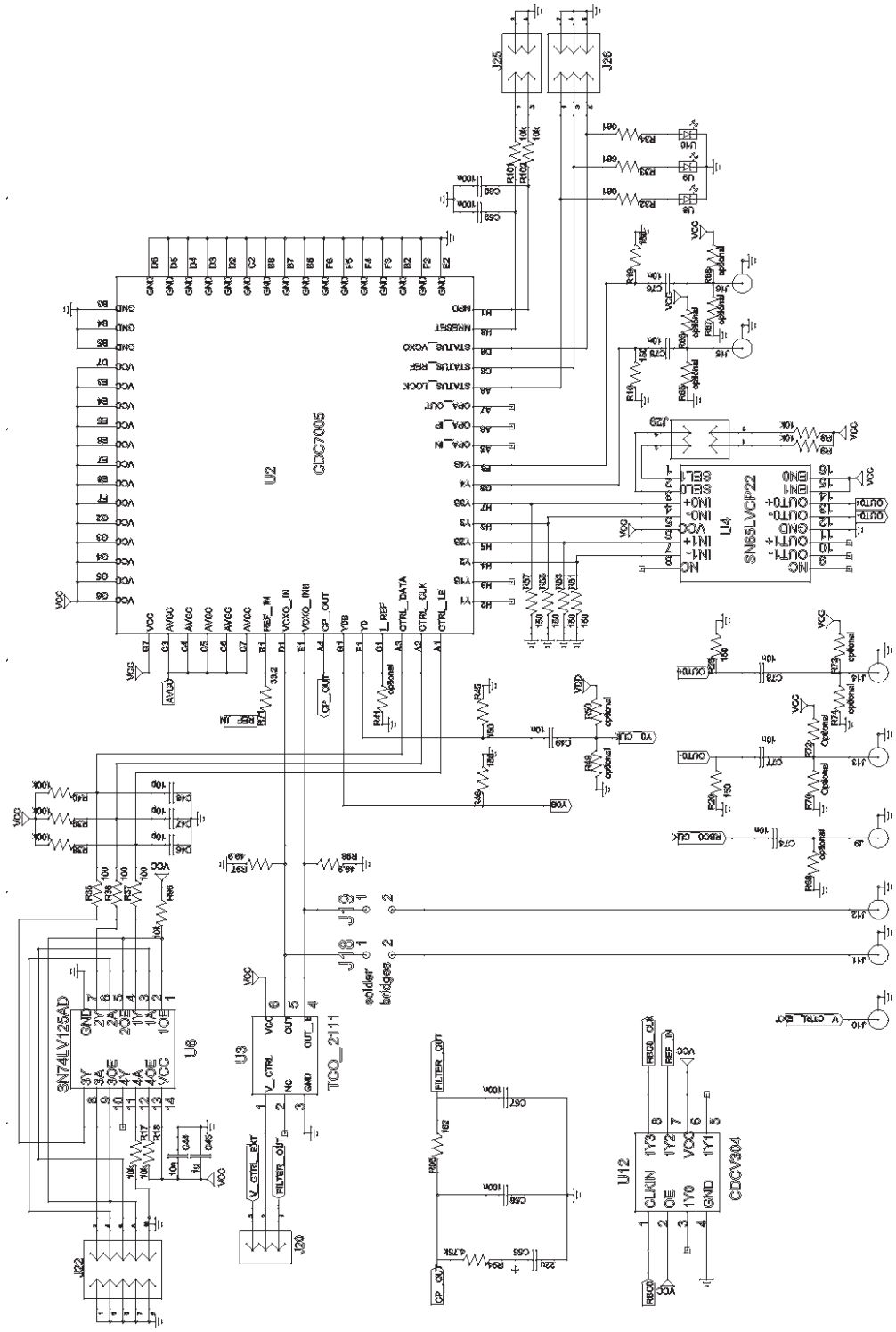


Figure 6−10. TSW2000 EVM Schematics, Power Supply