

CDCM7005EVM-CVAL Evaluation Module (EVM) User's Guide

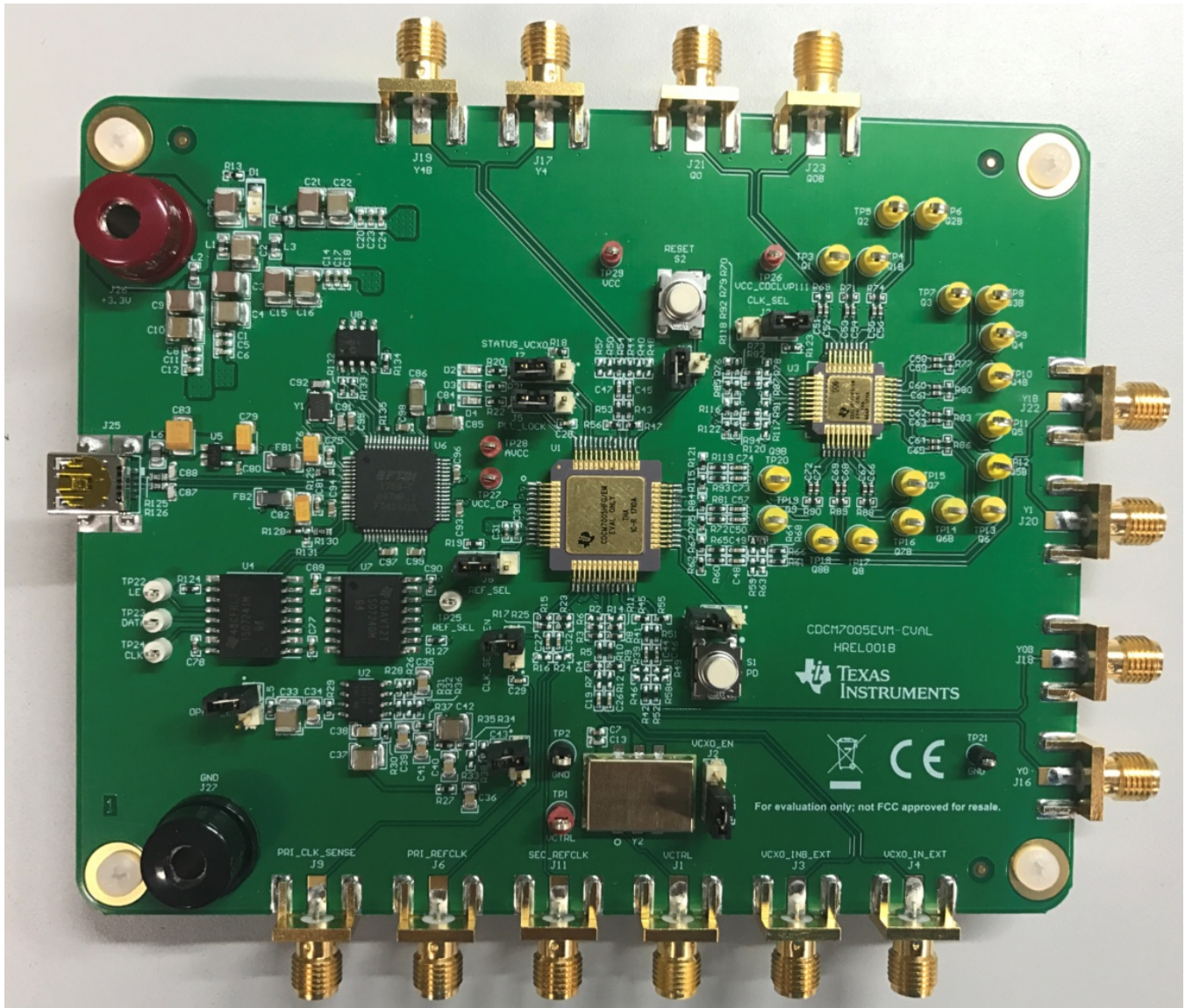


Figure 1. CDCM7005EVM-CVAL

This user's guide provides an overview of the CDCM7005EVM-CVAL evaluation module (EVM) including hardware and software features and functions to be considered while using this module.

1 CDCM7005EVM-CVAL Overview

The CDCM7005-SP is a high-performance, low phase noise and low skew clock synchronizer that synchronizes an on-board voltage controlled crystal oscillator (VCXO) frequency to an external reference clock. The device operates up to 2 GHz. The PLL loop bandwidth and damping factor can be adjusted to meet different system requirements by selecting the external VCXO, loop filter components, frequency for PFD, and charge pump current. Each of the five differential LVPECL and five LVCMOS pair outputs can be programmed by a serial peripheral interface (SPI). The SPI allows individual control of the frequency and enable/disable state of each output. As the system requires external components like a loop filter and VC(X)O, this EVM provides an easy method to evaluate and modify the performance and parameters of the clock system in conjunction with the specific customer application. Loop bandwidth can be selected as low as 10 Hz or less, allowing the device to clean the system's clock jitter. In non PLL mode, the CDCM7005 can be used as a simple LVPECL or LVCMOS buffer with divider options.

In series with two of the CDCM7005-SP(**U1**) outputs is the CDCLVP111-SP (**U3**), a radiation hardened, low-voltage 1:10 LVPECL clock distributor. This allows measurement comparisons between the CDCM7005-SP and CDCM7005-SP + CDCLVP111-SP so that additive noise of the cascaded clock generation path can be analyzed.

2 CDCM7005-SP Software GUI Installation

Download the GUI installer, sglc002.zip from the product web page.

Unzip the installer and launch the executable and follow all instructions. Refer to Appendix A for detailed software installation instructions.

3 CDCM7005EVM-CVAL Setup and Quick Test

This section provides the minimum procedures required to begin testing the device in a phase locked configuration using the on-chip PLL. Please refer to subsequent sections of this guide for more details on EVM and GUI features.

Figure 2 illustrates the necessary hardware connections to begin testing.

1. Connect USB-to-micro-USB cable between PC and CDCM7005EVM-CVAL at port **J25**.
2. Provide power to the CDCM7005EVM-CVAL by providing +3.3V DC between **J27**, **GND**, and **J26**, **+3.3V**. LEDs **D1** and **D2** will illuminate when power is provided to the EVM.
3. Provide reference signal to **J6**, **PRI_REFCLK** of CDCM7005EVM-CVAL. LED **D3** should illuminate indicating the detection of a reference signal and LED **D4** should illuminate indicating that the PLL has successfully phased locked this reference signal to the on-board VCXO, **Y2**.
 - a. Frequency = 61.44 MHz
 - b. Amplitude ≥ 400 mVpp-se
4. Connect instrumentation balun (i.e. Picosecond 5310A) to convert differential output (**Y0**, **J16** and **Y0B**, **J18**) to single ended input of measurement instrument (i.e. spectrum analyzer, phase noise analyzer, oscilloscope). [Note: If only device functionality is being testing and not specified performance, one can connect one of the differential outputs to an instrument (with 50- Ω input termination) and the other unused output with 50- Ω termination.]

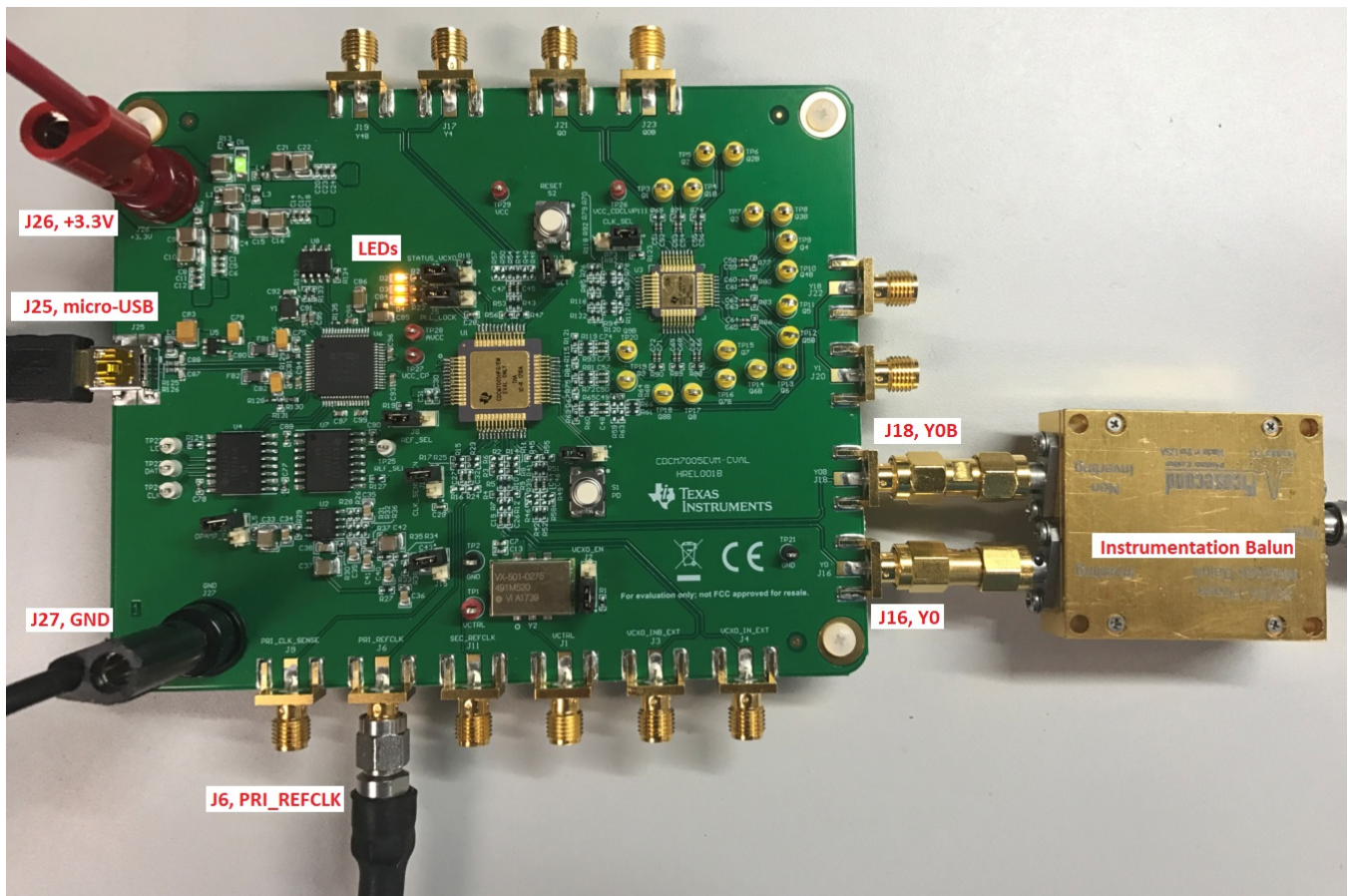


Figure 2. CDCM7005EVM-CVAL Setup

Since the power on reset default state of the CDCM7005-SP configures the device such that the PLL will phase lock the on-board VCXO, **Y2**, 491.52 MHz, to the input reference of 61.44 MHz, and provide a VCXO/8 output signal at 61.44 MHz, no software GUI is required to complete this test and confirm functionality of the hardware.

[Note: It is observed that the disable pin for the on-board VCXO, **Y2**, does not fully disable this oscillator and, when invoked, the 2nd harmonic of the VCXO, 983.04-MHz signal, is strong enough in amplitude that the CDCM7005-SP detects signal as a valid VCXO input signal as indicated by LED **D2**, **VCXO STATUS**, always being lit regardless of the position of **J2**, **VCXO_EN**. In fact, the PLL can lock to this 2nd harmonic if the input reference signal is changed from 61.44 MHz to 122.88 MHz.]

To measure cascaded performance of the CDCM7005-SP and CDCLVP111-SP move the instrumentation balun from **Y0/Y0B** port to **Q0/Q0B** port at designators **J21** and **J23**, respectively, as shown in [Figure 3](#).

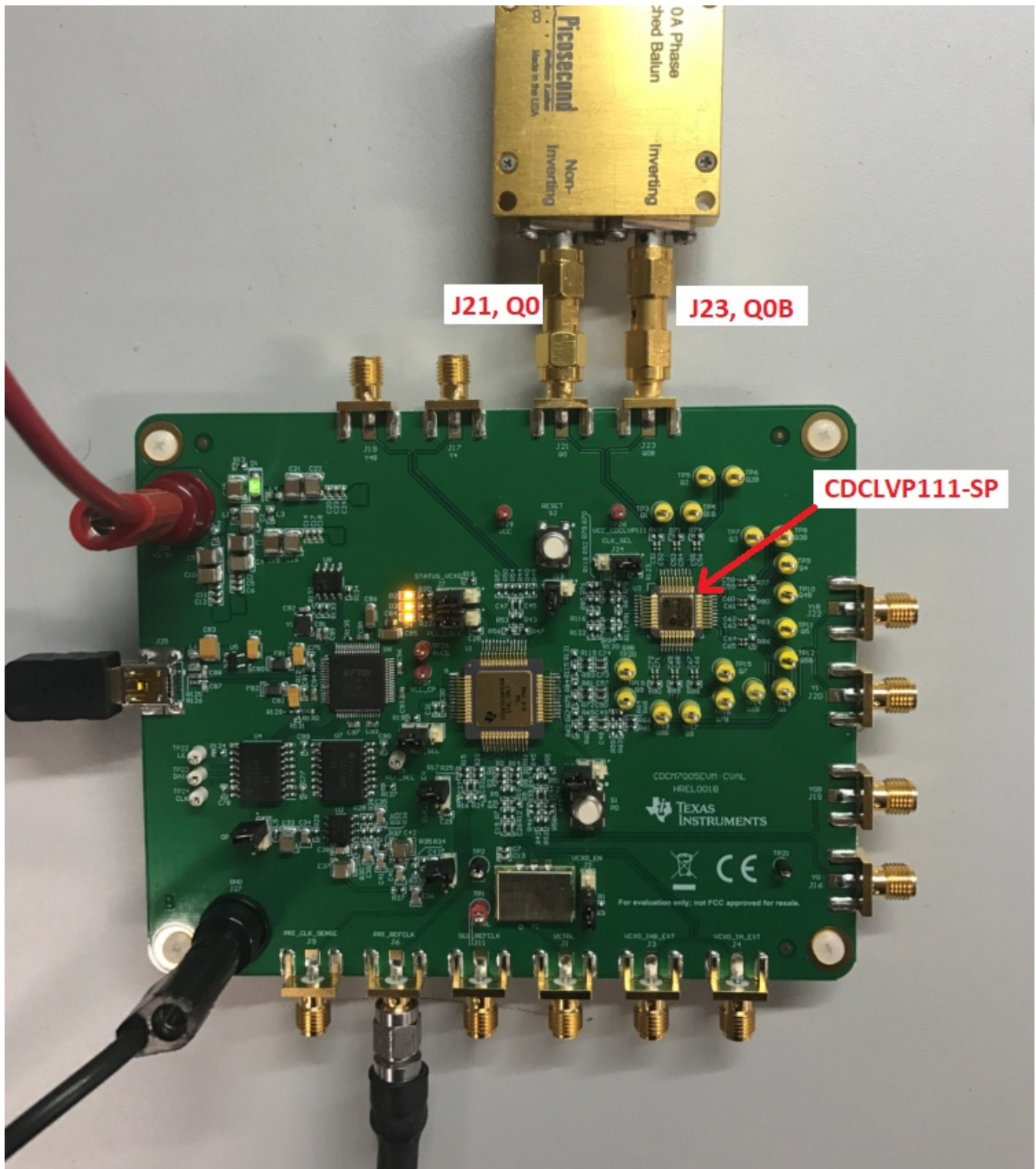


Figure 3. Measuring CDCM7005-SP + CDCLVP111-SP

4 CDCM7005EVM-CVAL EVM Detailed Description

The following sub-sections describe the CDCM7005EVM-CVAL EVM in detail.

4.1 CDCM7005EVM-CVAL Content

Figure 4 below shows the active components used on the CDCM7005EVM-CVAL.

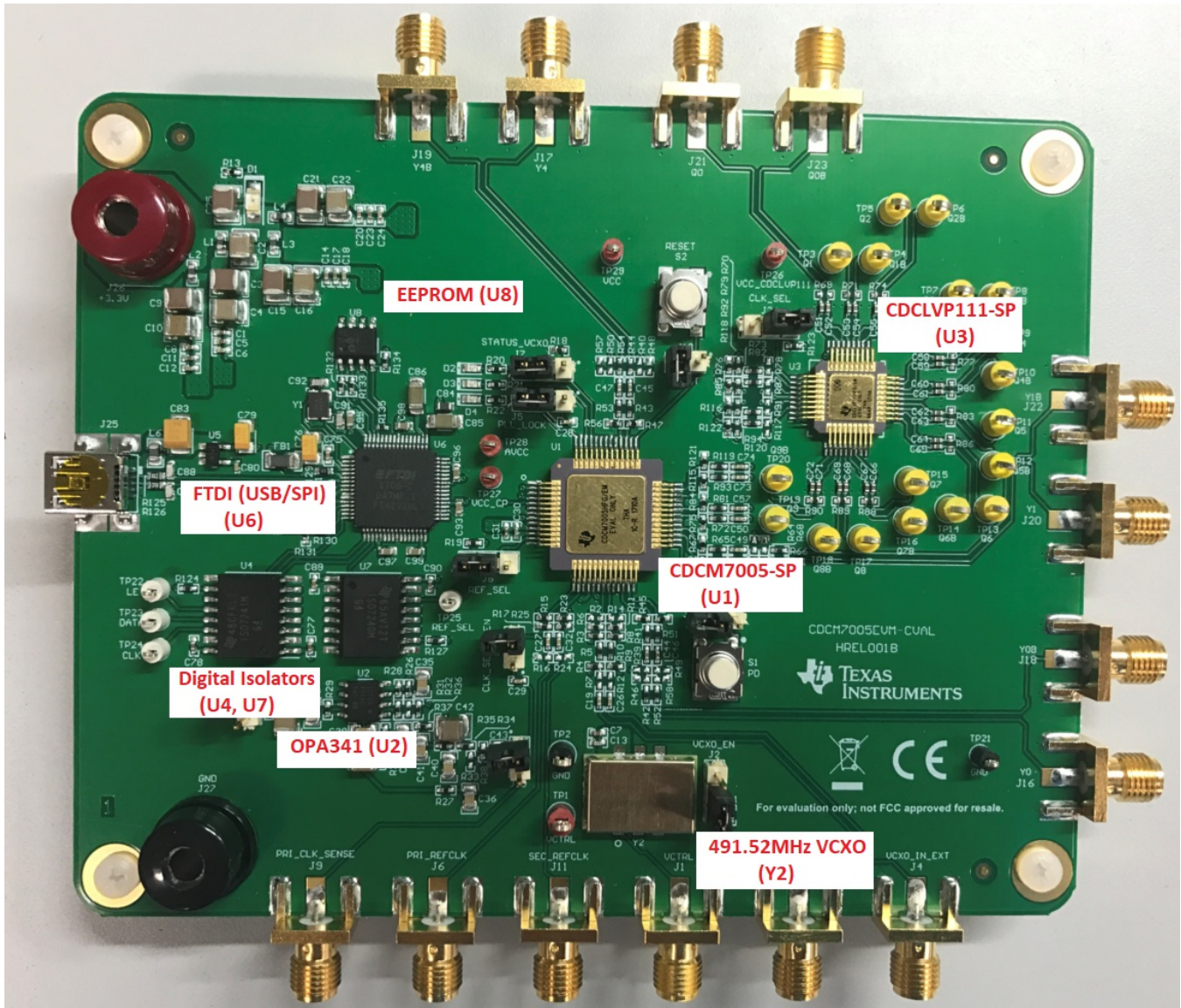


Figure 4. CDCM7005EVM-CVAL Content

4.2 CDCM7005EVM-CVAL EVM Jumpers and Test Points

Table 1 describes the jumpers on the CDCM7005EVM-CVAL.

Table 1. CDCM7005EVM-CVAL Header Descriptions

REF Designator	Jumper Name	Default Config	Description
J2	VCXO_EN	Short pins 1-2	Power Supply for VCXO
J5	PLL_LOCK	Short pins 2-3	(1-2) LOCK signal routed to cap C28 (2-3) LOCK signal routed to LED D4
J7	STATUS_VCXO	Short pins 2-3	(1-2) Signal routed to resistor R18 (2-3) Signal routed to LED D3
J8	REF_SEL	Short pins 1-2	(1-2) VCC enables PRI_REF input (2-3) GND enables SEC_REF input
J10	CLK_SENSE_EN	Open	Output path to monitor primary reference clock source
J12	PD	Open	(OPEN) Powerdown OFF (~763 mA) (1-2) Powerdown ON (~534 mA)
J13	RESET	Open	Resets Device and SPI to default configuration
J14	OPAMP_EN	Open	(OPEN) Powerdown opamp (1-2) Powers ON opamp
J15	n/a	Open	Shorts capacitor C43
J24	CLK_SEL (CDCLVP111-SP)	Short pins 1-2	(1-2) VCC enables PRI_REF input (2-3) GND enables SEC_REF input

4.3 CDCM7005EVM-CVAL Test Points

Table 2 lists all test points on the CDCM7005EVM-CVAL EVM.

Table 2. CDCM7005EVM-CVAL Test Points Description

Test Point	Color	Silkscreen	Schematic Page	Description
TP1	RED	VCTRL	CDCM7005-SP.SchDoc	Control Voltage for on-board VCXO (loop filter output).
TP2	BLACK	GND	CDCLVP111-SP.SchDoc	Ground connection.
TP3	YELLOW	Q1	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 1.
TP4	YELLOW	Q1B	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 1 Complementary.
TP5	YELLOW	Q2	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 2.
TP6	YELLOW	Q2B	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 2 Complementary.
TP7	YELLOW	Q3	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 3.
TP8	YELLOW	Q3B	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 3 Complementary.
TP9	YELLOW	Q4	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 4.
TP10	YELLOW	Q4B	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 4 Complementary.
TP11	YELLOW	Q5	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 5.
TP12	YELLOW	Q5B	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 5 Complementary.
TP13	YELLOW	Q6	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 6.
TP14	YELLOW	Q6B	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 6 Complementary.
TP15	YELLOW	Q7	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 7.
TP16	YELLOW	Q7B	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 7 Complementary.
TP17	YELLOW	Q8	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 8.
TP18	YELLOW	Q8B	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 8 Complementary.
TP19	YELLOW	Q9	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 9.
TP20	YELLOW	Q9B	CDCLVP111-SP.SchDoc	CDCLVP111-SP Output 9 Complementary.
TP21	BLACK	GND	USB_FTDI.SchDoc	Ground connection.

Table 2. CDCM7005EVM-CVAL Test Points Description (continued)

Test Point	Color	Silkscreen	Schematic Page	Description
TP22	WHITE	LE	USB_FTDI.SchDoc	Serial interface latch enable signal.
TP23	WHITE	DATA	USB_FTDI.SchDoc	Serial interface data signal.
TP24	WHITE	CLK	USB_FTDI.SchDoc	Serial interface clock signal.
TP25	WHITE	REF_SEL	USB_FTDI.SchDoc	Not used. Floating test point.
TP26	RED	VCC_CDCLVP111	CDCM7005-SP.SchDoc	Power supply to CDLVP111-SP device.
TP27	RED	VCC_CP	CDCM7005-SP.SchDoc	CDCM7005-SP pin 10 charge pump power supply.
TP28	RED	AVCC	CDCM7005-SP.SchDoc	CDCM7005-SP analog power supply (pins 3, 6, 9, 16, 17).
TP29	RED	VCC	CDCM7005-SP.SchDoc	CDCM7005-SP power supply (pins 19, 22, 23, 26, 28, 31, 32, 35, 36, 39, 41, 44, 46, 47, 48).

4.4 CDCM7005EVM-CVAL Switches and LED Indicators

The EVM contains two switches: (1) **SW1, PD**, and (2) **SW2, RESET**. Press and hold **SW1** to enter a power down state of the CDCM7005-SP at which time all current sources internal to the device are switched off, all outputs are switched into tri-state, and all dividers (M, N, and P) are reset to the default state. The total EVM current will drop from ~753 mA to ~530 mA in the power down state as the EVM is still powering the CDCLVP111-SP, the VCXO, and other peripheral devices such as the FDTI.

Press and hold **SW2** to enter RESET mode of the CDCM7005-SP in which case the charge pump is tri-stated and all the counters, N, M and P, are held to zero. RESET mode does not erase divider settings which a maintained after RESET.

The three status outputs of the CDCM7005 are fed to LED indicators. **D1** lit indicates power is being supplied to the EVM. **D2** on indicates a valid reference input clock signal. **D3** is on if the VC(X)O input clock is valid and **D4** turns on if the PLL has been locked.

4.5 CDCM7005EVM-CVAL Loop Filter Options

The loop filter is one of the key elements determining the loop bandwidth of the PLL. The loop filter converts the charge pump current into the control voltage for the voltage controlled oscillator. The phase difference between the input clocks of the phase frequency detector determines the width of the charge pump output current pulses. These high frequency pulses are transformed into a voltage to control the oscillator. The control voltage of the VC(X)O can be measured at **TP1, VCTRL**.

There are two types of loop filters available on the EVM: (1) External passive loop filter (default configuration) and (2) external active loop filter using an external low-noise OPA. Filter types can be selected by soldering in/out resistors **R32, R33, R34, R36** (see [Table 3](#)). If external active loop filter is desired, jumper **J14** need to be installed so that power is provided to the OPA341 amplifier.

Table 3. CDCM7005EVM-CVAL Passive vs Active Loop Filter

—	R32	R33	R34	R36	J14
Passive Filter	DNI	DNI	INSTALLED	INSTALLED	OPEN
Active Filter	INSTALLED	INSTALLED	DNI	DNI	SHORT

The passive loop filter is a second order filter (two poles, one zero). The zero is required for the overall loop stability. **R1**, **C1**, and **C2** generate the dominant pole of the system. A second pole is introduced by **R2** and **C3**.

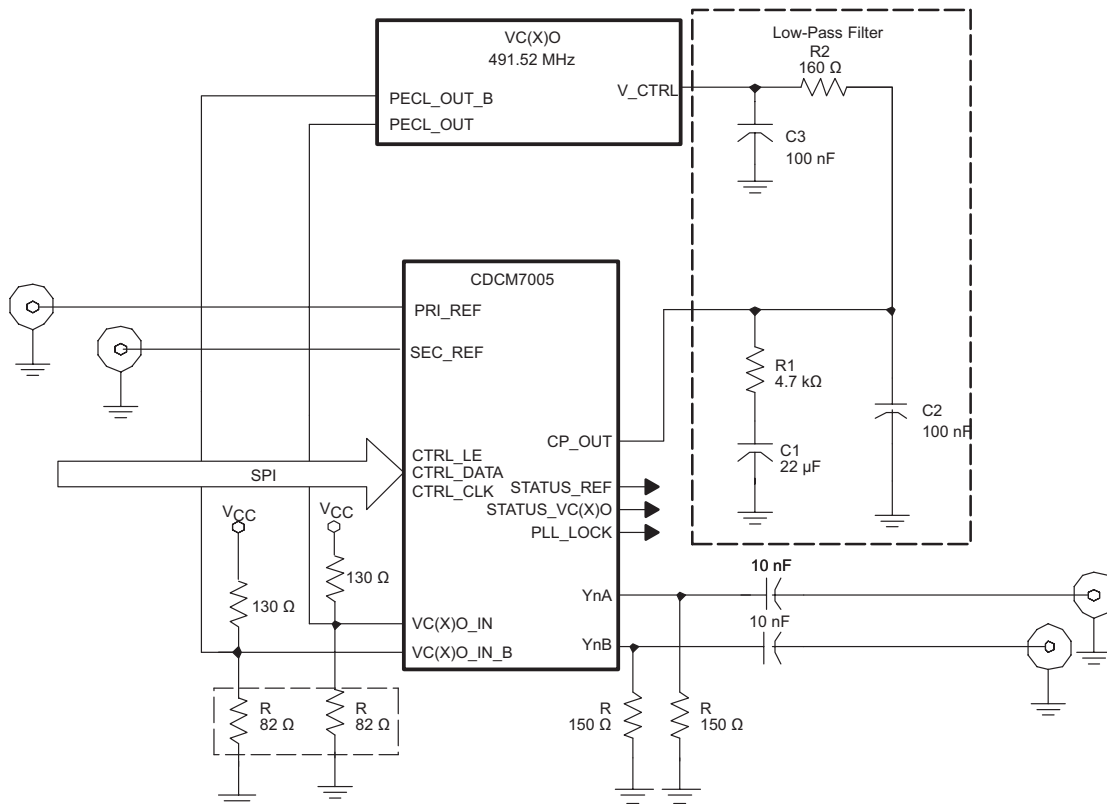


Figure 5. CDCM7005EVM-CVAL Passive Loop Filter

The external active loop filter using OPA341 is shown in [Figure 6](#).

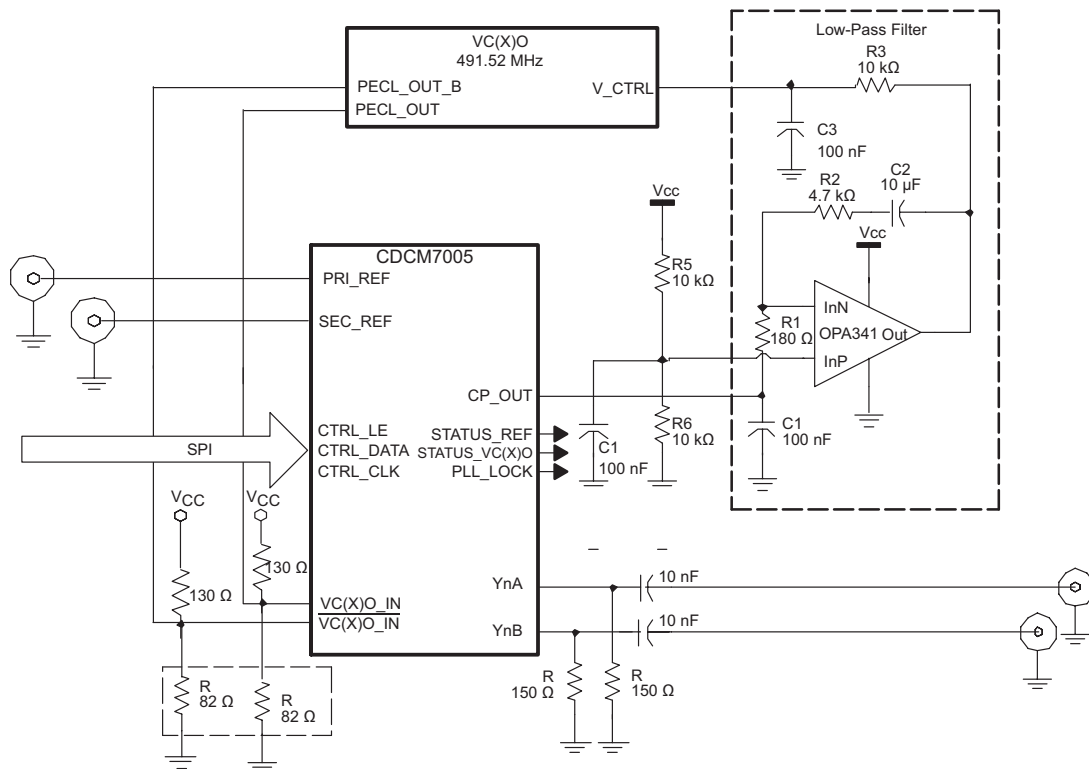


Figure 6. CDCM7005EVM-CVAL Active Loop Filter

4.6 CDCM7005EVM-CVAL AC Coupling PRI_REF(J6) and SEC_REF (J11)

AC-coupling is provided at **J6**, **PRI_REFCLK** and **J11**, **SEC_REFCLK** to ease the use of the CDCM7005-SP with different signaling levels (LVCMOS, LVPECL, LVDS). However, the ac-coupling can increase the PLL stabilization time after power up due to transient effects. It can also increase the switching time between **PRI_REFCLK** and **SEC_REFCLK** in case of automatic reference clock switching. Therefore, the ac-coupling capacitors must be removed for optimized system performance (**C27** and **C32** should be replaced with a 0-Ω resistors and **R15**, **R17**, **R23**, and **R25** should be removed).

4.7 CDCM7005EVM-CVAL VCXO Inputs and Outputs

The CDCM7005-SP requires an external VC(X)O in order to complete the PLL loop. The VC(X)O adjusts the frequency and phase depending on the control voltage level coming from the loop filter and provides the input clock to the LVPECL block. In lieu of the on-board VCXO, an external oscillator can be used by using **J1**, **VCTRL**, as the control voltage from the loop filter and providing the input signals to **J4**, **VCXO_IN_EXT** and **J3**, **VCXO_INB_EXT**. If this option is used, 0-Ω resistors **R4** and **R9** must be moved to **R7** and **R12** positions.

4.8 CDCM7005EVM-CVAL High Speed Inputs/Outputs

The CDCM7005-SP drives five differential LVPECL outputs. All PECL outputs are ac-coupled and terminated with 150 Ω to GND which simplifies the power supply scheme from a conventional LVPECL termination which provides $V_{CC} - 2\text{ V}$ as a termination voltage. The trace impedance of the device outputs are all 50 Ω with differential traces matched in length. All outputs have unpopulated options for pull-up and pull-down resistors. When powered, the CDCM7005-SP defaults to five LVPECL outputs all enabled in divide-by-8 mode.

The reference input clock signal can be applied to **J1, PRI_REFCLK**, or **J6, SEC_REFCLK**. The reference input clock signal can be sensed at **J9, PRI_CLK_SENSE** when jumper **J10, CLK_SENSE_EN** is shorted. The reference input clock sense line is matched to the LVPECL outputs line to avoid any additional delay offset and this output is ac-coupled with **C29**.

5 CDCM7005EVM-CVAL GUI Software in Detail

The CDCM7005EVM-CVAL GUI software will show a green indicator with **CONNECTED** in the status bar at bottom right when the GUI has successfully communicated with an EVM, as shown in [Figure 7](#).

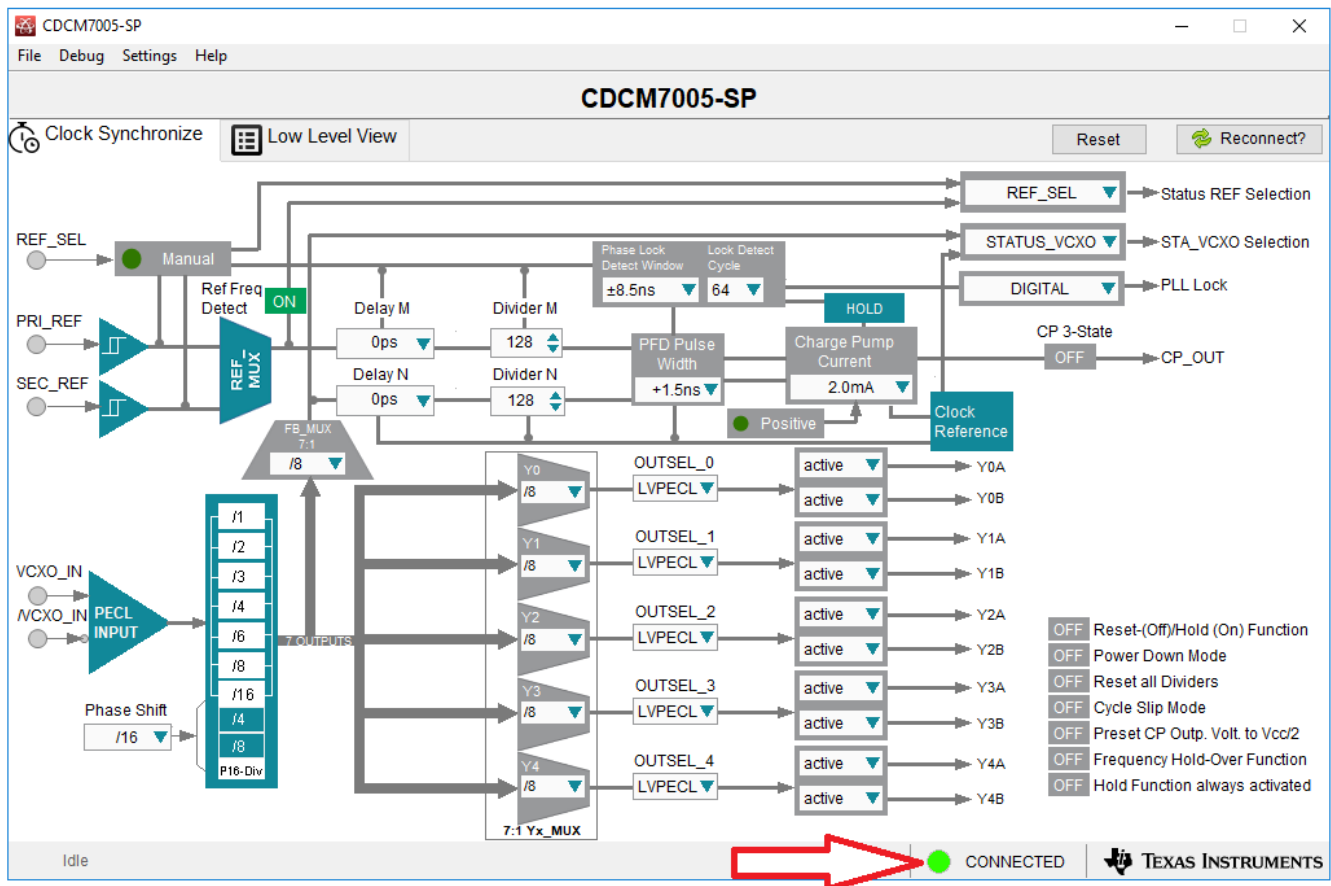


Figure 7. CDCM7005EVM-CVAL USB Connected

If the GUI is launched without a valid USB connection to the PC, an error message will appear asking user to **Continue in Simulation** mode or to **Reconnect FTDI?**

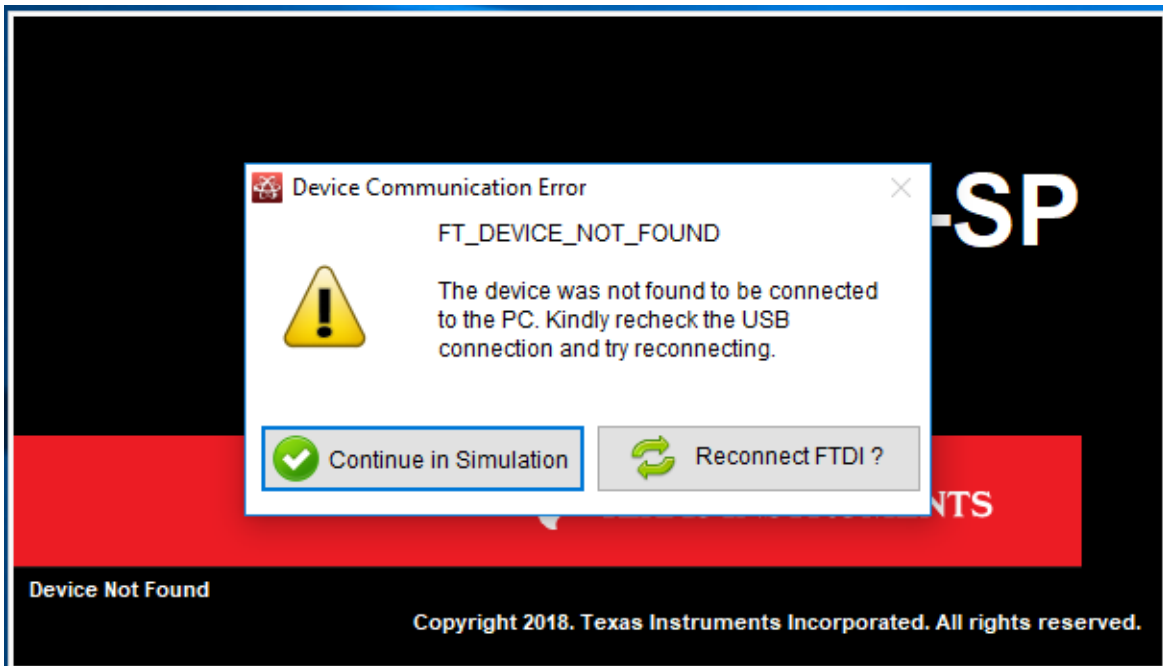


Figure 8. CDCM7005EVM-CVAL Error With No USB Connection

If using simulation mode, the GUI status indicator will reflect this as shown in Figure 9. Simulation mode can be used to become familiar with the interdependencies of some of the controls in the absence of hardware.

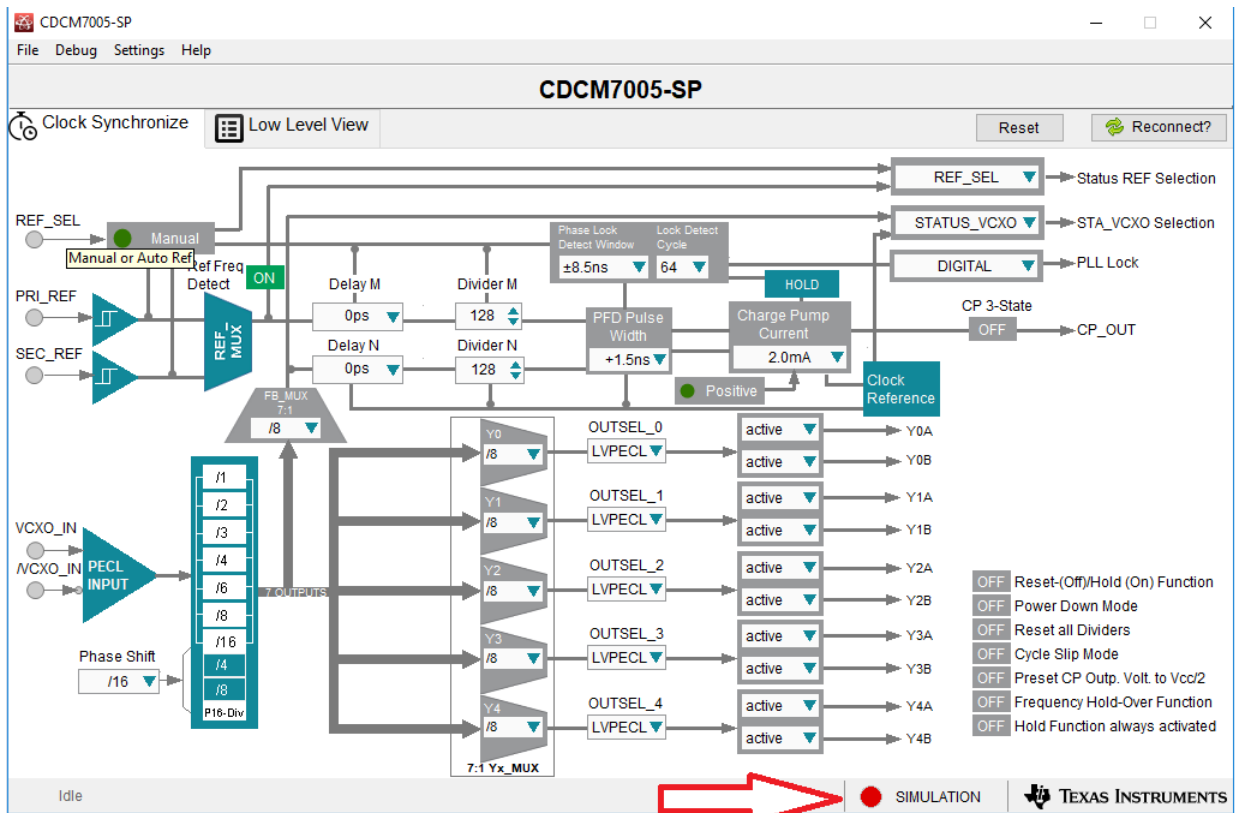


Figure 9. CDCM7005EVM-CVAL Simulation Mode

6 CDCM7005EVM-CVAL EVM Schematic

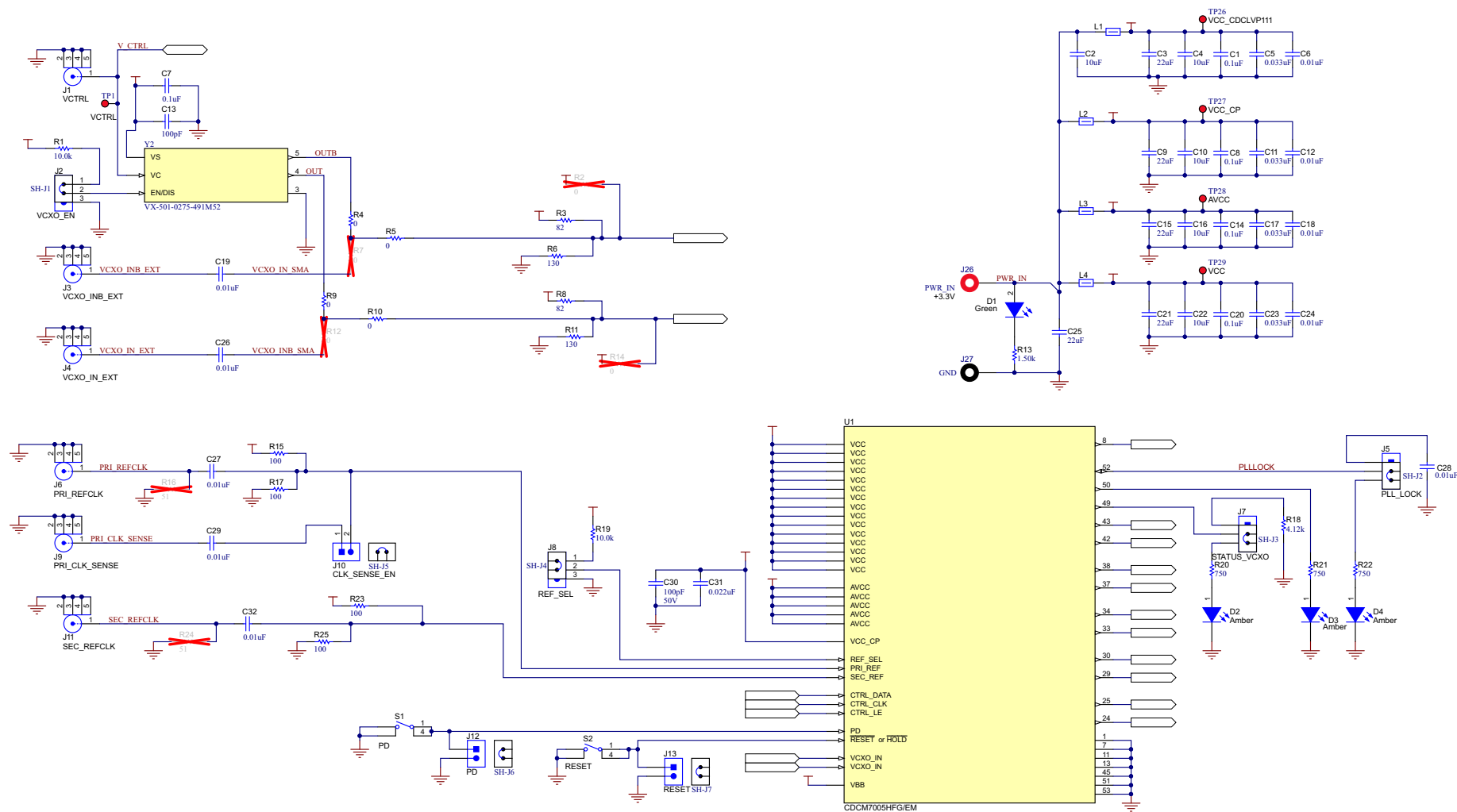
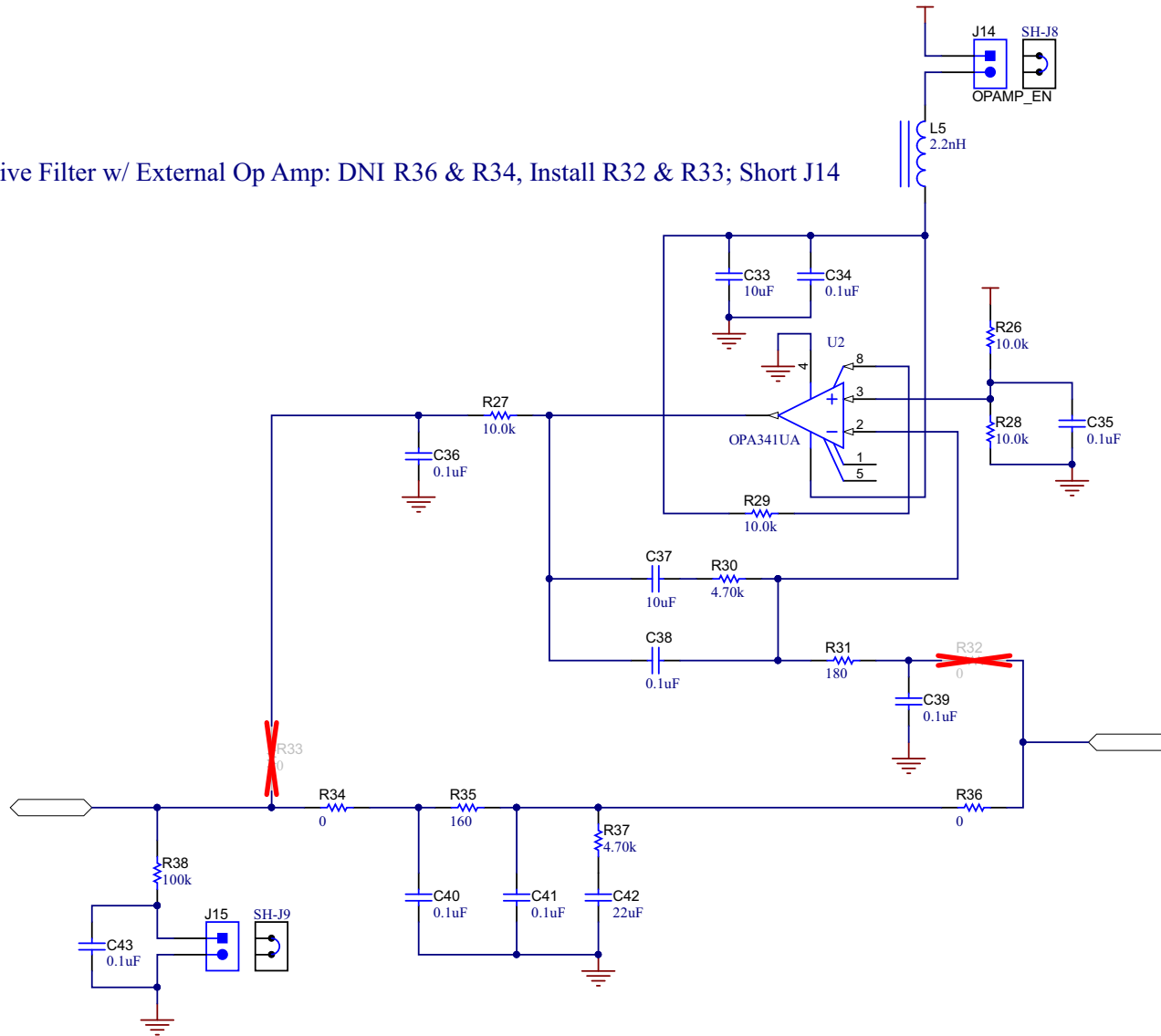


Figure 10. CDCM7005EVM-CVAL Schematic CDCM7005-SP

Active Filter w/ External Op Amp: DNI R36 & R34, Install R32 & R33; Short J14



Passive Filter (Default Setting) : DNI R32 & R33, Install R36 & R34; Open J14

Figure 11. CDCM7005EVM-CVAL Schematic Loop Filter

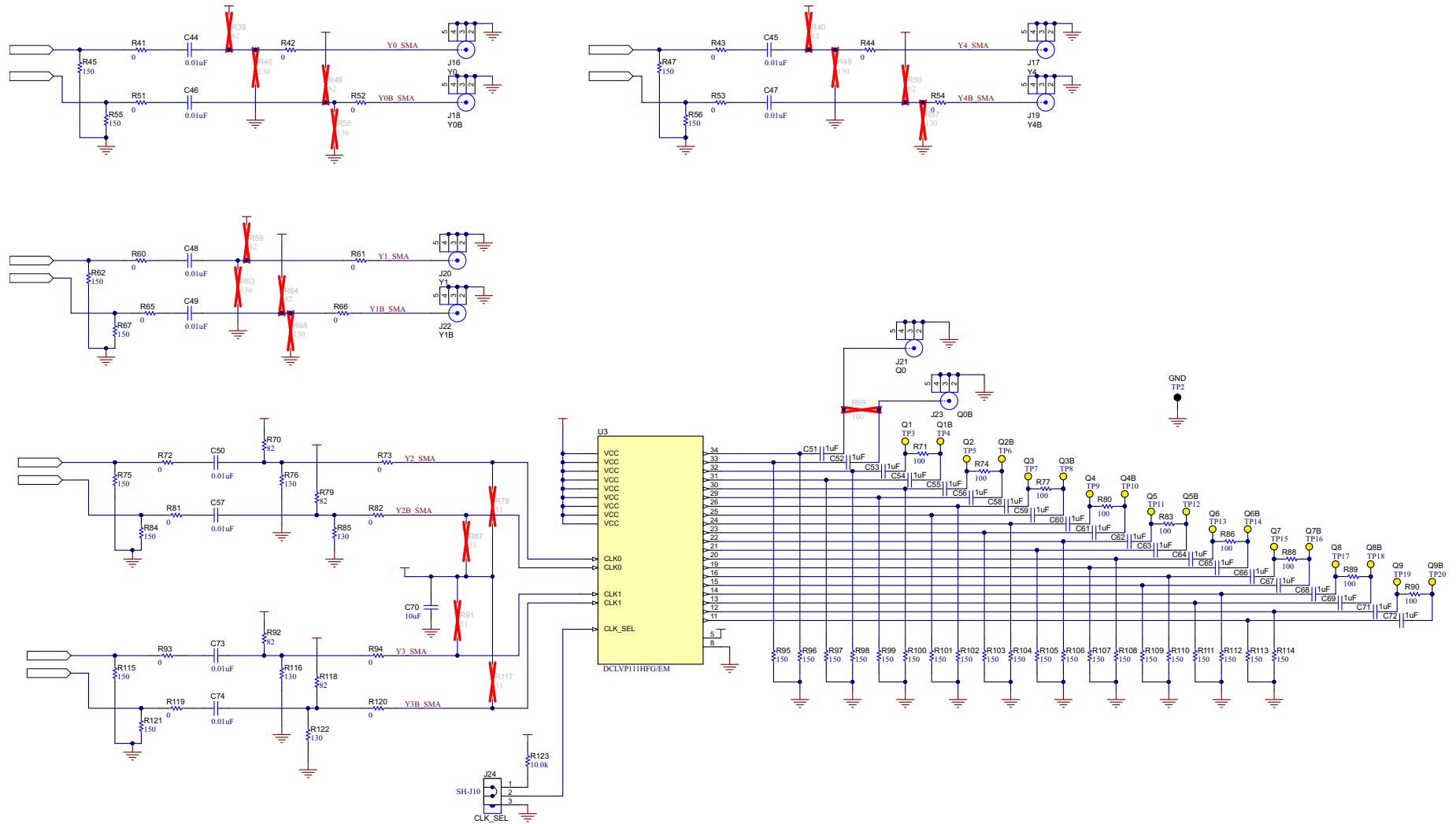


Figure 12. CDCM7005EVM-CVAL Schematic CDCLVP111-SP

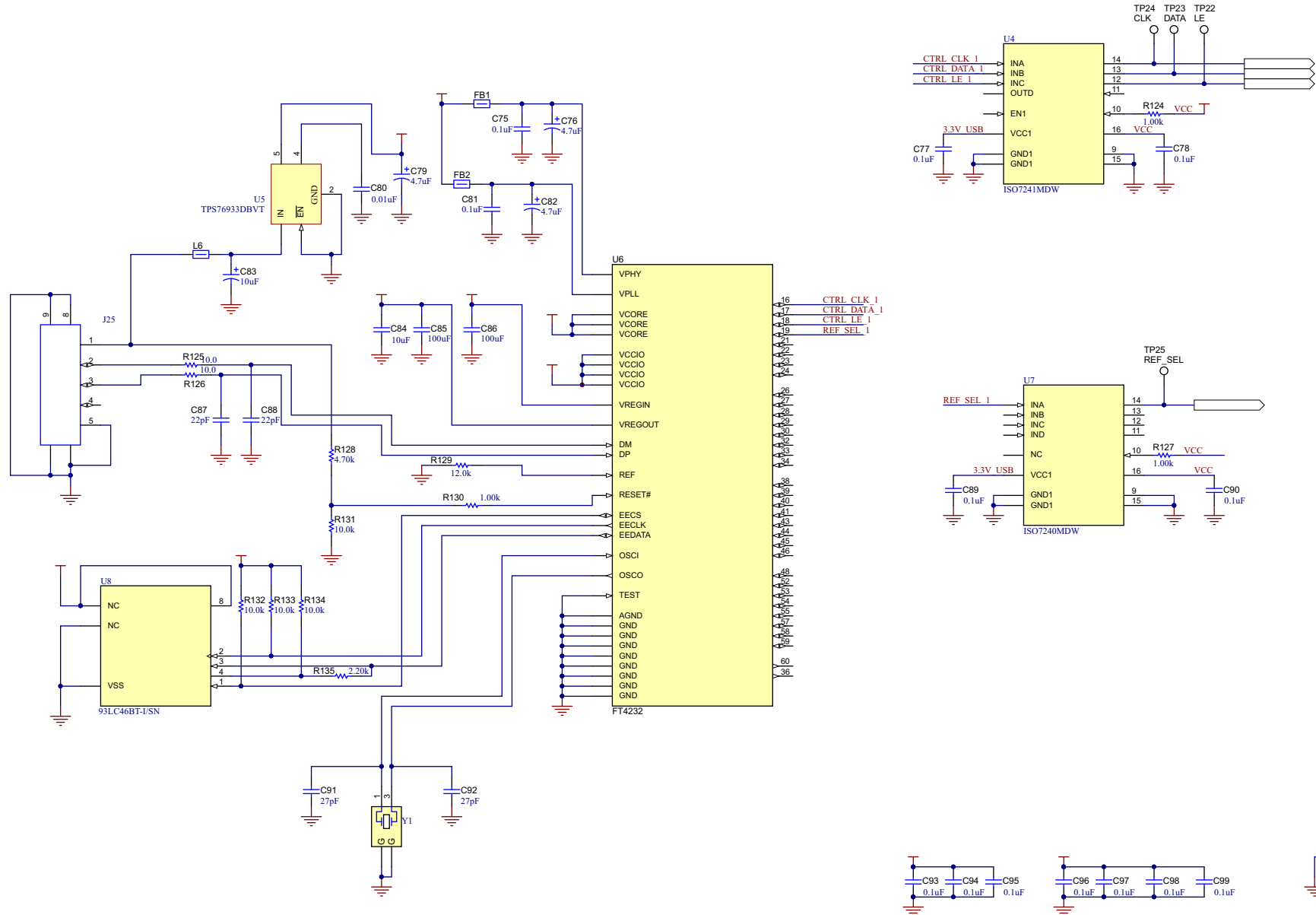


Figure 13. CDCM7005EVM-CVAL Schematic USB/FTDI

7 CDCM7005EVM-CVAL EVM Bill of Materials (BOM)
Table 4. CDCM7005EVM-CVAL BOM

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		HREL001	Any
C1, C8, C14, C20	4	0.1 μ F	CAP, CERM, 0.1 μ F, 16 V, +/- 20%, X5R, 0402	0402	885012105016	Wurth Elektronik
C2, C4, C10, C16, C22, C70	6	10 μ F	CAP, CERM, 10 μ F, 10 V, +/- 10%, X5R, 1210	1210	C1210C106K8PACTU	Kemet
C3, C9, C15, C21, C25	5	22 μ F	CAP, CERM, 22 μ F, 10 V, +/- 10%, X5R, 1210	1210	GRM32ER61A226KE20L	MuRata
C5, C11, C17, C23	4	0.033 μ F	CAP, CERM, 0.033 μ F, 16 V, +/- 10%, X5R, 0402	0402	GRM155R61C333KA01D	MuRata
C6, C12, C18, C19, C24, C26, C27, C28, C29, C32, C44, C45, C46, C47, C48, C49, C50, C57, C73, C74	20	0.01 μ F	CAP, CERM, 0.01 μ F, 25 V, +/- 10%, X7R, 0402	0402	GCM155R71E103KA37D	MuRata
C7	1	0.1 μ F	CAP, CERM, 0.1 μ F, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	CGA2B3X7R1H104K050BB	TDK
C13, C30	2	100 pF	CAP, CERM, 100 pF, 50 V, +/- 10%, X7R, 0402	0402	CC0402KRX7R9BB101	Yageo America
C31	1	0.022 μ F	CAP, CERM, 0.022 μ F, 50 V, +/- 10%, X7R, 0402	0402	GRM155R71H223KA12D	MuRata
C33, C37	2	10 μ F	CAP, CERM, 10 μ F, 25 V, +/- 10%, X5R, 1210	1210	GRM32DR61E106KA12L	MuRata
C34, C35, C36, C38, C39, C40, C41, C43	8	0.1 μ F	CAP, Film, 0.1 μ F, 16 V, +/- 20%, 0805 SMD	0805	ECPU1C104MA5	Panasonic
C42	1	22 μ F	CAP, CERM, 22 μ F, 10 V, +/- 10%, X7R, 1210	1210	GRM32ER71A226ME20L	MuRata
C51, C52, C53, C54, C55, C56, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C71, C72	20	1 μ F	CAP, CERM, 1 μ F, 35 V, +/- 10%, X5R, 0402	0402	GRM155R6YA105KE11D	MuRata
C75, C77, C78, C81, C89, C90	6	0.1 μ F	CAP, CERM, 0.1 μ F, 16 V, +/- 10%, X5R, 0402	0402	GRM155R61C104KA88D	MuRata
C76, C79, C82	3	4.7 μ F	CAP, TA, 4.7 μ F, 16 V, +/- 10%, 4 Ω , SMD	3216-18	TAJA475K016RNJ	AVX
C80	1	0.01 μ F	CAP, CERM, 0.01 μ F, 25 V, +/- 10%, X7R, 0402	0402	GRM155R71E103KA01D	MuRata
C83	1	10 μ F	CAP, TA, 10 μ F, 16 V, +/- 10%, 2.8 Ω , SMD	3528-21	TAJB106K016RNJ	AVX
C84	1	10 μ F	CAP, CERM, 10 μ F, 6.3 V, +/- 20%, X5R, 0603	0603	GRM188R60J106ME47D	MuRata
C85, C86	2	100 μ F	CAP, CERM, 100 μ F, 6.3 V, +/- 20%, X5R, 1206_190	1206_190	C1206C107M9PACTU	Kemet
C87, C88	2	22 pF	CAP, CERM, 22 pF, 100 V, +/- 5%, COG/NPO, 0603	0603	GRM1885C2A220JA01D	MuRata

Table 4. CDCM7005EVM-CVAL BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C91, C92	2	27 pF	CAP, CERM, 27 pF, 250 V, +/- 2%, NP0, 0603	0603	251R14S270GV4T	Johanson Technology
C93, C94, C95, C96, C97, C98, C99	7	0.1 μ F	CAP, CERM, 0.1 μ F, 16 V, +/- 10%, X7R, 0603	0603	GRM188R71C104KA01D	MuRata
D1	1	Green	LED, Green, SMD	1.6x3.2 mm	LTST-C150KGKT	LiteOn
D2, D3, D4	3	Amber	LED, Amber, SMD	1.6x0.8 mm	HSMA-C190	Avago
FB1, FB2	2	120 Ω	Ferrite Bead, 120 Ω @ 100 MHz, 4 A, 1206	1206	HI1206P121R-10	Laird-Signal Integrity Products
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1, J3, J4, J6, J9, J11, J16, J17, J18, J19, J20, J21, J22, J23	14		JACK, SMA, 50 Ω , Gold, EDGE MNT	JACK, SMA, 50 Ω , Gold, EDGE MNT	142-0701-841	Cinch Connectivity
J2, J5, J7, J8, J24	5		Header, 100 mil, 3x1, Gold, TH	Header, 100 mil, 3x1, TH	HTSW-103-07-G-S	Samtec
J10, J12, J13, J14, J15	5		Header, 100 mil, 2x1, Gold, TH	Header, 100 mil, 2x1, TH	HTSW-102-07-G-S	Samtec
J25	1		Connector, Receptacle, USB - mini AB, R/A, SMD	Receptacle, 5-Leads, Body 9.9x9 mm, R/A	67803-8020	Molex
J26	1		BANANA JACK, SOLDER LUG, RED, TH	Red Insulated Banana Jack	SPC15363	Tenma
J27	1		BANANA JACK, SOLDER LUG, BLACK, TH	Black Insulated Banana Jack	SPC15354	Tenma
L1, L2, L3, L4	4	80 Ω	Ferrite Bead, 80 Ω @ 100 MHz, 0.6 A, 0603	0603	CIM10U800NC	Samsung Electro-Mechanics
L5	1	2.2 nH	Inductor, Multilayer, Ceramic, 2.2 nH, 0.3 A, 0.16 Ω , SMD	0402	L-07C2N2SV6T	Johanson Technology
L6	1	1000 Ω	Ferrite Bead, 1000 Ω @ 100 MHz, 0.5 A, 0805	0805	BLM21AG102SN1D	MuRata
R1, R19, R26, R27, R28, R29, R123, R131, R132, R133, R134	11	10.0k	RES, 10.0 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF1002X	Panasonic
R3, R8, R70, R79, R92, R118	6	82	RES, 82, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040282R0JNED	Vishay-Dale
R4, R5, R9, R10, R34, R36, R41, R42, R43, R44, R51, R52, R53, R54, R60, R61, R65, R66, R72, R73, R81, R82, R93, R94, R119, R120	26	0	RES, 0, 5%, 0.063 W, 0402	0402	ERJ-2GE0R00X	Panasonic
R6, R11, R76, R85, R116, R122	6	130	RES, 130, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402130RFKED	Vishay-Dale
R13	1	1.50k	RES, 1.50 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF1501X	Panasonic
R15, R17, R23, R25, R71, R74, R77, R80, R83, R86, R88, R89, R90	13	100	RES, 100, 1%, 0.1 W, 0402	0402	ERJ-2RKF1000X	Panasonic
R18	1	4.12k	RES, 4.12 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04024K12FKED	Vishay-Dale

Table 4. CDCM7005EVM-CVAL BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R20, R21, R22	3	750	RES, 750, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402750RFKED	Vishay-Dale
R30, R37, R128	3	4.70k	RES, 4.70 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF4701X	Panasonic
R31	1	180	RES, 180, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402180RJNED	Vishay-Dale
R35	1	160	RES, 160, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402160RJNED	Vishay-Dale
R38	1	100k	RES, 100 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF1003X	Panasonic
R45, R47, R55, R56, R62, R67, R75, R84, R95, R96, R97, R98, R99, R100, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R121	30	150	RES, 150, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402150RFKED	Vishay-Dale
R124, R127	2	1.00k	RES, 1.00 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF1001X	Panasonic
R125, R126	2	10.0	RES, 10.0, 1%, 0.1 W, 0603	0603	RC0603FR-0710RL	Yageo America
R129	1	12.0k	RES, 12.0 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1202V	Panasonic
R130	1	1.00k	RES, 1.00 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1001V	Panasonic
R135	1	2.20k	RES, 2.20 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF2201X	Panasonic
S1, S2	2		Switch, Tactile, SPST-NO, 1VA, 32 V, SMT	Switch, 6.3x5.36x6.6 mm, SMT	KT11P2JM34LFS	C&K Components
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10	10	1x2	Shunt, 100 mil, Flash Gold, Black	Closed Top 100 mil Shunt	SPC02SYAN	Sullins Connector Solutions
TP1	1		Test Point, Compact, Red, TH	Red Compact Test point	5005	Keystone
TP2	1		Test Point, Compact, Black, TH	Black Compact Test point	5006	Keystone
TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20	18		Test Point, Compact, Yellow, TH	Yellow Compact Test point	5009	Keystone
TP21	1		Test Point, Miniature, Black, TH	Black Miniature Test point	5001	Keystone
TP22, TP23, TP24, TP25	4		Test Point, Miniature, White, TH	White Miniature Test point	5002	Keystone
TP26, TP27, TP28, TP29	4		Test Point, Miniature, Red, TH	Red Miniature Test point	5000	Keystone
U1	1		3.3-V High Performance Rad-Tolerant Class V, Clock Synchronizer And Jitter Cleaner, HFG0052A (CFP-52)	HFG0052A	CDCM7005HFG/EM	Texas Instruments
U2	1		Single 5.5 MHz, RRIO, Low Power, 2.5 to 5.5 V, -55 to 125 degC, 8-pin SOIC (D8), Green (RoHS & no Sb/Br)	D0008A	OPA341UA	Texas Instruments
U3	1		Low-Voltage 1:10 LVPECL With Selectable Input Clock Driver, HFG0036A (CFP-36)	HFG0036A	CDCLVP111HFG/EM	Texas Instruments
U4	1		150 Mbps Quad Channels, 3 / 1, Digital Isolator, -40 to +125 degC, 16-pin SOIC (DW), Green (RoHS & no Sb/Br)	DW0016B	ISO7241MDW	Texas Instruments

Table 4. CDCM7005EVM-CVAL BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
U5	1		Single Output LDO, 100 mA, Fixed 3.3 V Output, 2.7 to 10 V Input, with Low IQ, 5-pin SOT-23 (DBV), -40 to 125 degC, Green (RoHS & no Sb/Br)	DBV0005A	TPS76933DBVT	Texas Instruments
U6	1		Quad High Speed USB to Multipurpose UART/MPSSE IC	LQFP_10x10 mm	FT4232HL	FTDI
U7	1		150 Mbps Quad Channels, 4 / 0, Digital Isolator, 3.3 V / 5 V, -40 to +125 degC, 16-pin SOIC (DW), Green (RoHS & no Sb/Br)	DW0016B	ISO7240MDW	Texas Instruments
U8	1		1K Microwire Compatible Serial EEPROM	SOIC-8	93LC46BT-I/SN	Microchip
Y1	1		CRYSTAL 12.000 MHz 10PF SMD	3.2x0.55x2.5 mm	ABM8G-12.000MHZ-B4Y-T	Abracon Corporation
Y2	1		Oscillator, 491.52 MHz, SMD	9.5x14.4 mm	VX-501-0275-491M52	Vectron
R2, R7, R12, R14, R32, R33	0	0	RES, 0, 5%, 0.063 W, 0402	0402	ERJ-2GE0R00X	Panasonic
R16, R24, R78, R87, R91, R117	0	51	RES, 51, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040251R0JNED	Vishay-Dale
R39, R40, R49, R50, R59, R64	0	82	RES, 82, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040282R0JNED	Vishay-Dale
R46, R48, R57, R58, R63, R68	0	130	RES, 130, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402130RFKED	Vishay-Dale
R69	0	100	RES, 100, 1%, 0.1 W, 0402	0402	ERJ-2RKF1000X	Panasonic

CDCM7005EVM-CVAL Software GUI Installation

1. Download software GUI from ti.com at www.ti.com/lit/zip/sglc002.
2. Unzip the GUI installer file *sglc002.zip*.
3. Invoke the installer executable file, *CDCM7005-SP_EVM_GUI_Installer.exe*, as administrator by right clicking and choosing the option Run as administrator.

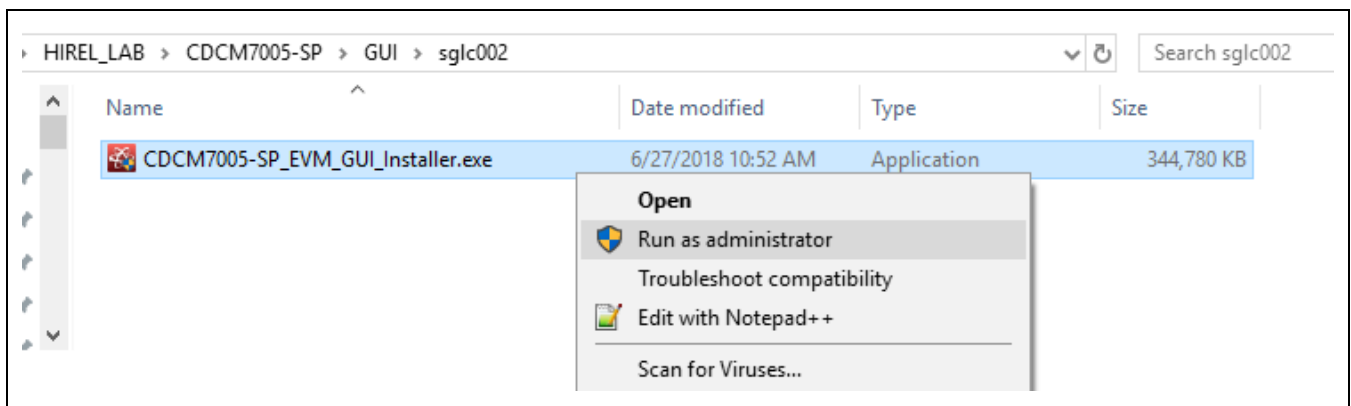


Figure 14.

4. Click *Next*

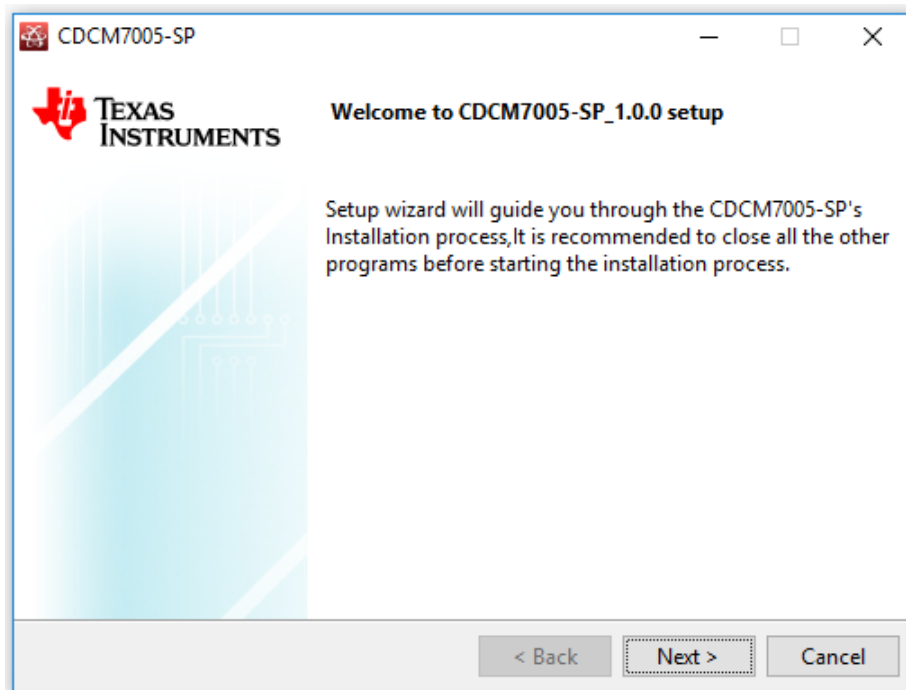


Figure 15.

5. Read the License Agreement and click the I accept the agreement button and click *Next*.

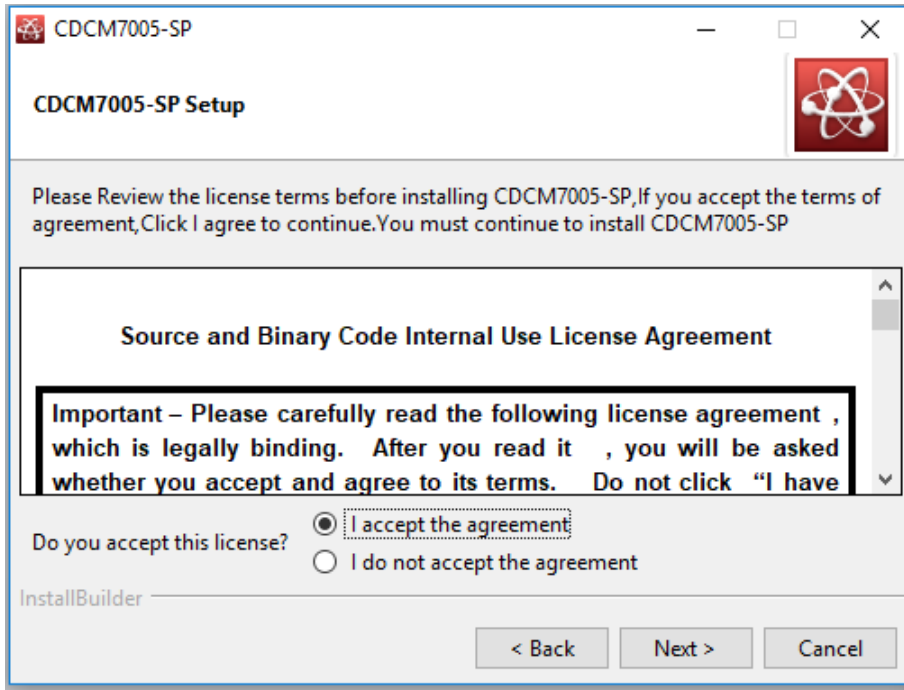


Figure 16.

6. Read the License Agreement and click the I accept the agreement button and click *Next*.

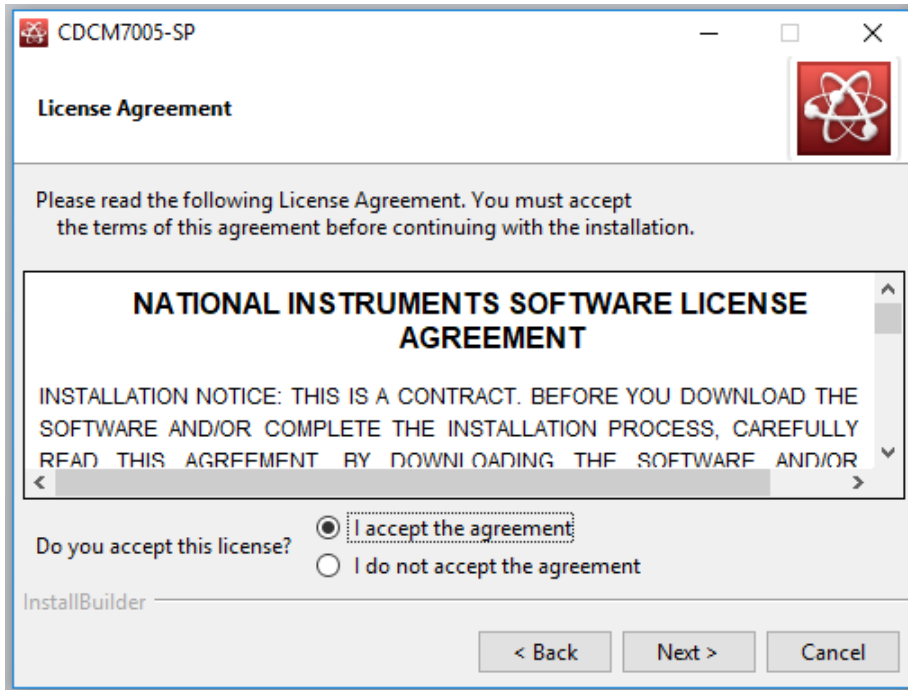


Figure 17.

7. Accept the default install path, or change it, and then click *Next*.

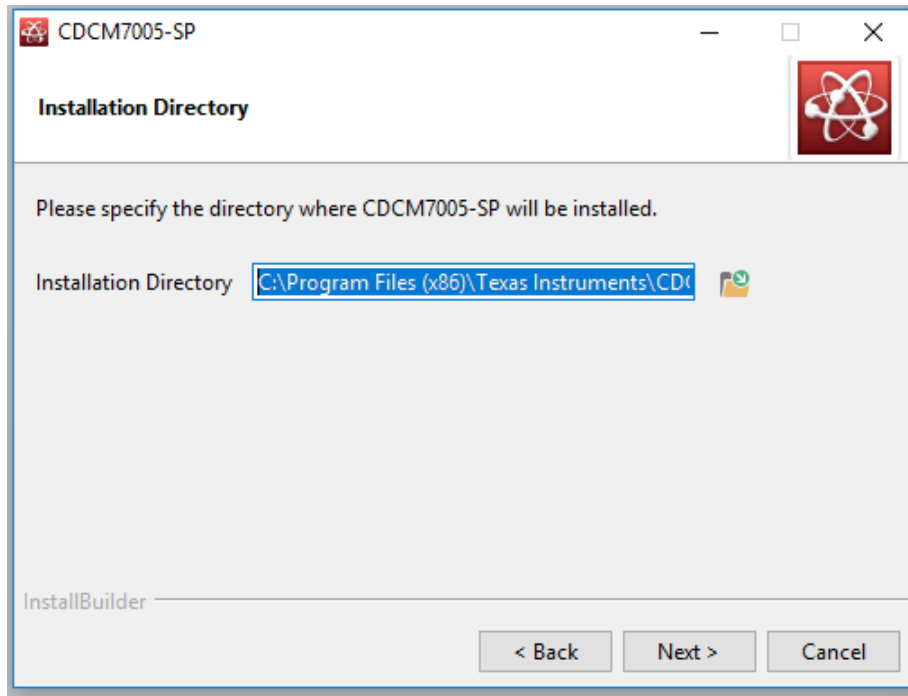


Figure 18.

8. Select/Deselect components to be installed and press Next. [GUI should automatically determine and select what is needed.]

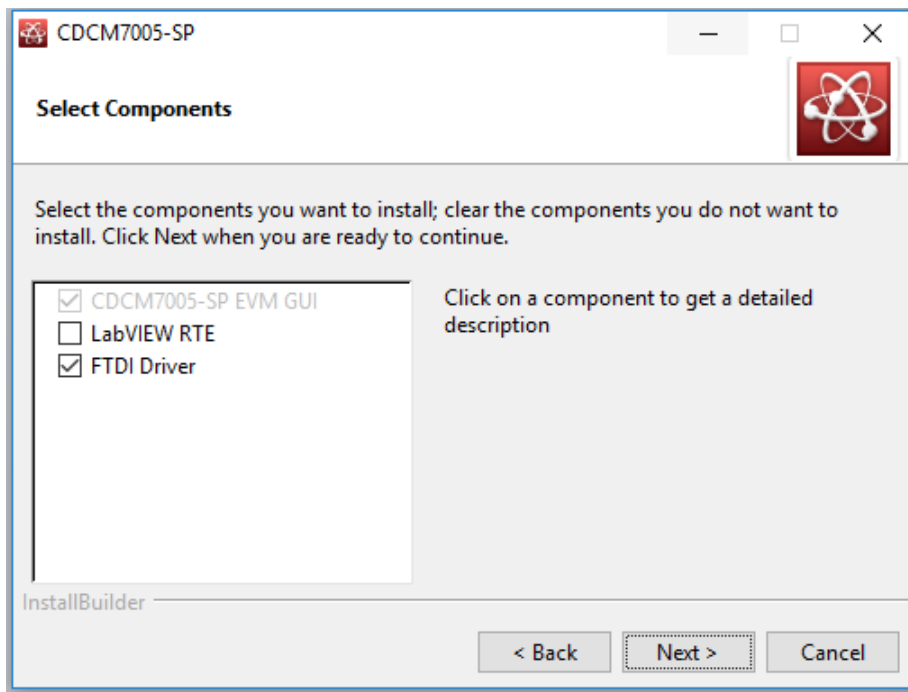


Figure 19.

9. Click *Next*.

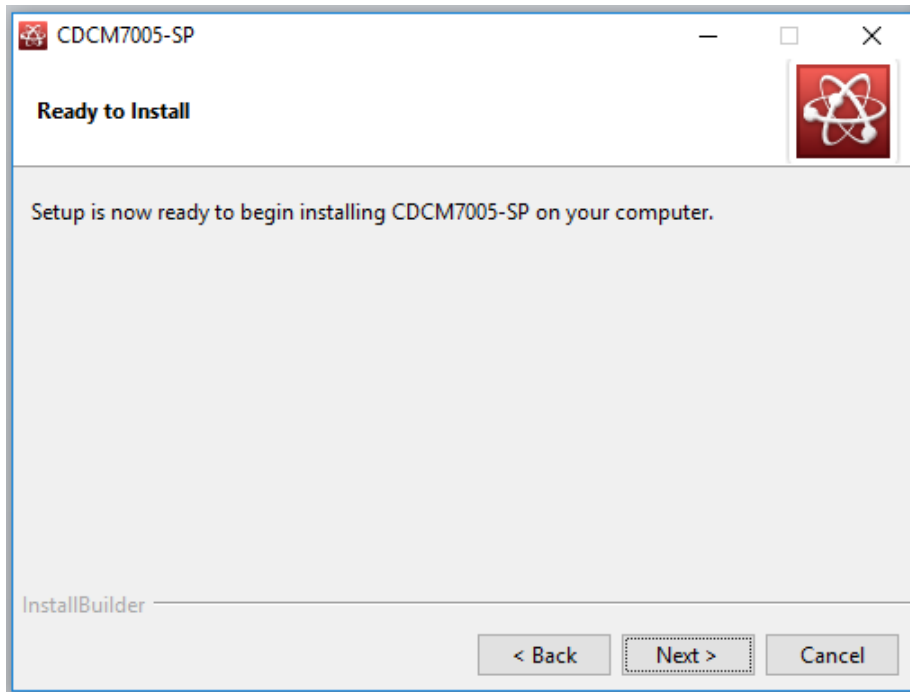


Figure 20.

10. Installation will begin showing progress.

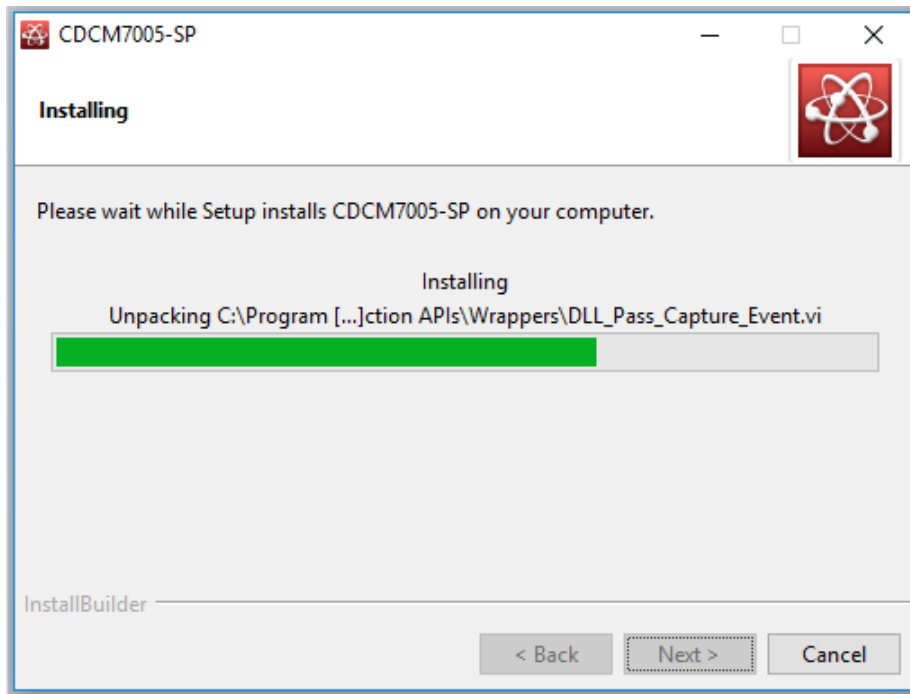


Figure 21.

11. Select what components to add and/or view and press Finish.

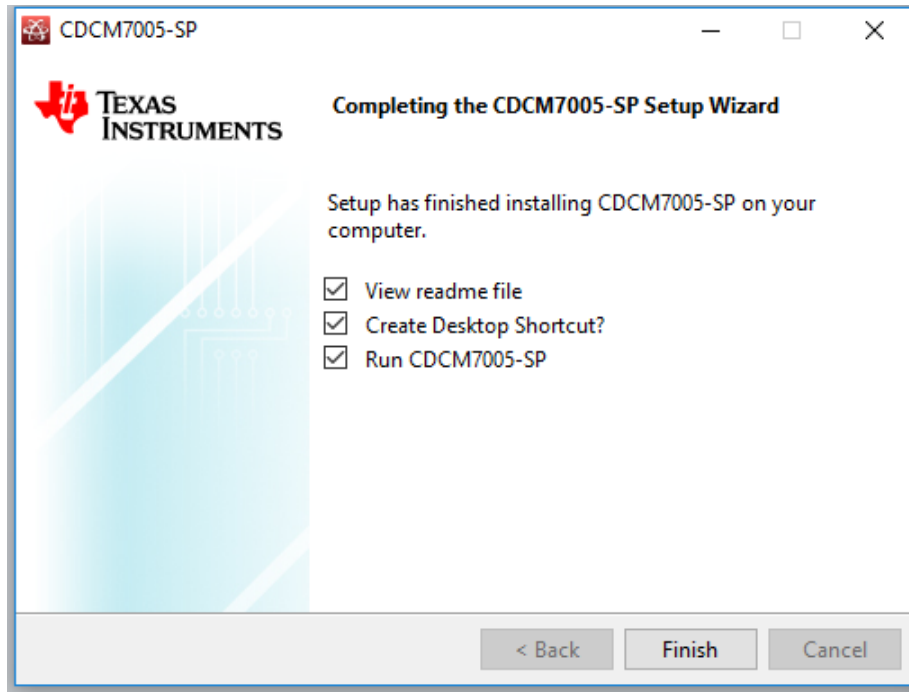


Figure 22.

12. If selected on previous menu, the following README file will appear. Press OK.

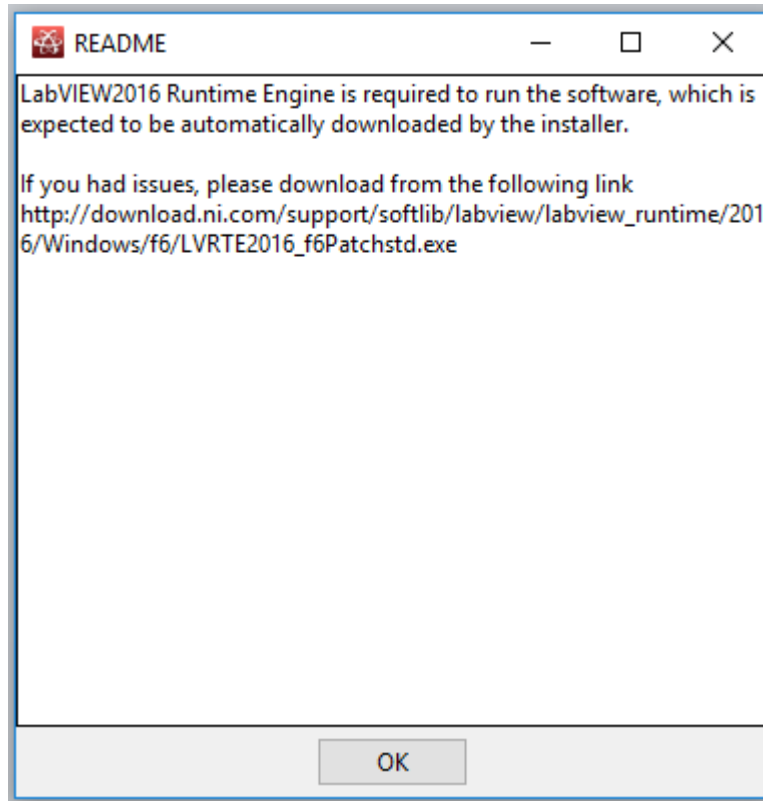


Figure 23.

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