*Application Brief*

# *Important Multiplexer Characteristics for I3C Applications*

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### What is I3C and where is it used?

I3C (Improved Inter Integrated Circuit) is a serial communication interface specification that addresses the limitations and lacking features of the I2C and SPI legacy interfaces According to the MIPI alliance, there are three goals of I3C:

1. Standardize sensor communication.
2. Reduce the number of physical pins used in sensor system integration.
3. Support low power, high speed, and other critical features that are currently covered by I2C and SPI.

I3C addresses these goals by combining key attributes and features of I2C and SPI and enhancing them to provide a higher performance protocol. A few of the features that are provided by I3C are in-band interrupts, in-band target resets, greater speed when compared to I2C, and fewer necessary wires than SPI all while consuming less power than current legacy interfaces. Additionally, I3C is backwards compatible with I2C.

Due to the increased functionality when compared to SPI or I2C, I3C allowed improvements in next generation designs of server, notebook, and enterprise customers. Additionally, I3C helped bring about the advent of DDR5.

Further definition of the specs and features of I3C are provided here.

### How to find an I3C compatible passive mux?

There are many characteristics that influence whether a passive mux can be considered I3C compatible. This article focuses on the most significant ones: on-capacitance, configuration, voltage, bandwidth, and topology. While consideration of these characteristics accounts for the most common requirements for selecting a passive mux, this list is not exhaustive. Depending on the application, other characteristics can influence passive mux selection.

### On-Capacitance

One of the most important specifications to consider for I3C is the limited bus capacity. Where I2C has a 400-pF limit per bus, I3C greatly reduces this limit to 50 pF. To allow enough room for the trace capacitances, the capacitance of the controller, and the capacitance of the peripherals on the bus line, the on-capacitance of the multiplexer must not exceed 10 pF. However, using a multiplexer with an on-capacitance of less than 5 pF to prevent the multiplexer from contributing greatly to the capacitive load of the bus line is recommended. Additionally, the trace must be as short as possible to allow for more margin in the driver, mux, and peripheral capacitance.

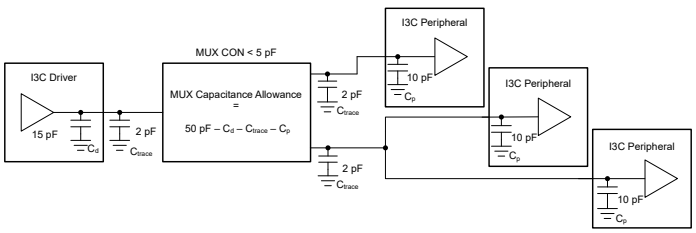


**Figure 1. I3C Bus Line Capacitive Load**

A single I3C driver can communicate with multiple buses. Adding a multiplexer separates the capacitances of the I3C peripheral buses, which allows the total capacitance of the system to surpass the 50-pF maximum while keeping the capacitance below 50 pF for any given bus line.

### Configuration

The most common I3C mode is Standard Data Rate (SDR) mode. This is a 2-wire protocol consisting of a single clock and single data line. 2-wire protocol typically requires a 2 channel 2:1 (SPDT) device to allow for communication to two peripheral controllers from a single controller. However, a 2 channel 4:1 option is also feasible to allow for even further expandability of a single controller. With a much lower bus capacitance allotted for I3C, situations can arise where one of the buses is close to 50-pF bus limit, so adding another device is not possible. With a multiplexer, the number of peripherals that a single controller can communicate with can be expanded.

### Voltage Levels

The target voltages of I3C are 1.2 V, 1.8 V, and 3.3 V, so any multiplexer used for I3C applications must support at a minimum these voltage levels. However, this does not greatly limit the selection of multiplexers as most TI multiplexers can support up to 3.3-V signal pass through.

### Bandwidth

The I3C clock has a maximum clock rate of 12.5 MHz using square waves. To maintain the integrity of the clock signal any multiplexer must have a large enough bandwidth to accommodate this signal. For such clock and data signals, we recommend a bandwidth 5-7x greater than the frequency of the input. As a result, the bandwidth of the multiplexer must be at least 62.5 MHz. Additionally, the bandwidth of the system is influenced by Con and Ron so keeping Ron below 10 ohms to preserve the high bandwidth of the system is recommended.

### Topology

I3C requires compatibility with push-pull topology. Since I3C can share a bus with I2C peripherals, there can be instances where both push-pull and open drain are required. This requirement does not limit the selectable options for an analog switch or multiplexer as these devices are passive multiplexers capable of supporting both open drain and push-pull topology.

**Table 1. Key I3C Specifications for Passive Multiplexers**

| Features | I3C Specifications | TMUX136 | TMUX154E |
|---|---|---|---|
| Configuration | 2-wire protocol for Standard Data Rate | 2-channel 2:1 (SPDT) configuration allows for communication to two peripherals from a single controller. | 2-channel 2:1 (SPDT) configuration allows for communication to two peripherals from a single controller. |
| Voltage levels | 1.2 V, 1.8 V, 3.3 V | I/O pins support up to 3.6 V | I/O pins support up to 4.3 V |
| Capacitance | 50 pF maximum capacitance loading | CON (Typical): 1.4 pF has minimal impact to overall loading. | CON (Typical): 7.5 pF has minimal impact to overall loading. |
| On-Resistance | Enables lower distortion and error (flatness) | RON (Typical): 5.7 Ω | RON (Typical): 6 Ω |
| Bandwidth | All clock at 12.5 MHz<br>Standard data rate: 12.5 Mbps | Supports up to 6 GHz per line | Supports up to 900 MHz per line |
| Topology | Open drain and push-pull | Passive switch allows for both signals to be passed through. | |

Table 1 lists the key I3C specification to consider in a passive multiplexer, but there can be more requirements that can affect the choice of which multiplexer to use. To facilitate selection, use the filtered product selection table with all possible multiplexer options that meet the specifications listed in Table 1.

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