Application Report

Low Voltage Translation For SPI, UART, RGMII, JTAG Interfaces

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ABSTRACT

With an increased need for reduced power consumption, modern trends are driving supply voltages lower across many system level designs. As processor voltage levels decrease, peripheral devices still maintain higher voltage levels creating voltage level discontinuities in the system. A solution to this problem is to use a voltage translator, which converts signal voltage levels up or down to another level. They are highly applicable for use in simple GPIO applications as well as in common push-pull interfaces such as SPI, UART, JTAG, and RGMII. The information in this application report discusses industry standard interfaces, along with common end equipment applications with a focus on the AXC family of direction-controlled level translators with the lowest operating voltage in the industry (0.65 V to 3.6 V).

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Trademarks

1 Introduction

The AXC family of devices belong to TI's direction-controlled level translator family. These voltage translators use two separate configurable power supply rails to up- or down-translate incoming signals. The AXC translators are designed for an ultra-low V_{CC} range of 0.65 V to 3.6 V, making them the lowest voltage level translator available in the industry. This allows the device to communicate with advanced processors operating at low-voltage nodes of 0.7 V, 0.8 V, or 0.9 V. The wide V_{CC} range also accommodates the industry standard voltage nodes (1.2 V, 1.8 V, 2.5 V, and 3.3 V) commonly found in processors and peripherals. These devices support data rates of up to 380 Mbps while providing 12 mA of drive strength. V_{CC} isolation, I_{OFF} functionality, and built-in ESD (electro static discharge) protection with 8-kV HBM (human body model) and 1-kV CDM (charged device model) are all features standard across this family of devices. Refer to Table 1-1 for information on the AXC family.

Table 1-1. AXC Family Features

PARAMETER	AXC FAMILY
Voltage Support	0.65 V–3.6 V
Data Rate	380 Mbps
Drive Strength	12 mA
Icc (AXC1T at 125°C)	14 µA
ESD Ratings	8-kV HBM, 1-kV CDM
Operating Temperature	-40°C to 125°C
Power Sequencing	Not Required
Ioff Partial power down	Supported

Most of the devices in the family have a version with bus-hold functionality, denoted by “H” as in AXCH*. Bus hold circuitry allows the voltage translator to retain the last known output state in the event an input becomes high impedance or floating. See the *System Consideration for Using Bus-Hold Circuits to Avoid Floating Inputs* application report for more information. The 4-bit and 8-bit devices feature two direction control pins allowing two independent banks of buses on a single device. This allows more control in how the device can be provisioned for simultaneous up- and down-translations; and, ideally reduces the BOM count. Additionally, these devices include an output enable pin to put all outputs in a high impedance state which also reduces power consumption. All devices in the family were designed to ensure glitch free power sequencing across hundreds of possible start up or shut down conditions. This allows either supply rail to be powered on or off in any order without causing a glitch at the output. See the *Glitch Free Power Sequencing with AXC Level Translators* application report.

2 Common Interfaces and AXC Implementation

2.1 General Purpose Input Output (GPIO)

All microprocessors have General purpose input output (GPIO) ports for communication with the peripheral devices. However, the core and peripheral chips might work at different voltage levels, which is why the system would need a level shifter. If the required signals are not shifted to the voltage at which the microprocessor is operating, it impacts the reliability of communication. The SN74AXC1T45 can be implemented as part of the I/O circuit, especially in single channel signals such as control inputs. The SN74AXC1T45 provides a solution for voltage translating I/O pins such as the following:

- Enable
- Restart
- Clock buffering
- Power good
- Error flag
- Reset
- Memory error
- Processor overheat
- LED driving as shown in Figure 2-1

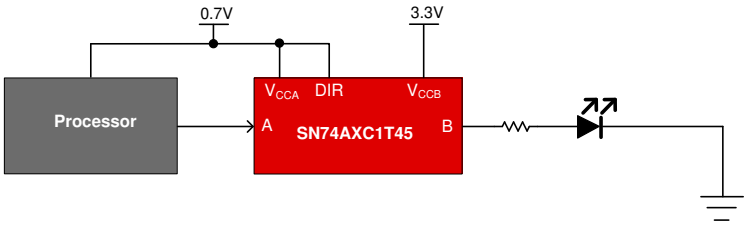


Figure 2-1. GPIO Translation Using SN74AXC1T45 for LED Driving

2.2 Serial Peripheral Interface (SPI)

Serial peripheral interface (SPI) provides synchronous communication between a processor and peripheral. SPI is a four line “controller-peripheral” architecture communication interface, with three lines driven by the controller (usually the processor) and one line driven by the peripheral (usually the peripheral). Table 2-1 describes the SPI signal interface.

Table 2-1. SPI Interface

SIGNAL	DESCRIPTION	DIRECTION
CLK	Clock Signal	Controller to Peripheral
CIPO	Controller Input/Peripheral Output	Peripheral to Controller
COPI	Controller Output/Peripheral Input	Controller to Peripheral
CS	Peripheral Select	Controller to Peripheral

The first signal line driven by the controller is CLK, which is the clock signal. With each clock pulse, the controller can transmit or receive one bit to or from the peripheral. The data rate is usually 10 Mbps, however, it can be extended as desired in the system. Since SPI is full duplex, two data lines are needed: COPI and CIPO. COPI stands for controller output peripheral input, and is driven by the controller to send data to the peripheral. CIPO stands for controller input peripheral output, and is driven by the peripheral to send data to the controller. The final line is CS, which is the peripheral select signal. The CS line is driven low by the controller to select the peripheral device for communication. Multiple peripherals may exist in a system and this ensures that the desired peripheral is being communicated with to prevent any system level bus contention. SPI is commonly used in the following:

- Control signals
- Sensors
- Memory
- LCD display
- SD cards

2.2.1 Voltage Translation for SPI

Interfacing between devices with SPI protocol is possible when the signal levels are the same. In cases where there is a voltage mismatch, it is recommended to use a level shifter. The SN74AXC4T774 or SN74AVC4T774 is the ideal solution to translate all four lines used in SPI. The SN4AXC4T774 has the advantage of each direction of the channel being independently controlled. This makes it extremely useful in SPI where one line operates in the opposite direction from the other three. Additionally, the AXC family can support up to 380 Mbps, which is well above the usual SPI data rates. Since SPI is an interface that can accommodate multiple independent peripherals operating under the same controller, the position of the voltage translator is an important design consideration. In cases where the bus has multiple peripherals each on a different voltage node, it is recommended to put a signal level translator before each peripheral, as opposed to only using one level shifter after the controller as shown in Figure 2-2

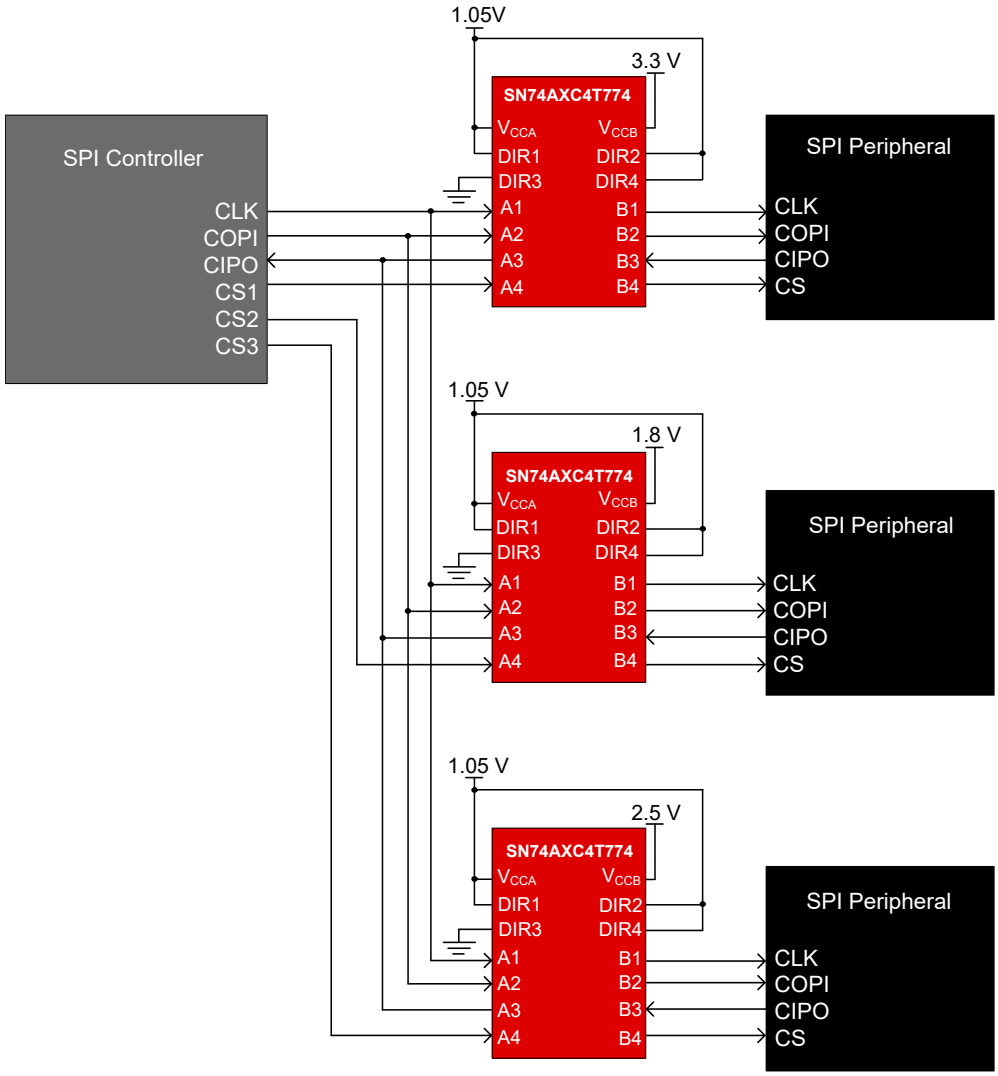


Figure 2-2. SPI Interface Using SN74AXC4T774 Device

2.2.2 SPI Applications

SPI is one of the most common interfaces due to its simple protocol, relatively high speeds, and full duplex communication. One common application of SPI in the automotive sector is within the automotive head unit. It enables communication between the applications processor and external media. It also allows the applications processor to communicate with other peripherals such as atmospheric sensors within the car.

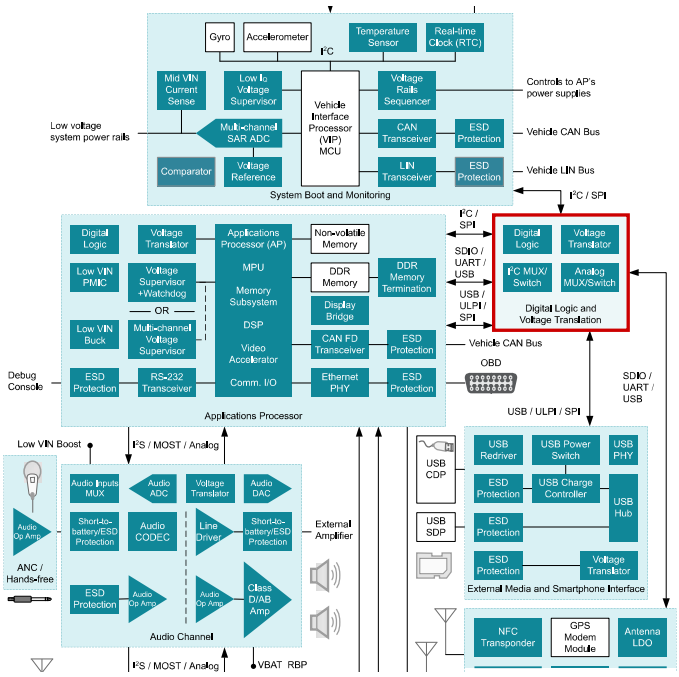


Figure 2-3. Automotive Head Unit

The SPI enables communication between the processor and MCU, and between the processor and LCD display in the smart speaker or smart display as shown in Figure 2-4.

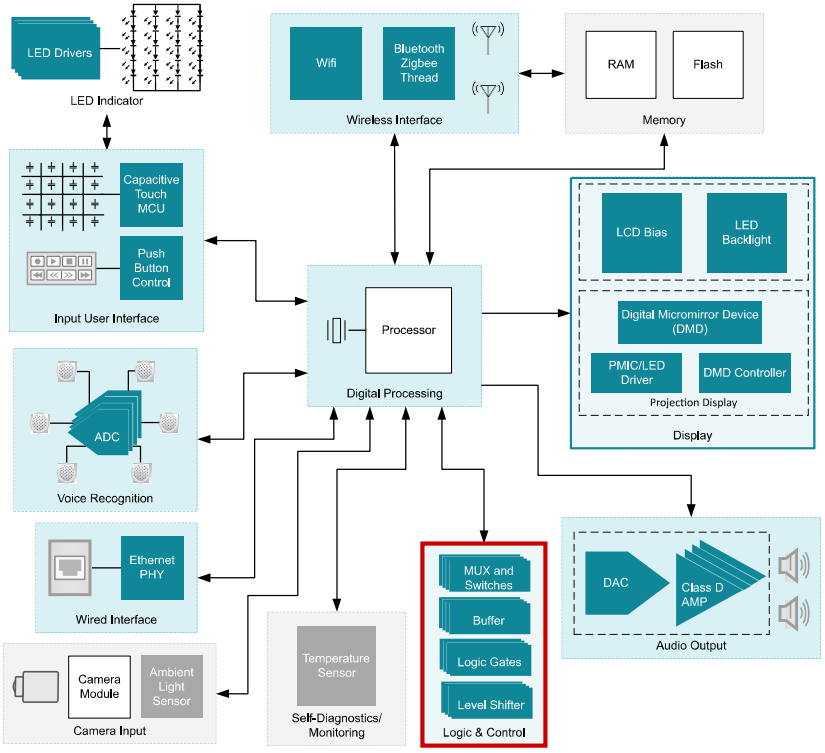


Figure 2-4. Smart Speaker and Smart Display

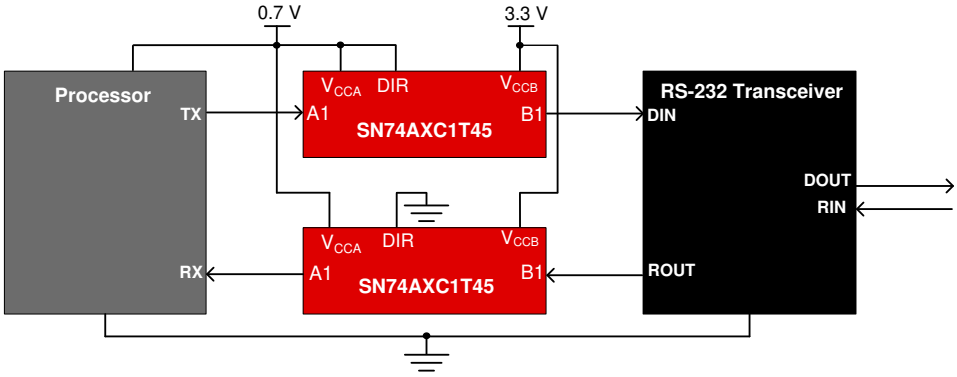
2.3 UART

Universal Asynchronous Receiver/Transmitter (UART) is a hardware device that enables two or four signal, asynchronous, full duplex communication interfaces. The UART is responsible for converting parallel data to serial for transmission, and vice-versa for receiving. In the two signal UART variation, the signals are host transmit (TX) and host receive (RX). In the four signal variation, there are RX and TX signals, as well as ready-to-send (RTS) and clear-to-send (CTS), which are used for handshaking. The data frame consists of a low level start bit, data bits, optional parity bit, and the stop bits. While the UART does handle data framing, generating, and receiving data, it does not define a common signaling method between devices. The UART output is a signal at the operating voltage of the device, such as 1.2 V or 2.5 V. These signals are acceptable for use in short distances between two UARTs operating at the same voltage level. Since this is not usually the case, the signal from the UART is usually sent to a line driver to convert the signal to a standard such as RS-232 or RS-485. The standards allow longer distance communication through defined signal characteristics. RS-232 uses a voltage range of –12 V to 12 V to improve noise margin on the line. RS-485 uses differential pairs to transmit a signal. Both RS-485 and RS-232 standards use UART data framing, yet a transceiver is necessary to invert and translate the UART signals. Since UART is asynchronous, there is no clock signal. Instead, both communicating devices must be configured to use the baud rate, equivalent to bits per second (bps) in UART. UART is generally considered a low speed interface with speeds between 300 bps to 115 kbps.

2.3.1 Voltage Translation With UART

To use UART between two devices operating at different voltage levels, a voltage translator is necessary. Depending on the system configuration, either SN74AXC1T45 or SN74AXC4T245 voltage translators may be used.

Figure 2-5. 2-wire UART Voltage Translation Using SN74AXC1T45



For a simple two line interface, two SN74AXC1T45 on each data line can be implemented to achieve voltage translation. This configuration requires the direction pin on one device to be pulled to V_{CCA} high to achieve A to B translation, and the DIR pin of the other device pulled to ground to achieve B to A translation as shown in Figure 2-5.

For the four line interface, SN74AXC4T245 can be used with DIR1 pin pulled to V_{CCA} and the other DIR2 pin pulled to ground. This ensures that two channels translate from A to B and two channels translate B to A. The TX and CTS lines should communicate in one direction, while RX and RTS communicate in the opposite direction as shown in Figure 2-6.

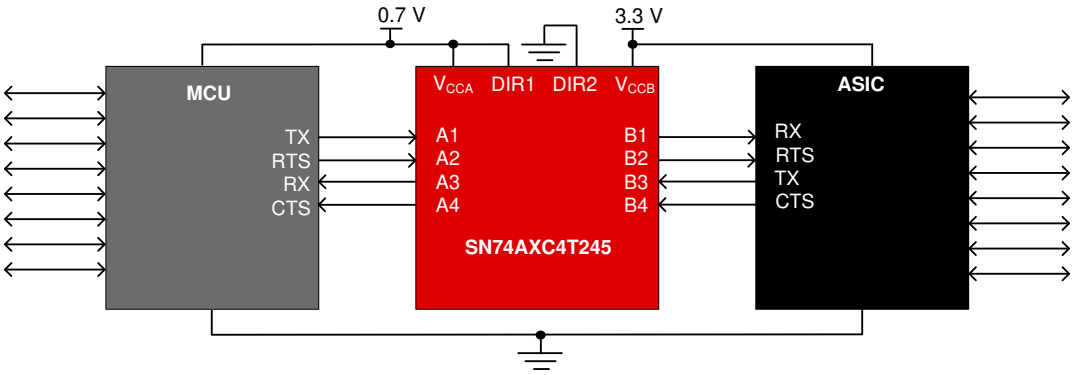


Figure 2-6. 4-wire UART Voltage Translation Using SN74AXC4T245

Another common UART configuration is having two separate UARTs running. To achieve translation in this configuration, the SN74AXC4T245 can be used. The setup is the same as the 4-line UART, with both direction pins being pulled to V_{CCA}. In this configuration, both TX lines would run in the same direction, opposite to the two RX lines as shown in Figure 2-7.

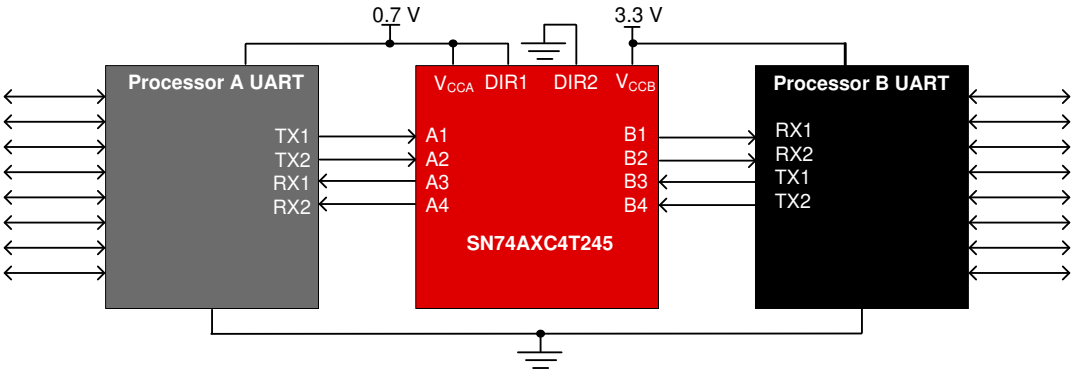


Figure 2-7. Two 2-wire UART Interface Voltage Translation Using SN74AXC4T245

2.3.2 UART Applications

UART hardware is found on nearly every processor. Because of its wide availability and simple implementation, UART is found in systems across every market sector. It is a common means of processor to processor communications as well as communication between microcontrollers and peripherals. In the automotive advanced driver-assistance system (ADAS) applications, like the surround view system electronic control unit (ECU) or ADAS domain controller, UART is used in the digital processing block to enable communication between the application processor and the automotive microcontroller (MCU) as shown in Figure 2-8.

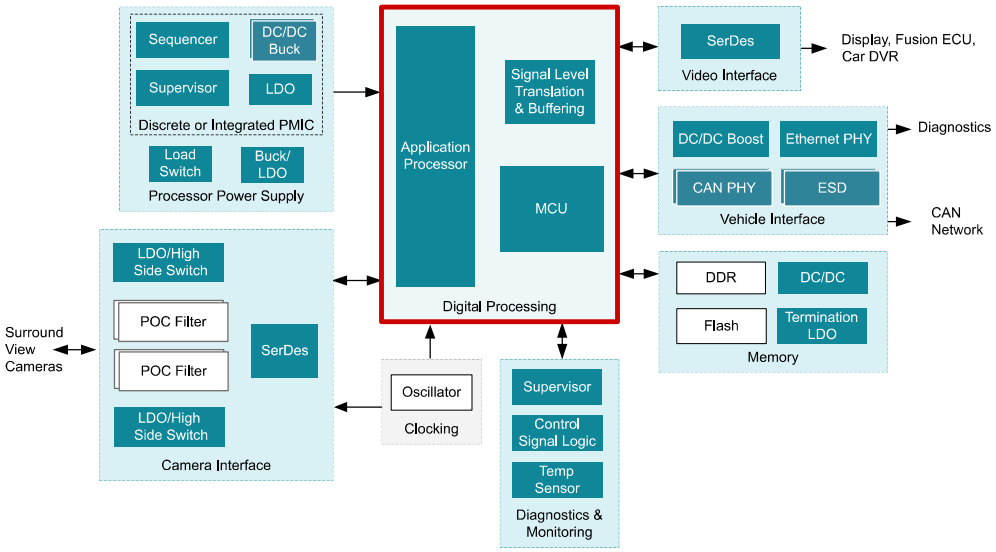


Figure 2-8. UART in ADAS Surround View System ECU

RS-232 communication port in Remote Radio Units (RRU) is used to control the fan and climate control in the system, while also providing a debug consol interface. To ensure the RS-232 transceiver receives proper logic levels, a voltage translator, such as an AXC family device, may be used between the processor and transceiver as shown in Figure 2-9.

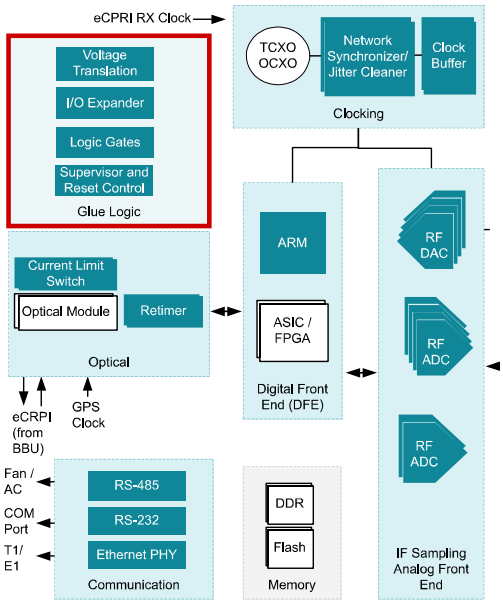


Figure 2-9. UART in Remote Radio Unit

2.4 Joint Test Action Group (JTAG)

Joint Test Action Group (JTAG) developed a hardware interface of the same name to allow debugging, testing, verification, and programming of embedded designs. JTAG usually operates using five lines: TCK, TMS, TDI, TDO, and TRST as listed in Table 2-2. Test Clock (TCK) provides the timing for the data input and output. Test Mode Select (TMS) allows the user to choose what will be tested. Test Data In (TDI) is where data to be tested is input to the device under test, the resulting output is carried on Test Data Out (TDO). The final signal, Test Reset (TRST), is optional and gives the ability to reset JTAG to the last known good state.

Table 2-2. JTAG Interface

SIGNAL	DESCRIPTION	DIRECTION
TCK	Test Clock Signal	Controller to Debugger
TDI	Test Data In	Controller to Debugger
TDO	Test Data Out	Debugger to Controller
TMS	Test Mode Select	Controller to Debugger
TRST	Test Reset	Controller to Debugger

Since JTAG is similar to SPI, the configuration of voltage translators is similar. The key difference is that JTAG has four lines running in one direction and one in the opposite direction. To enable use of JTAG interface between a low voltage FPGA or processor, and a JTAG probe, the SN74AXC4T774 or the SN74AVC4T774 device, as configured in Figure 2-10 is recommended. Alternatively, one SN74AXC4T245 for the TCK, TMS, TDI, and TRST signal lines, and one SN74AXC1T45 for the TDO line operating in the other direction can be used, for the five-line JTAG interface.

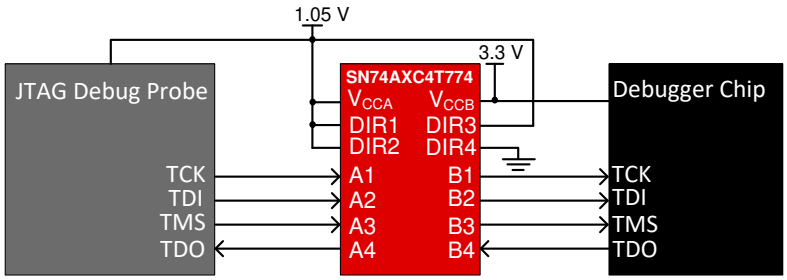


Figure 2-10. JTAG Voltage Translation Using SN74AXC4T774

2.4.1 JTAG Applications

JTAG is an industry standard for testing PCBs and Integrated circuits, as well as programming many FPGAs. The ability to run boundary scan tests, program, and debug makes JTAG essential across development, production, and deployments. Because of this, JTAG ports are found on microprocessors and JTAG headers are found on many PCBs across every market.

In enterprise computing, JTAG headers are commonly found in Rack servers. JTAG is essential in this application as many servers require periodic diagnostic maintenance. Having a JTAG port available on servers enable the technicians and engineers to quickly debug issues during maintenance.

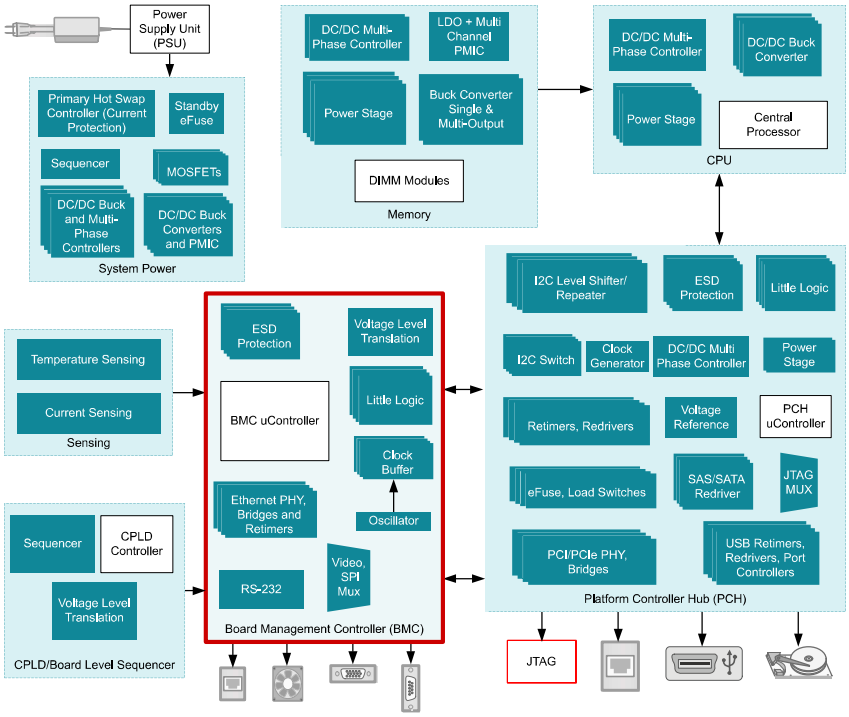


Figure 2-11. JTAG in Rack Servers

2.5 Reduced Gigabit Media Independent Interface (RGMII)

Reduced Gigabit Media Independent Interface (RGMII) is a high speed interface to connect a media access control device (MAC) to an Ethernet physical layer chip (PHY). It is a modification of Media Independent Interface (MII), with the improvements being the gigabyte data rate, as opposed to 100 Mbps, and reduced interface pin count.

Table 2-3. RGMII Signals

SIGNAL	DESCRIPTION	DIRECTION
TXC	Clock signal	MAC to PHY
TXD[0…3]	Transmitted Data	MAC to PHY
TX_CTL	Transmitter Enable/Error	MAC to PHY
RXC	Recovered clock signal (from received data)	PHY to MAC
RXD[0…3]	Received Data	PHY to MAC
RX_CTL	Received data valid/receiver error	PHY to MAC

RGMII uses 12 lines as described in Table 2-3. The clock is set to 125 MHz for achieving gigabit speeds, and 25/2.5 MHz for 100/10 Mbps speeds, respectively. In gigabit operation, data is clocked on both the rising and falling edge of this signal, and in 100/10 Mbps operation, data is clocked only on the rising edge. Due to the high speed requirements of RGMII, a tight timing budget must be implemented with limited skew. The final two signals are RX_CTL and TX_CTL, two control signals multiplexed by the clock signals. RX_CTL carries the received data valid signal and the receiver error signal. TX_CTL contains the transmitter enable and transmitter error signal.

2.5.1 Voltage Translation for RGMII

To enable communication between a low-voltage MAC and a PHY of a different voltage level, a high-speed voltage translator with tight output channel-to-channel skew is recommended. To meet these system requirements, consider the SN74AXC8T245. To use the SN74AXC8T245 in this application, the six transmit signals, TXC, TXD [0…3], and TX_CTL should share one device. The six receiving signals, RXC, RXD [0…3] and RX_CTL use a separate SN74AXC8T245. It is recommended that the transmitter clock and data signals, as well as the receiver clock and data signals, are on the same device. A small difference in propagation delay between the output channels (skew) of the device could have a negative effect on the strict timing budget of the RGMII interface.

The bus-hold circuit avoids unknown voltage levels caused by floating inputs. Bus-hold circuitry allows the voltage translator to retain the last known output state in the event an input becomes high impedance or floating. This is useful in systems where peripherals may turn off intermittently or in cases where peripherals are plugged into a backplane via a plug-in card as in the case of Ethernet-PHY. See the *System Considerations for Using Bus-hold Circuits to Avoid Floating Inputs* application report. Devices with integrated bus-hold circuitry on the input and output ports, like the SN74AXCH8T245, are commonly used for many of the enterprise and communication applications.

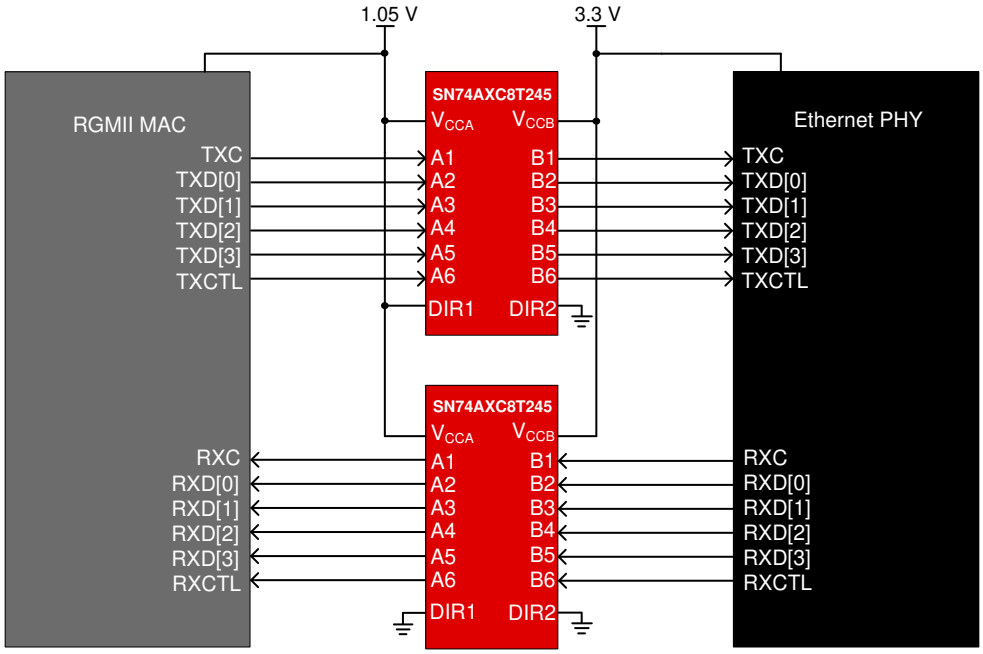


Figure 2-12. RGMII Voltage Translation Using SN74AXC8T245

2.5.2 RGMII Applications

RGMII is used in many applications that need large amounts of bandwidth due to its very high speed. Because of this, RGMII is found in many applications that sends data over ethernet, making it a widely used communication protocol in industrial and telecommunications sectors.

RGMII is heavily used in IP network cameras in the industrial sector. Figure 2-13 illustrates an example of an IP network camera transferring data over the Ethernet using RGMII. Once all video and audio data is processed, they are sent from the MAC to the PHY where they are serialized and sent over Ethernet. If the MAC and PHY are operating at different voltage levels, use a level shifter, such as the SN74AXC8T245 or the SN74AXCH8T245, to bridge the voltage mismatch to enable communication. Voltage translation may be also be required between the image sensor(or other peripherals) and the MPU.

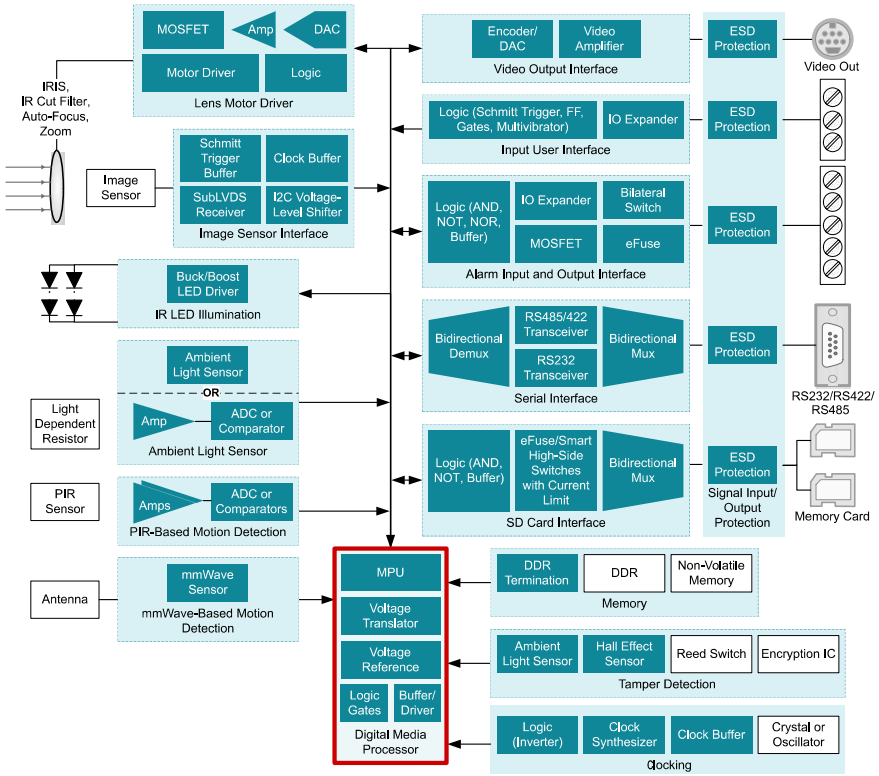


Figure 2-13. Data Over Ethernet in IP Network Camera Using RGMII

2.5.3 Skew Performance

Output skew is defined as the difference between the propagation delay on the output channels which are driving equal loads with all the inputs arriving at the same time. It is particularly important in the RGMII interface where the high speed clock needs to synchronize the data on RX and TX lines with maximum allowed skew of 500 ps. See the *RGMII Interface Timing Budgets* application report. The output channel-to-channel skew for A-to-B direction rising-edge input under standard loading conditions is 104 ps as shown in Figure 2-14. The measurement was taken with 1.65 V V_{cca}, 3.3 V V_{ccb} at 25°C. Similarly, under the same condition, the falling edge skew measurement is 127 ps.

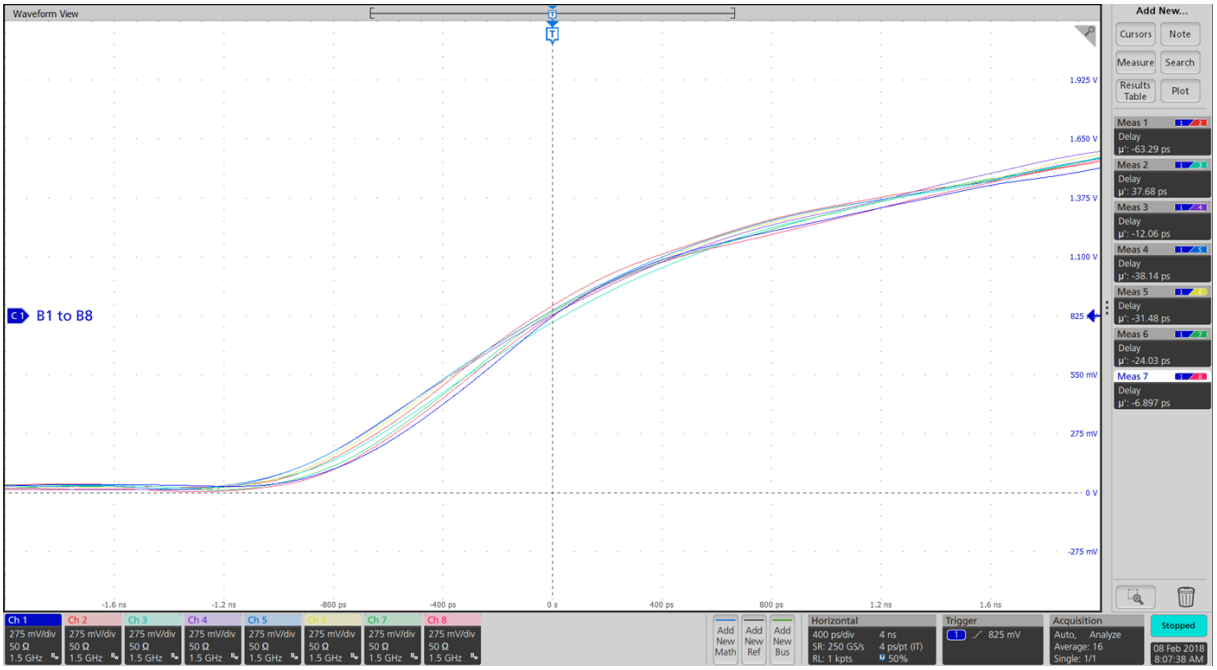


Figure 2-14. 104 ps Channel-to-Channel Skew for SN74AXC8T245

3 Summary

Table 3-1 summarizes the different industry standard interfaces and level shifter recommendations from TI.

Table 3-1. Summary of Interfaces and Level Shifter Device Recommendation

Interface	Recommended Translation Device
SPI	SN74AXC4T774
UART	SN74AXC1T45, SN74AXC4T245
JTAG	SN74AXC4T774
RGMII	SN74AXC8T245, SN74AXCH8T245
GPIO	SN74AXC1T45

4 Related Documentation

- Texas Istruments, *Glitch Free Power Sequencing with AXC Level Translators* application report
- Texas Instruments, *RGMII Interface Timing Budgets* application report
- Texas Instruments, *System Consideration for Using Bus-Hold Circuits to Avoid Floating Inputs* application report

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2019) to Revision B (May 2019)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	2
• Updated application report to include inclusive terminology	2

Changes from Revision * (November 2018) to Revision A (May 2019)	Page
• Edited application report for clarity	2
• Added the SN74AXC4T774 device.	3
• Added the SN74AXC4T774 device.	9

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