Product Overview
Translate Voltages for GPIO
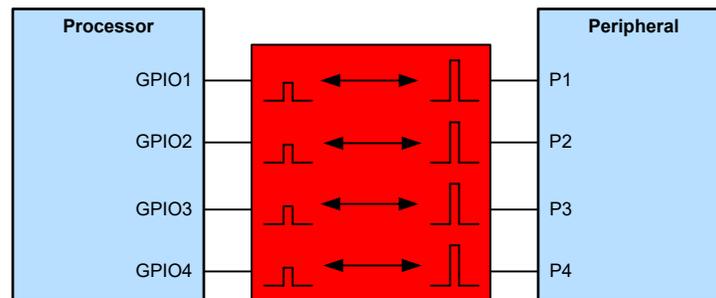
Example GPIO Voltage Translation Block Diagram

Design Considerations

- Translators enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Protect controller while peripheral is not connected
- [FAQ] What are the power sequencing requirements for the translation device?
- [FAQ] What should be done with unused I/O pins of the level translator devices?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

Recommended Parts

Part Number	AEC-Q100	Bits	Voltage Translation Range	Features
SN74LXC8T245		8	1.1 V–5.5 V	Schmitt-trigger inputs Dynamic pulldowns on I/O V_{CC} Isolation and V_{CC} Disconnect
SN74LXC8T245-Q1	✓			
TXU0104		4	1.1 V–5.5 V	Schmitt-trigger inputs Integrated pulldown resistors V_{CC} Isolation and V_{CC} Disconnect
TXU0104-Q1	✓			
SN74AXC2T45		2	0.65 V–3.6 V	Direction controlled Glitch-free power supply sequencing V_{CC} Isolation
SN74AXC2T45-Q1	✓			
SN74AXC1T45		1		
SN74AXC1T45-Q1	✓			

For more devices, browse through the *online parametric tool* where you can choose between the three types of translators.

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