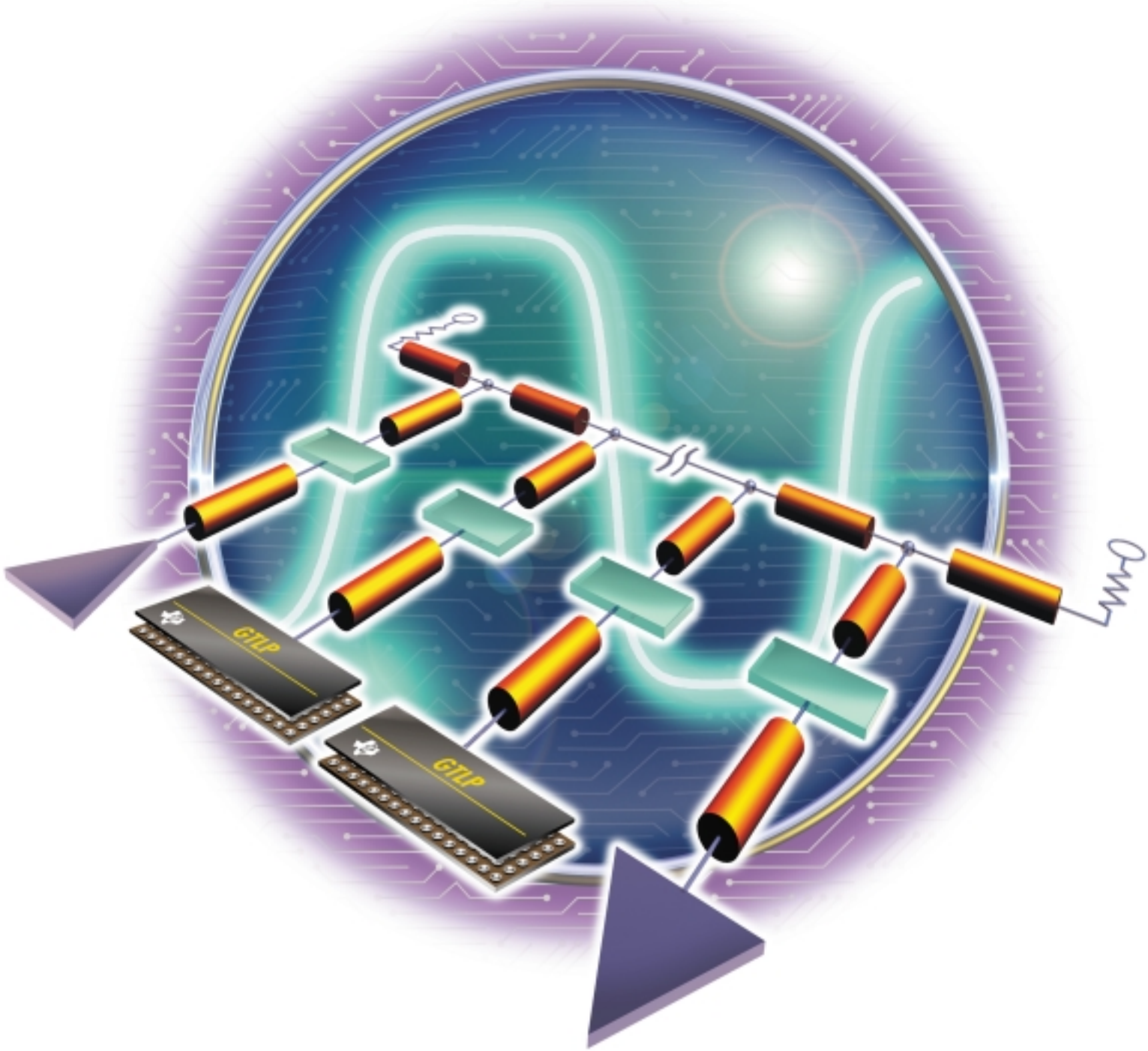
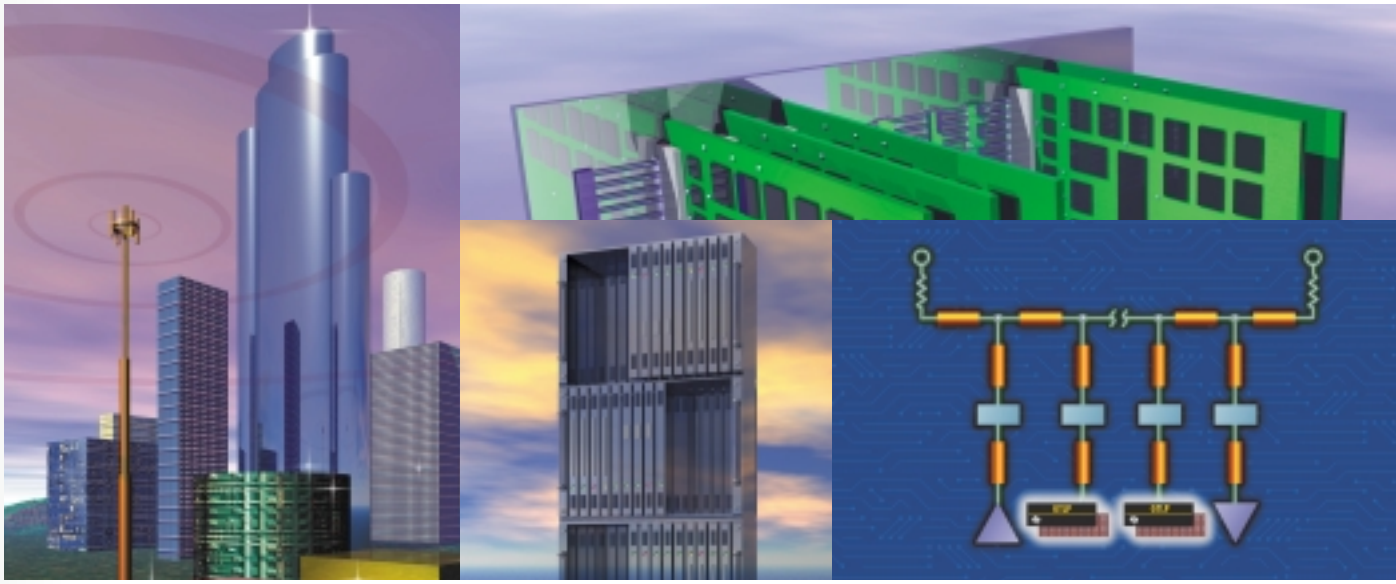
Increase the speed of parallel backplanes 3x with GTLP



For high-speed parallel backplanes, GTLP is the answer.

Users of the Internet, wireless communications or the traditional wireline infrastructure are clamoring for more bandwidth. As a result, the parallel backplanes used in switches, routers, hubs and other communications equipment is quickly evolving to faster speeds. GTLP logic is an easy first step toward higher data throughput.



Migrate to next-generation speed

In today's interconnected, bandwidth-hungry world, designers can easily increase by two to three times the data throughput speed of their networking, communications and telecommunications systems by migrating to TI's new GTL-Plus (GTLP) logic family for parallel backplanes. And since GTLP is backwardly compatible with traditional logic such as ABT, ALVT, LVT, LVC and FutureBus+, the migration to higher throughput is simple and direct.

Building upon its pioneering work with Gunning Transceiver Logic (GTL), TI has optimized the Output Edge Control™ circuitry and added live insertion and removal capabilities to produce devices specifically designed for medium and heavily loaded parallel backplanes.

GTLP brings the benefits of GTL – higher frequencies and lower EMI and transmission noise - to parallel backplanes in excess of 20 slots. Combining Output Edge Control circuitry with GTLP's narrow signal voltage swing gives GTLP clock speeds in excess of 80 MHz and data throughput rates of at least 3.2 gigabytes per second (Gbps) across a 32-bit backplane.

Improving on a good thing

In recent years, GTL logic has become increasingly popular in point-to-point applications and backplane systems with a limited number of slots. Now, GTLP brings the high-speed advantages of GTL to medium- and heavily loaded parallel backplanes.

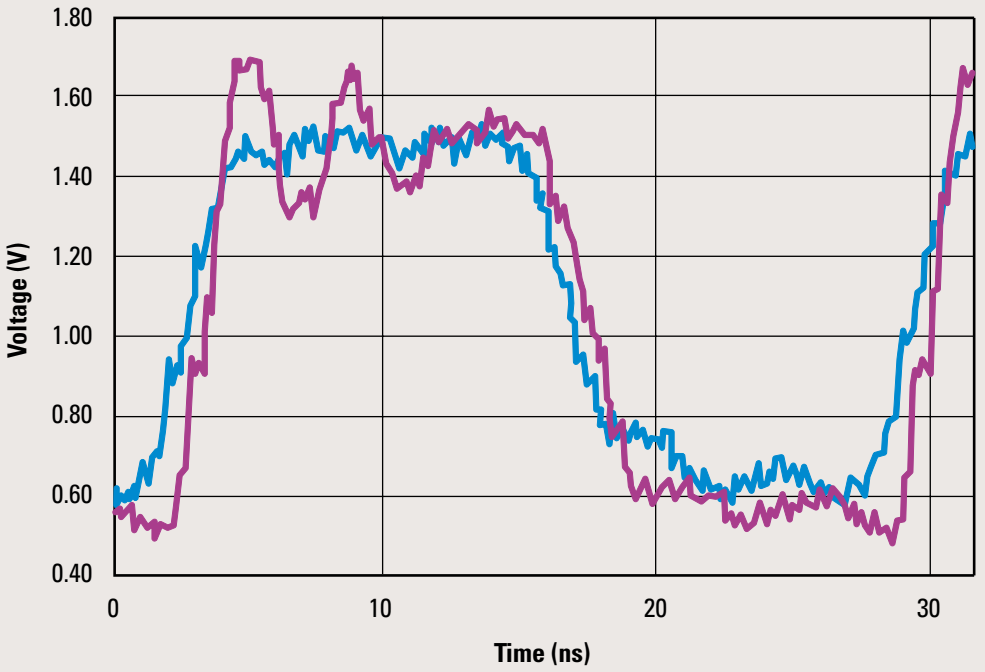
GTLP transceivers are differential input, open-drain n-channel devices. TI has optimized the Output Edge Control circuitry in GTLP transceivers to ensure good signal integrity (See chart below), reduce line reflections and limit the electromagnetic emissions at frequencies greater than 80 MHz.

GTLP devices have been optimized for a narrow signaling range between 0.55 and 1.5V with a threshold at 1.0V. Additionally, GTLP transceivers will operate at the GTL signal levels of 0.4 to 1.2V with a threshold at 0.8V.

GTLP transceivers are 3.3V CMOS devices, but they have 5V-tolerant LVTTL inputs and outputs which allows them to act as 5V-to-GTLP translators or 3.3V LVTTL-to-GTLP translators. As CMOS devices, GTLP transceivers consume less than a third of the power that is typical for BiCMOS GTL devices.

Designing GTLP transceivers into next-generation systems with significantly higher data throughput speeds is relatively easy because GTLP is backwards compatible with the logic currently used in parallel backplanes.

Output Edge Control (OEC™) Circuitry Comparison (V_{TT} = 1.5V)



Optimized OEC

Original OEC

The many packaging options as well as pin-outs that are similar to previous-generation devices simplify the designer's task.

Matching your backplane needs

For maximum flexibility in matching the needs of your backplane, the GTLP family comes in medium- and high-drive devices. High-drive devices sink 100 milli-Amperes (mA) of current, while medium-drive devices sink 50mA. Low impedance, heavily loaded backplanes achieve better data throughput performance with high-drive GTLP devices.

High-drive GTLP devices also feature TI's innovative variable edge rate control circuitry which allows you to adjust the signal's edge rate to better match the conditions of your backplane.

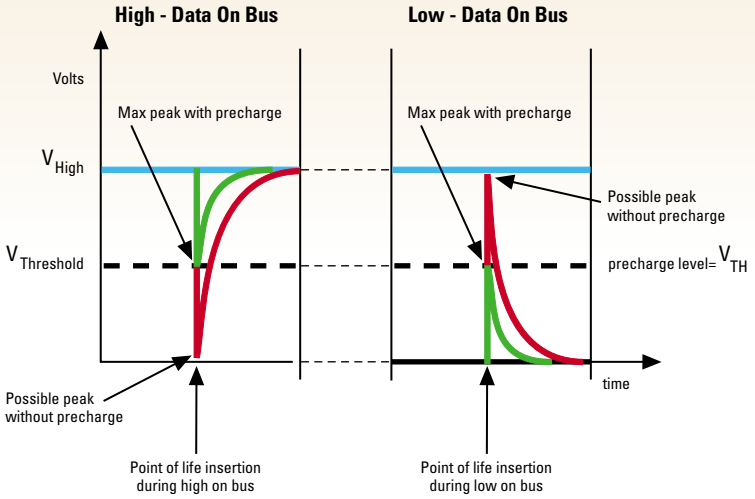
An Easy Migration

To help the designer make an easy migration to GTLP, this new logic family is fully supported with tools like application notes, application support, free samples, demonstration backplane models, and IBIS and SPICE simulation models.

Live board insertion

Many backplane systems are used in communication and networking applications where availability 24 hours a day, seven days a week (24/7) is a must. As a result, boards must be inserted or removed from the system while it is still running. TI has included three kinds of internal circuitry to accomplish fault-proof live insertion.

First, by including a blocking diode and removing a clamping diode, unexpected device behavior is eliminated when power is fully or partially removed. Second, new circuitry avoids driver conflict by ensuring that outputs are disabled during power up or down. And third, an internal pre-charging circuit prevents data corruption which can result from voltage spikes caused by inserting a board into a live backplane.



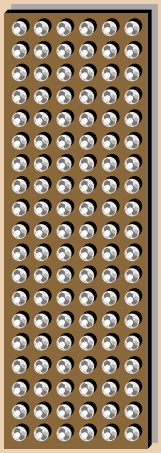
For more information on the GTLP family of high-speed parallel backplane logic or to find out how TI can help you make the switch to GTLP logic, visit our web site at **www.ti.com/sc/gtlp** ***or to reserve a copy of our GTLP Product Information book visit*** **www.ti.com/sc/gtlpbook.**

GTLP Chip Configurations

GTLP Device	*LVTTL-to-GTLP Function*	*Pin Count*	*SOIC*	*SSOP*	*TSSOP*	*TVSOP*	*LFBGA*
		Medium Drive (50 mA)					
SN74GTLP817	GTLP to LVTTL 1 to 6 Fanout Driver	24	✔		✔	✔	
SN74GTLPH306	8-Bit Bus Transceiver	24	✔		✔	✔	
SN74GTLPH16945	16-Bit Bus Transceiver	48		✔	✔	✔	
SN74GTLPH16912	18-Bit Universal Bus Transceiver	56		✔	✔	✔	
SN74GTLPH32945	32-Bit Bus Transceiver	96					✔
SN74GTLPH32912	36-Bit Universal Bus Transceiver	114					✔
		High Drive (100 mA)					
SN74GTLP1394	2-Bit 3-Wire Transceiver	16	✔		✔	✔	
SN74GTLPH1645	16-Bit Bus Transceiver	56		✔	✔	✔	
SN74GTLPH1655	16-Bit Universal Bus Transceiver	64			✔		
SN74GTLPH1612	18-Bit Universal Bus Transceiver	64			✔		
SN74GTLPH3245	32- Bit Bus Transceiver	114					✔

The Pluses of GTLP

- Two to three times faster data throughput on heavily loaded parallel backplanes
- 3.2 gigabits per second (Gbps) with a 32-bit backplane
- Easy migration path from traditional backplane logic like ABT, FCT, LVT, ALVT, LVC or FutureBus+
- Live insertion of cards into GTLP backplanes for high-availability systems
- Wide selection of high drive devices
- Wide selection of packaging options
- Consumes one-third the power of BiCMOS GTL devices



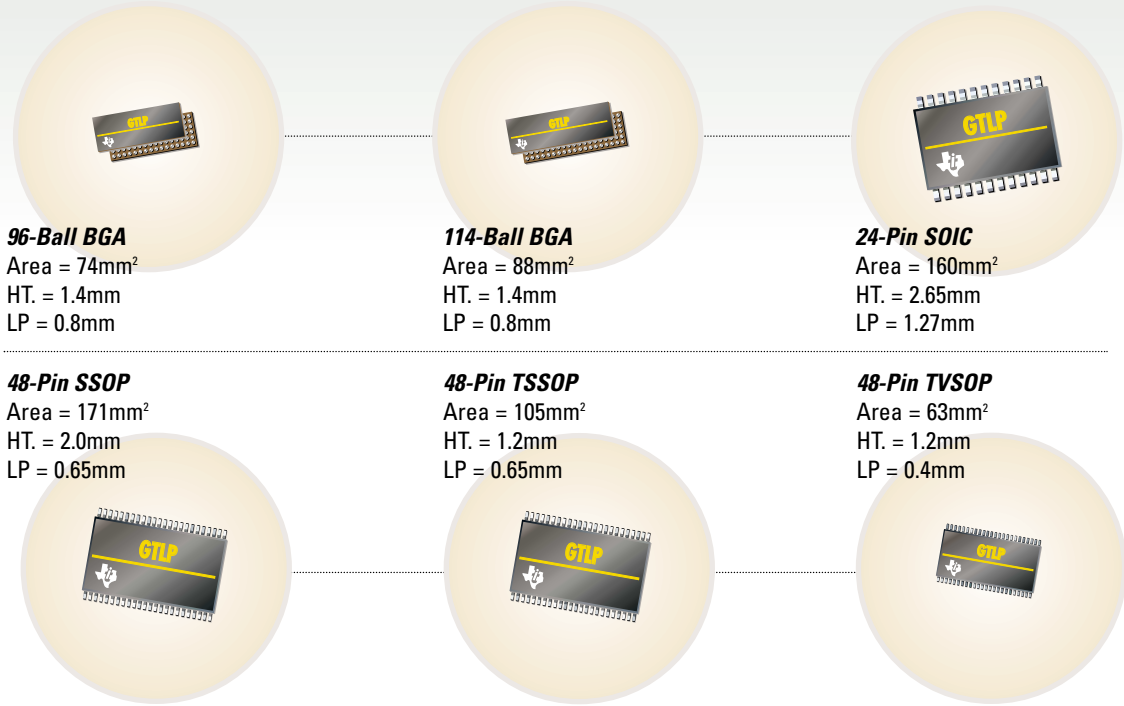
A wide range of GTLP packaging options is available to satisfy all design needs. TI's MicroStar BGA™ package reduces by 45 to 65 percent the board space needed for traditional surface mount packages.

With an easy migration to Texas Instruments' new Gunning Transceiver Logic-Plus (GTLP) family, designers can increase the data throughput of parallel backplane systems by 100 to 200 percent. GTLP extends the success of GTL logic in point-to-point applications to parallel backplane systems without requiring a radical redesign of the system.

And for high-availability systems in communications, telecommunications and networking, GTLP supports live insertion and removal of boards into a backplane.

Three times the speed - That's what a simple migration to GTLP logic can do for your parallel backplane system.

Packaging Options



96-Ball BGA
Area = 74mm²
HT. = 1.4mm
LP = 0.8mm

114-Ball BGA
Area = 88mm²
HT. = 1.4mm
LP = 0.8mm

24-Pin SOIC
Area = 160mm²
HT. = 2.65mm
LP = 1.27mm

48-Pin SSOP
Area = 171mm²
HT. = 2.0mm
LP = 0.65mm

48-Pin TSSOP
Area = 105mm²
HT. = 1.2mm
LP = 0.65mm

48-Pin TVSOP
Area = 63mm²
HT. = 1.2mm
LP = 0.4mm

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