Application Brief Using Serial Communications Within TPLD



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Why Use Serial Communications

The serial communication in TI's Programmable Logic Device (TPLD) enables the use of the USER register space. Using the USER register space allows for small adjustments of select fields, like counter blocks control data field, or can be used similar to I/O without having to go through device pins. The TPLD is currently only capable of being a The USER registers can be found under Detailed Description -> Device functional modes -> Programming -> "Device name" Registers -> "device name"_USER_REGISTER. For this application brief, the TPLD1202 is the device being used and any references to addresses are based on that devices USER register table.

Note

The USER register space is not the same as the configuration space. The USER register space does not allow for changing connections, or modifying the original design beyond select fields.

What is Available in the Register Space

Table 1 is an example of a USER register space. The table does not have all the options available in all devices, but is a large set of what can be available.

Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DEVICE_ID0				DEVICE	ID_MSB			
DEVICE_ID1				DEVICE	_ID_LSB			
DEVICE_ID2		DEVICE_ID_RSVD						
DEVICE_ID3		DEVICE_ID_REV						
DEVICE_ID4	DEVICE_ID4							
DEVICE_ID5	DEVICE_ID5							
DEVICE_ID6	DEVICE_ID6							
DEVICE_ID7				DEVIC	CE_ID7			
CNT0_COUNT				CNT0_	COUNT			
CNT1_COUNT				CNT1_	COUNT			
CNT2_COUNT				CNT2_	COUNT			
CNT3_COUNT				CNT3_	COUNT			
CNT4_COUNT_LSB				CNT4_CC	UNT_LSB			
CNT4_COUNT_MSB				CNT4_CC	UNT_MSB			
CNT5_COUNT_LSB				CNT5_CC	OUNT_LSB			
CNT5_COUNT_MSB				CNT5_CC	UNT_MSB			
CNT6_COUNT				CNT6_	COUNT			
CNT7_COUNT				CNT7_	COUNT			
CNT8_COUNT				CNT8_	COUNT			
CNT9_COUNT				CNT9_	COUNT			
CNT0_DATA				CNT0	_DATA			
CNT1_DATA				CNT1	_DATA			
CNT2_DATA				CNT2	_DATA			
CNT3_DATA				CNT3	DATA			
CNT4_DATA_LSB				CNT4_D	ATA_LSB			
CNT4_DATA_MSB				CNT4_D	ATA_MSB			
CNT5_DATA_LSB				CNT5_D	ATA_LSB			

Table 1. Example USER Registers



		Table 1. E	Example US	SER Register	s (continu	ued)		
Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT5_DATA_MSB				CNT5_DA	TA_MSB		1	1
CNT6_DATA				CNT6_I	DATA			
CNT7_DATA				CNT7_I	DATA			
CNT8_DATA				CNT8_I	DATA			
CNT9_DATA				CNT9_I	DATA			
WATCHDOG_TIMEOUT_DAT A		WATCHDOG_TIMEOUT_DATA						
WATCHDOG_OUTPUT_DATA	WATCHDOG_OUTPUT_DATA							
WATCHDOG_STATUS	WATCHDOG_STATUS							
PGEN_DATA_LSB				PGEN_DA	TA_LSB			
PGEN_DATA_MSB				PGEN_DA	TA_MSB			
STATE_MACHINE		RESERVED CURRENT_STATE						Ē
STATE0_OUT				STATE0	_OUT	•		
STATE1_OUT				STATE1	_OUT			
STATE2_OUT				STATE2	_OUT			
STATE3_OUT				STATE3	_OUT			
STATE4_OUT				STATE4	_OUT			
STATE5_OUT				STATE5	_OUT			
STATE6_OUT				STATE6	_OUT			
STATE7_OUT				STATE7	_OUT			
VREF_ACMP0				VREF_A	CMP0			
VREF_ACMP1				VREF_A	CMP1			
VREF_ACMP2				VREF_A	CMP2			
VREF_ACMP3				VREF_A	CMP3			
VREF_McACMP0_0				VREF_McA	CMP0_0			
VREF_McACMP0_1				VREF_McA	CMP0_1			
VREF_McACMP1_0				VREF_McA	CMP1_0			
VREF_McACMP1_1				VREF_McA	CMP1_1			
VREF_McACMP2_0				VREF_McA	CMP2_0			
VREF_McACMP2_1				VREF_McA	CMP2_1			
VREF_McACMP3_0				VREF_McA	CMP3_0			
VREF_McACMP3_1				VREF_McA	CMP3_1			
VIRTUAL_INPUT				VIRTUA	AL_IN			
VIRTUAL_OUTPUT				VIRTUAL	_OUT			
SER_COMM_CFG				RESERVED				ADDR_AUTOINC
CRC_STATUS		CRC_ERR_CNT	-		RES	ERVED		CRC_ERR_FLA G
SER_COMM_WR_MASK				SER_COMM_	WR_MASK			

The DEVICE_ID registers are used to create an identity for each design. The first 2 DEVICE_ID registers are set by the device depending on the device selected for example the TPLD1202 has 0x12 in DEVICE_ID0 and 0x02 in DEVICE_ID1 where as the TPLD2001 has 0x20 in DEVICE_ID0, and 0x01 in DEVICE_ID1. DEVICE_ID 4 - 7 are loaded at startup with the Program ID written in the system settings within InterConnect Studio.

Starting from address 0 to address 7 are identifiers of the device. This includes the device id which based on the TI product number, for example. The TPLD1202 has register at address 0x00 = 0x12, and address 0x01 = 0x02 where as the TPLD2001 has 0x20, and 0x01 respectively. After that in registers DEVICE_ID 4-7 are loaded at startup with the Program ID. What this means is reading from Addresses 0-7 can have an entirely unique value to each design created by the user. Reading those registers not only provide which device is being used, but also which design is currently being loaded.

The CNTx_COUNT registers are read only registers that reflect whatever the current count of a counter block is. This can be used to give a rough estimate of how long a counter has left before reaching zero. It's important to note that this read is asynchronous from the actual counter, so depending on when the value is read the counter can iterate before the value is return via the communication protocol.

The CNTx_DATA registers are read/write registers that store the value of control data written in InterConnect Studio. These values can be udated on the fly allowing the user to adjust PWM outputs, Increase/decrease delays, and adjust blocks like the frequency detectors on the fly.

The WATCHDOG portion of the register space allows the user to read the status, adjust the timeout period and output pulse length of the watchdog timer. The WATCHDOG_STATUS records how many times the watchdog has been triggered since startup or since the last read. This register is reset upon being read. Increasing the value in WATCHDOG_TIMEOUT_DATA increases the amount of time a signal can be low before an output pulse is triggered. Increasing the value of WATCHDOG_OUTPUT_DATA increases the length of the output pulse when the watchdog is triggered.

The STATE_MACHINE portion of the register space allows the user to control the current state and adjust each states behavior. SM_CURRENT_STATE contains the current state in binary format in bits 2-0. This is R/W so not only can the current state be read, but the serial controller can be used to force the state machine into certain states. This section also contains the state outputs listed as SM_S#_OUT_CFG. This allows the controller to adjust the outputs of any given state from this section.

the VREF portion of the register space allows the user to adjust the value going into the IN- of both multi-channel analog comparators and independent analog comparators. The value written here is not the value of the VREF, but rather what value the VREF is referencing. In the TPLD2001 the VREF steps by 32mV so increasing the value from 0x00 to 0x01 is changing that reference from 32mV to 64mV.

The VIRTUAL_INPUT register is used to store the values going into the TPLD device. This register is used to act as an optional inputs into the device. This can be used in place of pins to expand the output count of the controller.

The VIRTUAL_OUTPUT register is used to store the values going out of the TPLD device at any given time. Similar to the earlier CNT_COUNT registers mentioned above a read from this register is asynchronous, so after making the request and before the data is returned one of these values can possibly change.

The CRC_STATUS register is used to check if the device has started up correctly. The CRC_ERR_CNT section stores how many times the CRC process iterated before successful startup. The TPLD device is designed to run the CRC_ERR_CNT value up to 8 before full power on. If this value is at 8 and the CRC check fails the CRC_ERR_FLAG is flipped to 1. This register can be used to check if the design in the TPLD was successfully loaded, and if these values are unacceptable power cycle the device. If the device fails start-up again begin error analysis of your design attached to the TPLD.

The SER_COM_WR_MASK register is used to apply a mask over any future reads or writes. This can be used to read just the bottom half, or top half, of a register. The values not within the mask are all be read as 0 by the TPLD or returned as 0 to the controller.

How to Setup I2C or SPI Communication in a System.

Each TPLD has a specific set of pins that are tied to the serial communication which are initialized as the peripheral is added to the design. An example of a I2C setup can be seen in Figure 1, and an example SPI setup in Figure 2.





Figure 2. Example SPI Setup with TPLD1202

Figure 1. Example I2C Setup with TPLD1202



How to Setup I2C or SPI in InterConnect Studio

InterConnect Studio (ICS) is a software tool used to design, simulate, and configure the TPLD family of devices.

Figure 3 shows the initial setup of the I2C peripheral in InterConnect Studio. I2C can be added to the design by clicking the plus button indicated by the red arrow. The peripheral address is a binary value that can be used to statically set the address of this TPLD design. Below the peripheral address is a setting to enable an external pin-based address. Many I2C peripherals come with predefined addresses, but the TPLD does not, instead using these two settings allows many TPLDs to sit on an I2C bus without interfering with each other. Enabling the pin-based address allows for the peripheral address to be overwritten by the logic value present at the pin when the communication starts. The last setting unique to I2C is the Global Reset Listening which enables the device to be reset when a reset command is sent from the controller.

Programmable Filter (+) Pulse Width Modulator (+)		
Shift Register 🕀		
VCC (+)	001 ((01 Pirc0)	
Voltage Reference 🔶	SCL (IOT PIN:3)	
Watchdog Timer 🕀	SCL SCL	
✓ INTERFACES (2)		
I2C Receiver 1/1 🥑 🕀 🖣	SDA (IO2 PIn:4)	
SPI Receiver 🕀	IN4 IN5	
 SETTINGS (2) 	IN6 IN7	
Simulation 1/1 🥑 🕀	i2c0	
System Settings 🛛 1/1 🥑 🕀		
	I2C RECEIVER ®	9 E
	This block is not simulatable	
	Name	i2c0
	Label	
	Peripheral Address	Enter Binary value
	Use GPIO Instead of Bits in Address	Use GPIO input rather than register set address 🔹
	Global Reset Listening	
	Use Virtual Inputs	Selected virtual inputs will disable equivalent GPIO 🔹
	Device MacroCell Allocated	Any(SERIAL_COMMS)

Figure 3. Default I2C in ICS

SPI has fewer options as SPI is not an addressable protocol as shown in Figure 4. The shared option of Virtual Inputs is used to allow the device to view the VIRTUAL_INPUT register. In some TPLD family devices the virtual inputs take the place of some pins as input to the connection matrix, and checking the data sheet clarifies which inputs are unable to be used together. For example in the TPLD1202 VIR_IN0 is shared with IO1 as shown in Table 2, meaning that IO1 cannot be used as an input pin into the design if VIR_IN0 is selected.





Figure 4. Default SPI in ICS



Virtual input	VIR_IN0	VIR_IN1	VIR_IN2	VIR_IN3	VIR_IN4	VIR_IN5	VIR_IN6	VIR_IN7
Digital Input Pin	IO1	102	103	104	105	106	107	109

Building a Design Around I2C

A simple implementation of I2C can be using the TPLD1202 as an I/O expander as shown in Figure 5. Three pins are being used as digital inputs and being fed into the input side of the block. These pins are going to feed values into the VIRTUAL_OUTPUT register to be read during operation. Four pins are being used as digital outputs of the device, and are connected to VIR_IN0, VIR_IN1, VIR_IN2, VIR_IN3. These pins reflect the value present in the VIRTUAL_INPUT register, for example, pin4 (IO6) reflects bit 0 so on and so forth.

There is a PWM being run at 50% duty cycle by default. The KEEP input is held high so the duty cycle never changes unless the value of CNT_DATA is overwritten.





Figure 5. IO Expander With Pulse Width Modulation

The setup for operation is shown in Figure 6 with the logic analyzer connections excluded. The TPLD-PROGRAM is used to update the design without requiring a burn of the device. Internal pull-ups are used within the USB2ANY during messaging.





Figure 6. TPLD1202 to a USB2ANY

To write to pins 4 to 7 we write the values to the internal address of VIRTUAL_INPUT (address: 0xE0). The USB2ANY explorer setup can be viewed in Figure 7, and an example of the operation can be viewed in Figure 8. The address entered into the Slave Address box appears different from the design because in the TPLD1202 the I2C receiver only uses 4 bits while the USB2ANY uses a 7 bit address. The address value entered has to be shifted to the left 3 bits from the value entered into ICS for the TPLD to be recognized. The only changes between commands was changing the value in the write data section before selecting Write.



dapter connection						
Type: USB2ANY F	Rev:	Serial #	F1BA	1851050	02000 Firmware Version: 2,8,2,0	Close Device
ebug I2C						-
Slave Address		Inter	rnal Address	s (Hex) –	Bus Timeout	Select Interface
0x18 Use 0x p hex slave	orefix for address	E	EO	1	÷ bytes 10 ▼ ms.	
-Bit Rate (KHz) - C	ptions] <u> </u>	
400 👻	🔲 10-bit a	ddress	🔽 Enal	ole pullup	S Free Bus	3.3V ON
Message / Data						
Write data:					1:1	5.0V OFF
					I and I Write	
00					Lodu Write	
					Save	
					Save	
					Save	
					Save	
Pead data:					Save	
Read data:					Save	
Read data:					Save Save Read	
Read data:					Save Save Read	
Read data:					Save Save Read	
Read data:					Save Save 0 bytes	
Read data:					Save Save Read 0 bytes	
Read data:					Save Save Read O bytes Clear Data	
Read data:					Save Save Read 0 bytes Clear Data	Log Comment
Read data:					Save Save Read 0 bytes Clear Data	Log Comment
Read data:					Save Save Read 0 bytes Clear Data	Log Comment
Read data:	Module	R/W	Addr	Len	Save Save Read 0 bytes Clear Data	Log Comment
Read data: Read data: vity Log: nestamp 24-12-19 13:26:14.179	Module		Addr	Len	Save Save Read 0 bytes Clear Data Data/Message Target Power: 3.3v is ON, 5.0v is OFF, Adj is O	Log Comment
Read data: Read data: vity Log: mestamp 24-12-19 13:26:14.179 24-12-19 13:26:15.283	Module	R/W	Addr 0x0018	Len	Save Save Read 0 bytes Clear Data Data/Message Target Power: 3.3v is ON, 5.0v is OFF, Adj is 0 Data: 0F	Log Comment
Read data: Read data: vity Log: mestamp 24-12-19 13:26:14.179 24-12-19 13:26:15.283 24-12-19 13:26:26.962	Module INFO I2C I2C I2C	R/W Write Write	Addr 0x0018 0x0018	Len 1	Save Read 0 bytes Clear Data Target Power: 3.3v is ON, 5.0v is OFF, Adj is 0 Data: 0F Data: 0A	Log Comment
Read data: Read data: vity Log: mestamp 24-12-19 13:26:14.179 24-12-19 13:26:26.962 24-12-19 13:26:42.442	Module INFO I2C I2C I2C I2C	R/W Write Write	Addr 0x0018 0x0018 0x0018	Len 1 1 1	Save Save O bytes Clear Data Data/Message Target Power: 3.3v is ON, 5.0v is OFF, Adj is 0 Data: OF Data: OF Data: 0A Data: 09	Log Comment
Read data: Read data: vity Log: mestamp 24-12-19 13:26:14.179 24-12-19 13:26:15.283 24-12-19 13:26:26.962 24-12-19 13:26:42.442 24-12-19 13:26:42.585	Module INFO I2C I2C I2C I2C ERROR	R/W Write Write	Addr 0x0018 0x0018 0x0018 0x0018	Len 	Save Save Read O bytes Clear Data Data/Message Target Power: 3.3v is ON, 5.0v is OFF, Adj is 0 Data: 0F Data: 0A Data: 09 Receive buffer is empty	Log Comment
vity Log: mestamp 24-12-19 13:26:14.179 24-12-19 13:26:5283 24-12-19 13:26:42.442 24-12-19 13:26:42.585 24-12-19 13:26:42.585 24-12-19 13:27:11.384	Module INFO I2C I2C I2C I2C I2C I2C I2C I2C	R/W Write Write Write	Addr 0x0018 0x0018 0x0018 0x0018	Len 1 1 1 1	Save Save Read O bytes Clear Data Data/Message Target Power: 3.3v is ON, 5.0v is OFF, Adj is 0 Data: 0F Data: 09 Receive buffer is empty Data: 00	Log Comment
Read data: Read data: Imestamp 24-12-19 13:26:14.179 24-12-19 13:26:15.283 24-12-19 13:26:42.42 24-12-19 13:26:42.442 24-12-19 13:26:42.585 24-12-19 13:26:16.263	Module INFO I2C I2C I2C I2C I2C I2C I2C I2C	R/W Write Write Write Write	Addr 0x0018 0x0018 0x0018 0x0018	Len 1 1 1 1 1	Save Save Read O bytes Clear Data Clear Data Data: OF Data: OF Data: 0A Data: 00 Data: 0A	Log Comment
Read data: Read data: rivity Log: mestamp 24-12-19 13:26:14.179 24-12-19 13:26:5.283 24-12-19 13:26:42.422 24-12-19 13:26:42.442 24-12-19 13:26:42.585 24-12-19 13:26:16.263 24-12-19 13:56:16.263 24-12-19 13:56:21.850	Module INFO I2C I2C I2C ERROR I2C I2C I2C I2C I2C I2C I2C	R/W Write Write Write Write Write	Addr 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018	Len 1 1 1 1 1 1	Save Save Read O bytes Clear Data Clear Data Data: OF Data: OF Data: 00 Data: 0A Data: OF	Log Comment
Read data: Read data: mestamp 24-12-19 13:26:14.179 24-12-19 13:26:15.283 24-12-19 13:26:42.442 24-12-19 13:26:42.442 24-12-19 13:26:42.442 24-12-19 13:26:42.53 24-12-19 13:56:16.263 24-12-19 13:56:21.850 24-12-19 13:56:30.070	Module INFO I2C I2C I2C ERROR I2C I2C I2C I2C I2C I2C I2C I2C	R/W Write Write Write Write Write Write Write	Addr 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018	Len 1 1 1 1 1 1 1 1	Save Read 0 bytes Clear Data Clear Data Data/Message Clear Data Target Power: 3.3v is ON, 5.0v is OFF, Adj is 0 Data: 0F Data: 0A Data: 09 Receive buffer is empty Data: 0A Data: 0F Data: 0F Data: 0A Data: 0A Data: 0A Data: 0F Data: 0F Data: 01	OFF
Read data: Read data: rivity Log: nestamp 24-12-19 13:26:14.179 24-12-19 13:26:15.283 24-12-19 13:26:42.442 24-12-19 13:26:42.585 24-12-19 13:26:12.855 24-12-19 13:56:12.855 24-12-19 13:56:12.850 24-12-19 13:56:30.070 24-12-19 13:56:37.540	Module INFO I2C I2C I2C I2C I2C I2C I2C I2C I2C I2C	R/W Write Write Write Write Write Write Write	Addr 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018	Len 	Save Read 0 bytes Clear Data Clear Data Data/Message Clear Data Target Power: 3.3v is ON, 5.0v is OFF, Adj is 0 Data: 0F Data: 0P Receive buffer is empty Data: 0A Data: 0P Data: 0F Data: 01 Data: 09	Log Comment

Figure 7. USB2ANY Explorer Write to VIRTUAL_INPUT

10 s +20 s +30 s +40 s 0 0 101 s +20 s +30 s +40 s = 12C ⊗	
D0 101	
tcc-sql Trigger View A	<u>م</u>
Data 🕐 🥥	
n 102 ja ja ja ja ja ja vrite to okis	ack data: 0xE0 0x0A ack data: 0xE0 0x0F
write to 0x35 write to 0x35	ack data: 0xE0 0x01 ack data: 0xE0 0x09
write to 0x18	ack data: 0xE0 0x06
02 IO6 (OUTO)	
D3 ID5 (0/TT)	
D4 104 (0012	
es 103 (0013)	

Figure 8. Waveform of Writing to Pins

To read from pins 0 to 2 we first do an empty write to the register VIRTUAL_OUTPUT (address: 0xE1) then execute a read command to the device. The USB2ANY explorer setup can be viewed in Figure 9, and an example of the operation can be viewed in Figure 10

apter connection ype: USB2ANY Rev:	Serial #; F1BA1B5105002000	Firmware Version: 2,8,2,0	Close Dev
ug I2C	Internal Address (Hex)	Bus Timeout	Select Inter
0x18 Use 0x prefix hex slave addr	for E1 1 - bytes	50 v ms.	
3it Rate (KHz) Options 400 10	o-bit address 🔽 Enable pullups	Free Bus	3.3V C
Message / Data Write data:	1:0	Lood Write	5.0V O
		Save	
l Read data:			
07		Save Read	
		Clear Data	

Figure 9. USB2ANY Explorer Read From VIRTUAL_OUTPUT





Figure 10. Waveform of Reading From Pins

Lastly to adjust the PWM write a new value to the register CNT6_DATA (address: 0x26). The USB2ANY explorer setup can be viewed in Figure 11, and an example of the operation can be viewed in Figure 12



wapter connection	10 - 10		54 54			1
Type: F	Rev:	Serial #:	: No dev	/ice conr	nected Firmware Version:	Open Device
bug I2C						
Slave Address		Inter	rnal Address	(Hex) -	Bus Timeout	Select Interfaces
0x18 Use 0x p hex slave	orefix for e address	2	26	1	± bytes 10 ▼ ms.	
Bit Rate (KHz)C	Options					
400 -	🔲 10-bit a	ddress	🔽 Enat	ole pullup	ree Bus	3.3V OFF
Message / Data						
Write data:					1:1	5.0V OFF
					Save	
Read data:					Save Save Read bytes	
Read data:					Save Save Read 0 bytes Clear Data	Log Comment
Read data:	Module	R/W	Addr	Len	Save Save Read 0 bytes Clear Data Data/Message	Log Comment
Read data: ///////////////////////////////////	Module	R/W Write	Addr 0x0018	Len 1	Save Save Read 0 bytes Clear Data Data/Message Data: OF	Log Comment
Read data: Read data: vity Log: mestamp 24-12-19 13:56:21.850 24-12-19 13:56:30.070	Module I2C I2C	R/W Write Write	Addr 0x0018 0x0018	Len 1	Save Save Read 0 bytes Clear Data Data/Message Data: OF Data: 01	Log Comment
Read data: vity Log: nestamp 24-12-19 13:56:21.850 24-12-19 13:56:30.070 24-12-19 13:56:37.540	Module I2C I2C I2C I2C	R/W Write Write Write	Addr 0x0018 0x0018 0x0018	Len 1 1	Save Save Save Read 0 bytes Clear Data Clear Data Data/Message Data: 0F Data: 01 Data: 09	Log Comment
Read data: Read data: vity Log: nestamp 24-12-19 13:56:21.850 24-12-19 13:56:30.070 24-12-19 13:56:37.540 24-12-19 13:56:46.030	Module I2C I2C I2C I2C I2C	R/W Write Write Write	Addr 0x0018 0x0018 0x0018 0x0018 0x0018	Len 1 1 1 1	Save Save Save O bytes Clear Data Data/Message Data: 0F Data: 01 Data: 09 Data: 06	Log Comment
Read data: Read data: vity Log: mestamp 24-12-19 13:56:21.850 24-12-19 13:56:30.070 24-12-19 13:56:37.540 24-12-19 13:56:46.030 24-12-19 14:09:30.218	Module I2C I2C I2C I2C I2C I2C	R/W Write Write Write	Addr 0x0018 0x0018 0x0018 0x0018	Len 1 1 1 1	Save Save Read O bytes Clear Data Data/Message Data: 0F Data: 0F Data: 01 Data: 09 Data: 06 I2C internal address changed to 26	Log Comment
Read data: Read data: vity Log: nestamp 24-12-19 13:56:21.850 24-12-19 13:56:37.540 24-12-19 13:56:46.030 24-12-19 13:56:46.030 24-12-19 14:09:30.218 24-12-19 14:09:43.664	Module I2C I2C I2C I2C I2C I2C I2C	R/W Write Write Write Write	Addr 0x0018 0x0018 0x0018 0x0018 0x0018	Len 1 1 1 1 1 1	Save Save Save Read O bytes Clear Data Data/Message Data: 0F Data: 0F Data: 01 Data: 06 I2C internal address changed to 26 Data: FF	Log Comment
Read data: Read data: vity Log: nestamp 24-12-19 13:56:21.850 24-12-19 13:56:30.070 24-12-19 13:56:46.030 24-12-19 13:56:46.030 24-12-19 14:09:30.218 24-12-19 14:09:54.982	Module I2C I2C I2C I2C I2C I2C I2C I2C I2C I2C	R/W Write Write Write Write Write	Addr 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018	Len 1 1 1 1 1 1 1	Save Save Read O bytes Clear Data Data/Message Data: 0F Data: 0F Data: 01 Data: 09 Data: 06 I2C internal address changed to 26 Data: 03	Log Comment
Read data: Read data: vity Log: nestamp 24-12-19 13:56:21.850 24-12-19 13:56:30.070 24-12-19 13:56:37.540 24-12-19 13:56:46.030 24-12-19 14:09:30.218 24-12-19 14:09:54.982 24-12-19 14:09:54.982 24-12-19 14:10:10.425	Module 12C 12C 12C 12C 12C 12C 12C 12C	R/W Write Write Write Write Write Write	Addr 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018	Len 1 1 1 1 1 1 1 1	Save Read Save Read 0 bytes Clear Data Clear Data Data/Message Clear Data Data: 0F Clear Data Data: 0F Clear Data Data: 06 I2C internal address changed to 26 Data: FF Data: 03 Data: 80 Data: 80	Log Comment
Read data: Read data: vity Log: nestamp 24-12-19 13:56:21.850 24-12-19 13:56:30.070 24-12-19 13:56:37.540 24-12-19 13:56:46.030 24-12-19 14:09:30.218 24-12-19 14:09:54.982 24-12-19 14:09:54.982 24-12-19 14:10:10.425 24-12-19 14:10:10.425 24-12-10 14:10:10.425 24-12-10 14:10:10.425 24-12-10 14:10.425 24-1	Module I2C I2C I2C I2C I2C I2C I2C I2C I2C I2C	R/W Write Write Write Write Write Write	Addr 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018 0x0018	Len 1 1 1 1 1 1 1 1 1	Save Read Save Read 0 bytes Clear Data Clear Data Data/Message Clear Data Data: 0F Clear Data Data: 0F Clear Data Data: 0F Clear Data Data: 0F Clear Data Data: 09 Data: 06 I2C internal address changed to 26 Data: 07 Data: 03 Data: 80 Closed USB2ANY S/N F1BA 1B5105002000 Closed USB2ANY S/N F1BA 1B5105002000	Log Comment

Figure 11. USB2ANY Explorer Write to CNT6_DATA





Figure 12. Waveform of Adjusting PWM

Ordering Information

Hardware used in support of this document can be found in Table 3

Table 3. Ordering Information					
Device	EVM				
All TPLD	TPLD-PROGRAM				
TPLD1202	TPLD1202-DYY-EVM TPLD1202-RWB-EVM				
N/A	USB2ANY				

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