Application Brief

From Bottleneck to Breakthrough: QSPI Optimization in Data Centers with TXB0604/TXB0606

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Introduction

TI's TXB0604/ TXB0606 effectively solves redriving challenges and operating voltage mismatches in Controller/ Flash applications using serial Quad-SPI communication. Its strong AC driving capability allows designers to improve margin while maintaining robust processor-to-flash communication without sacrificing clock speed. These devices help mitigate transmission-line related signal integrity issues and enable more stable, higherperformance system designs by supporting data rates above 50MHz and 100Mbps while tolerating up to 100pF capacitive loading per channel.

The data center infrastructure of today relies on servers and advanced computing systems capable of high-speed communication to verify maximum processing efficiency. To prevent bottlenecks at the data handling side, host devices often leverage external non-volatile memory to resolve limited on-board memory, for example a Baseband Management Controller (BMC) paired with a NOR Flash.

For such memory-intensive data transfers, Quad-SPI (QSPI) is used as the serial communication interface between the two parties during specific commands such as power cycle/ reset. This interface is often used to hold FPGA firmware, system BIOS images and other system configuration parameters, allowing systems to reduce boot times and accelerate startup. Compared to standard SPI, which uses four channels with only two fixed, full-duplex data lanes, QSPI uses six channels with up to four half-duplex bidirectional data lanes, enabling significantly higher throughput.

A similar interface, enhanced SPI (eSPI) developed by Intel, leverages this serial bus for system-level communication between host and peripherals over the memory-based interface between host and Flash. eSPI serves as a high speed, low pin count bus interface to replace traditional SPI and other sideband signals often used to interface different platforms between server and client sides.

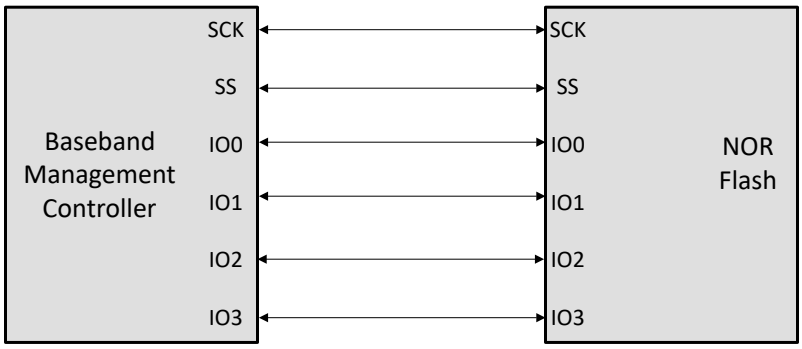

Figure 1. Quad-SPI Application Example Block Diagram

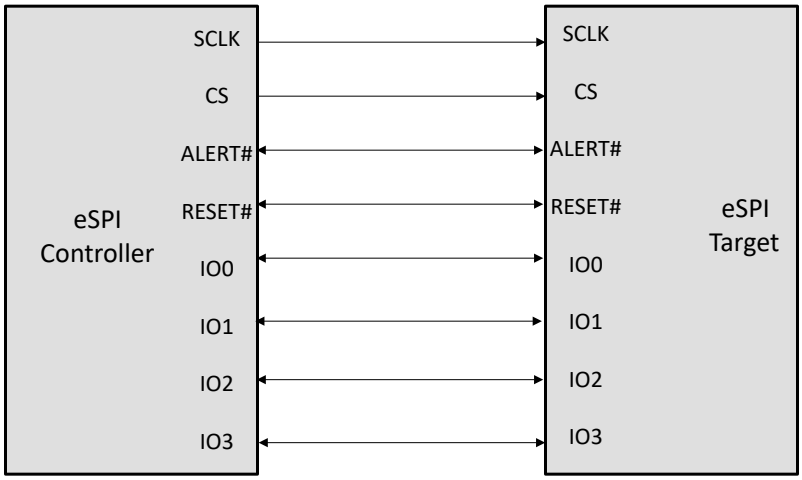

Figure 2. eSPI Application Example Block Diagram

Designers often face constraints that prevent placement of processors and PHYs next to each other due to board design limitations. This results in instances where the two parties are separated by long connectors in-between the motherboard and daughter card. As a result, parasitic capacitances stemmed from the transmission line can prevent the QSPI bus from operating at desired speeds which can serve to be a bottleneck for the operating system. While most cases involve a point-to-point connection between controller and Flash, there are instances where multiple MUX devices and long connector lengths are used in between. In this situation, the combination of all individual C_{IO} capacitances along the QSPI bus severely degrades signal integrity as the bus becomes overloaded. These slower edge rates reduces noise margin, and creates serious signal-integrity challenges. As a result, designers are forced into repeated termination tuning, routing optimization, or even costly board re-spins just to stabilize the interface.

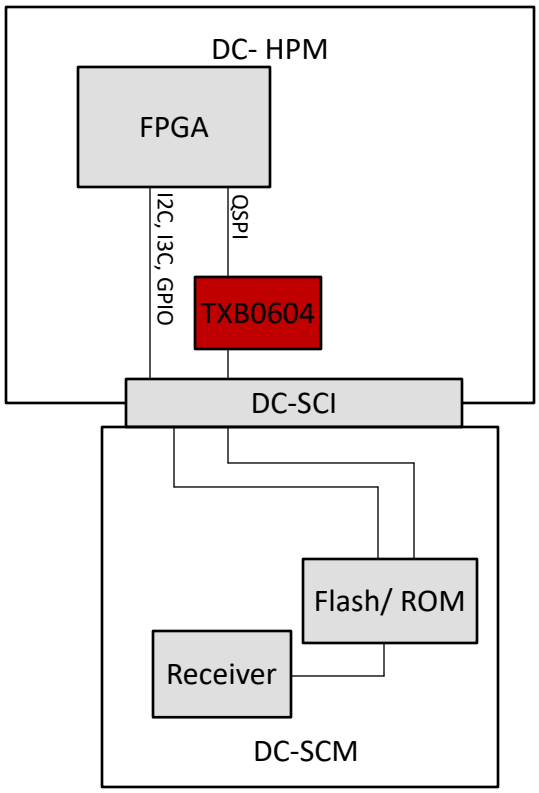

Figure 3. TXB0604 Used in Between FPGA to Flash Memory

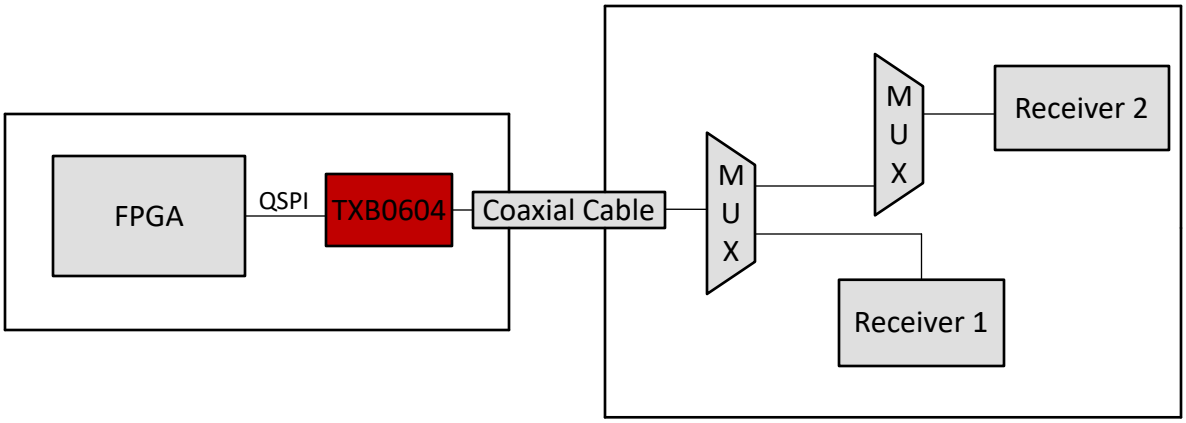

Figure 4. FPGA Connection to Multiple Receivers Downstream

If a datacenter module is using a CPU to attempt to read from ROM that stores BIOS settings and long trace lengths were used in-between, data processing speeds can be limited due the to signal integrity concerns exhibited by the transmission line. The prolonged downtimes and slower boot times increase transfer latency and adding debug and validation overhead.

Until now, engineers were limited to two options: redesigning board layouts for shorter trace lengths or reducing serial bus bandwidth. The TXB0604 and TXB0606 now provide a third option, offering the capability to overcome this system limitation.

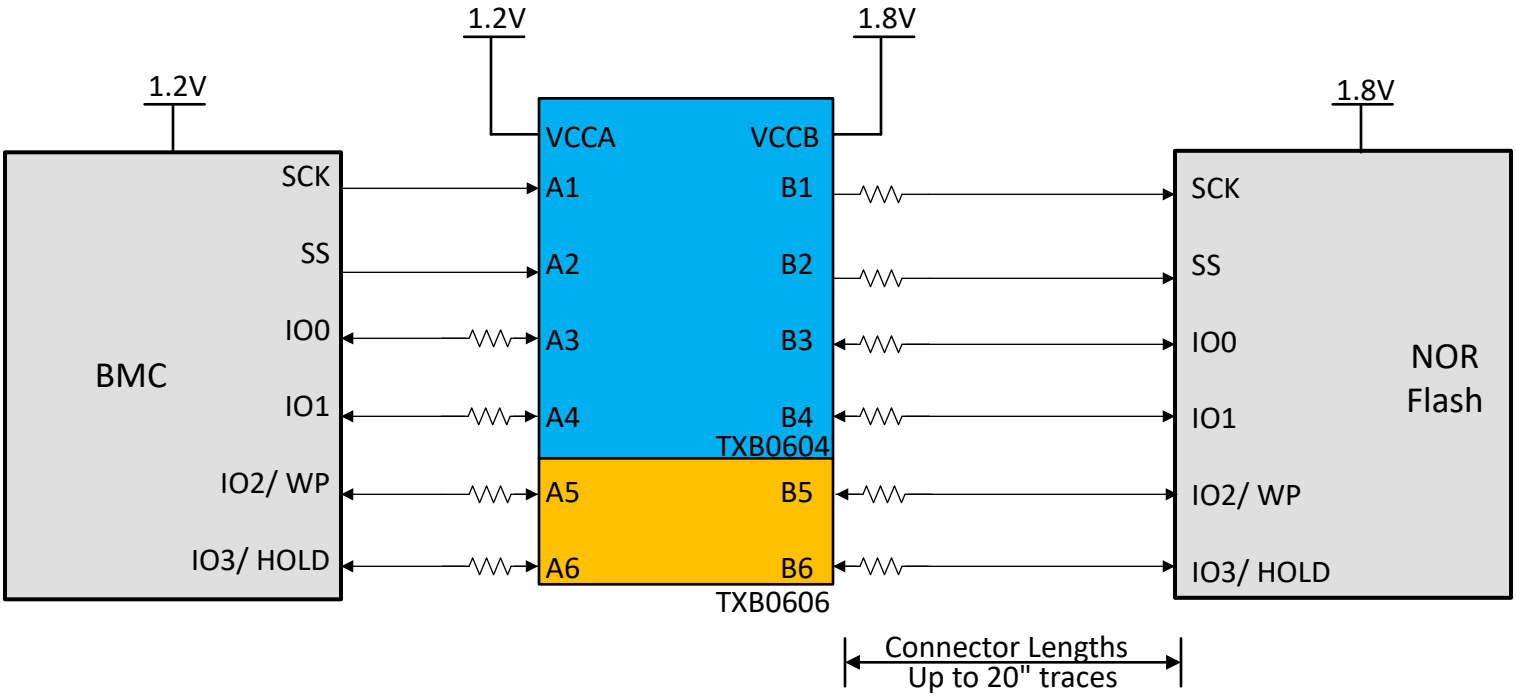

Figure 5. TXB0604, TXB0606 Diagram

Table 1.

	Device		
Spec	TXB0104	TXB0604	TXB0606
Channel Count	4	4	6
Operating Voltage (V_{CCA}, V_{CCB})	1.2V-3.6V 1.65V-5.5V	0.9V-2V 1.65V-3.6V	
Max Data Rate (1.8V to 3.3V, Cload= 15pF)	30MHz/ 60Mbps	87.5MHz/ 175Mbps	
Max Data Rate (1.8V to 3.3V, Cload= 100pF)	Not Characterized/ Not Designed For	57.5MHz/ 115Mbps	
Design Considerations	• Sensitivity to output loads >70pF • External series resistors suggested when pairing with long cabling • Input driving Requirement: +/- 2mA • $V_{CCA} \leq V_{CCB}$	• Supports 100pF output loads while sustaining high data rate • External series resistors suggested when pairing with long cabling • Input driving Requirement: +/- 3mA • $V_{CCA} \leq,=, \geq V_{CCB}$ • Direction change wait time (Tdcw) must be considered.	

Summary

As enterprise applications grow increasingly memory-intensive, achieving higher QSPI throughput while maintaining signal integrity has become a critical design challenge. Voltage mismatches and insufficient buffering along the signal path have long been pain points with limited designs besides degrading bandwidth and redesigning entire systems. This application brief explores how the TXB0604 and TXB0606 addresses these gaps, offering system designers a practical design to overcome redriving and level-shifting needs without sacrificing performance.

References

- Texas Instruments, *Overcoming TXB-Type Translators Design Challenges*, application note.
- Texas Instruments, *TXB0604 Auto-Bidirectional Level Translator for High-Speed Interfaces*, datasheet.
- Texas Instruments, *Enabling SPI-Based Flash Memory Expansion by Using Multiplexers*, application brief.

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