Application Note

Design of Insulation Monitoring Device (IMD) in On-Board Charger System With Active Single-Switch Architecture

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ABSTRACT

An insulation monitoring device (IMD) is a new requirement in bidirectional on-board charger (OBC) systems. This document focuses on the design considerations of the active single-switch IMD architecture, including the hardware and software design and the optimization of the hardware and software implementation. The simulation results are provided to verify the performance and provide a reference for designing an IMD configuration.

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1 Introduction

1.1 Background

As electric vehicle designs continue to implement higher battery voltages, isolating the high-voltage (HV) components to the protective earth through high-ohmic paths is crucial to safety. The IMD circuit is used to monitor insulation resistance and reports failures in cases of insufficient insulation resistance.

For unidirectional OBC, the existing IMD circuits in the battery management system (BMS) or charging station cover insulation monitoring. However, in a bidirectional OBC application, the IMD circuits in the BMS and charging station are not connected to the system in a vehicle-to-load (V2L) or vehicle-to-vehicle (V2V) configuration. The IMD circuit must be implemented on the AC side of the on-board charger to cover the V2L and V2V scenarios.

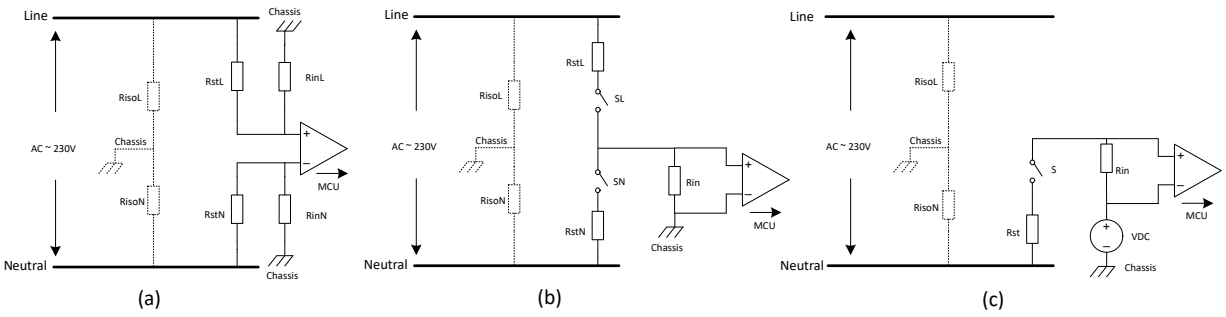
The main IMD architectures and typical requirements are elaborated on in the references section [1]. The architecture block diagrams are shown in Figure 1-1 and the comparison table is shown in Table 1-1.
Active single-switch architecture has several benefits compared to other architectures, making the architecture especially applicable in bidirectional OBC use-cases. Active single-switch architectures:

- Detect both symmetrical and asymmetrical insulation failures, which is usually required by safety standards.
- Operate without AC grid voltage. In a bidirectional OBC application, usually the insulation resistance must be monitored before the vehicle is connected to the load. At this time, the OBC has not yet output power to loads in the AC side, there is no AC voltage between the line and neutral.
- Costs are potentially reduced for implementing the isolation. Since the OBC usually forms a two-in-one system with the high-voltage to low-voltage (HVLV) DC-DC converter, the low-voltage battery side has a microcontroller (MCU). If the MCU on the low-voltage battery side is used for insulation monitoring, the IMD circuit does not require galvanic isolation. For other architectures, because the AC voltage sensor is usually based on the AC side rather than the low-voltage (LV) side, the IMD circuit usually needs to be done using the MCU on the AC side, which requires galvanic isolation.

The accuracy of active single-switch architectures is less affected by the Y capacitor. The impact of a Y capacitor is elaborated on in the references section [1], which includes two parts:

- The influence of the settling time during the transient state
- The influence of the phase delay during the steady states

The Y capacitor and insulation resistance form an RC series-parallel circuit. If an AC voltage is applied, the Y capacitor causes a phase shift between the voltage across the resistor and the AC power supply. The larger the Y capacitor, the greater the phase shift. If a DC voltage is applied, as long as the charging time is sufficient, the voltage across the resistor is less affected by the Y capacitor.



A. Basic architecture
B. Dual switches architecture
C. Active single switch architecture

Figure 1-1. Block Diagram of Different IMD Architectures

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Table 1-1. Architecture Comparison Table

Architecture		Basic	Dual Switches	Active Single Switch
Components		Op-amp × 1	Switch × 2 + Op-amp × 1	Switch × 1 + Op-amp × 1 + DC bias * 1
Accuracy		Low	High	Medium
Relative software complexity		Low	High	Medium
Potential cost		Low	High	Medium
Influence of Y capacitor		High	Medium	Low
Features	Symmetric and asymmetric fault	No	Yes	Yes
	Detect fault location	Yes	Yes	No
	Calculate insulation resistance	No	Yes	No
	Operate without AC grid voltage	No	No	Yes

This document introduces the design steps, elaborates on the specific design details and key design considerations of an active single-switch architecture. Simulation results are provided to verify performance.

1.2 Operation Principle

Figure 1-2 shows the block diagram and the equivalent circuit of the active single-switch architecture. The red line and blue line are the AC line and AC neutral respectively. R_{isoL} is the insulation resistance between the line and PE. R_{isoN} is the insulation resistance between the neutral and PE. This insulation resistance must be monitored, to maintain proper isolation between the AC voltage and PE.

R_{stL} and R_{stN} are the resistor divider branch, and R_{in} is the voltage sensing resistor that serves as the scaled-down voltage input to the operational amplifier. VDC is the power supply to provide the DC bias voltage for the IMD circuit. S is the solid stage switch, which is generally open to limit the leakage current.

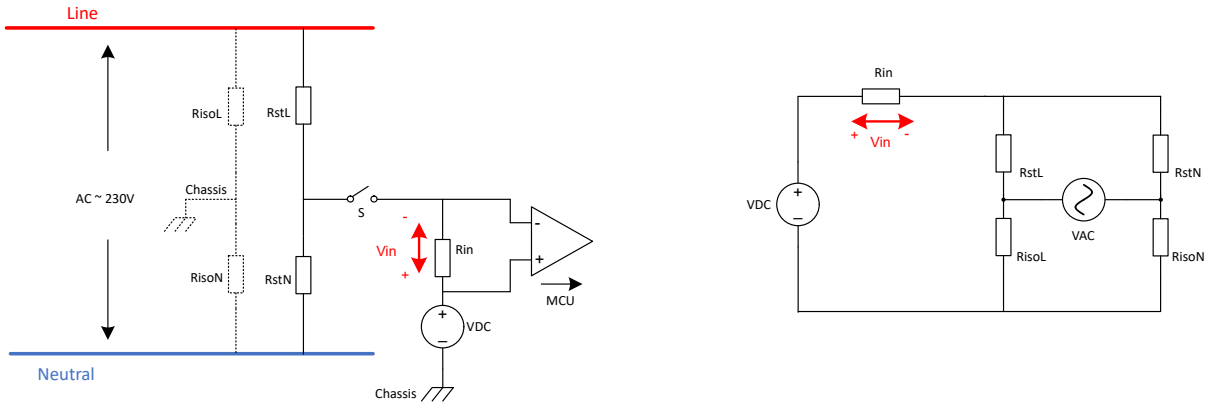

Figure 1-2. Block Diagram and the Equivalent Circuit of the Active Single-Switch Architecture

The basic principle of operation is to create resistor branch when the switch S closes. From the equivalent circuit in Figure 1-2, if the effect of AC voltage is filtered out, the system resistance can be calculated by the sensed voltage $V_{(in(DC))}$.

$$R_{sys} = (R_{stL} \parallel R_{stN}) + (R_{isoL} \parallel R_{isoN}) \quad (1)$$

$$V_{in(DC)} = \frac{R_{in}}{R_{sys} + R_{in}} \times V_{DC} \quad (2)$$

Although this architecture cannot solve R_{isoL} and R_{isoN} directly, the system insulation resistance R_{sys} can reflect the overall insulation status.

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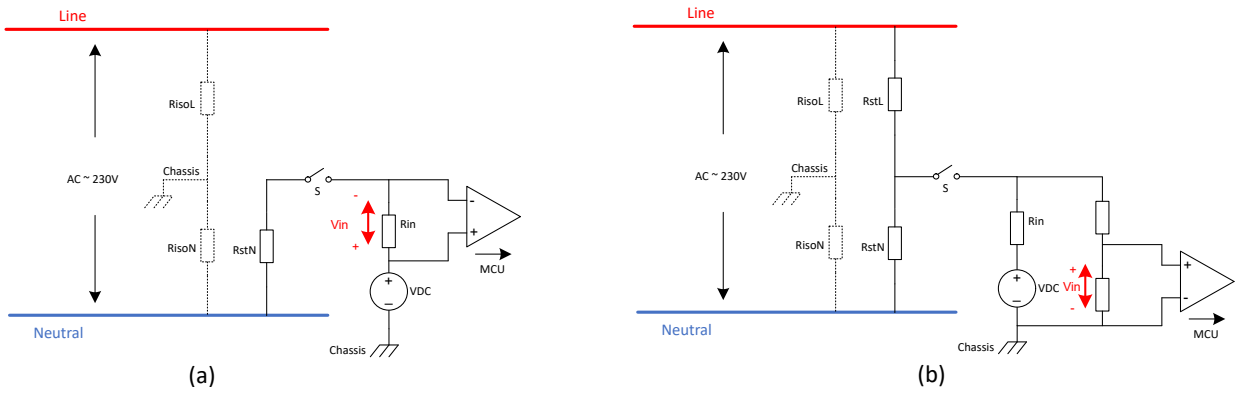
Based on the block diagram in Figure 1-2, there can also be variations in the architecture. Variations are shown in Figure 1-3, image (a). If R_{stL} or R_{stN} is disconnected, variant in image (a) can be considered as a resistor with very high resistance. In this case, the IMD circuit is only connected to the line or neutral, so the power loss on R_{st} is smaller, but the IMD circuit becomes asymmetrical. Since this architecture can only detect the equivalent resistance of the system, if the IMD circuit is asymmetrical, the resistance threshold for an insulation failure of R_{isoL} and R_{isoN} is slightly different.

As shown in Figure 1-3, image (b), the operational amplifier does not need to be connected across R_{in}, because the amplifier can be connected to the scaled-down voltage between the R_{in} and chassis instead. In this variant, the op-amp shares the same ground plane with the chassis, so the variant does not require an isolated op-amp or an op-amp with high common-mode voltage. However, the variant requires an additional resistor series for further voltage scale-down, which introduces extra sensing errors.



A. The R_{stL} series is disconnected
B. The VDC is included in the sensing circuit

Figure 1-3. Block Diagram of Two Architecture Variants

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2 Hardware Design

This section mainly introduces the design steps of hardware circuits and the impact of various parameters on the performance of the system.

2.1 Solid State Relay (SSR)

The first step is to select the appropriate SSR component. The SSR uses a semiconductor FET to build the high-voltage ability switches with isolation barrier. Compared to a traditional relay or photo MOS, the SSR can support single or bidirectional ON and OFF control and a higher switching speed to enable less settling time. Additionally, SSR can support stand-alone switch control without a dedicated driver circuit or dedicated bias power for coil excitation. Table 2-1 summarizes the SSR components.

Table 2-1. SSR Components Summary Table

Part Number	Channels	Standoff Voltage	Load Current	Avalanche Current (60s)	Insulation
TPSI2140-Q1	1	1200V	50mA	1mA	Basic
TPSI2240-Q1	1	1200V	50mA	1mA	Reinforced
TPSI2240T-Q1	1	1200V	50mA	3mA	Reinforced
TPSI2072-Q1	2	600V	50mA	1mA	Basic
TPSI2260-Q1	1	600V	50mA	1mA	Reinforced

For an active single-switch architecture, select single channel SSR components. A higher standoff voltage is beneficial in high potential testing, and the higher avalanche current is very helpful for high potential testing. Therefore, TPSI2240T-Q1 is selected as the SSR component.

2.2 Resistors

The second step is to select the resistors R_{stL}, R_{stN}, and R_{in}, including the maximum resistance value calculation, minimum resistance value calculation, and the resistance ratio calculation. To simplify the circuit design, the assumption of $R_{stL} = R_{stN} = R_{st}$ is used in the following analysis.

2.2.1 Minimum Resistance

To protect the SSR component, the minimum resistance value is dependent on the requirements of high potential (Hi-Pot) testing. Typically, Hi-Pot testing is required between the AC side and the protective earth. Figure 2-1 shows the typical diagram of Hi-Pot testing. R1 is the total resistance value in the Hi-Pot testing circuit.

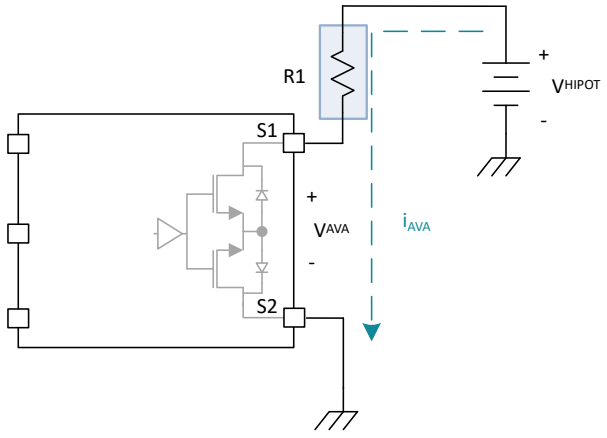

Figure 2-1. Diagram of Hi-Pot Testing

In a typical Hi-Pot testing setup, the AC line and AC neutral are short-circuit, as shown in Figure 1-2; in this architecture, Equation 3 applies.

$$R_1 = 0.5 \times R_{st} + R_{in} \tag{3}$$

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According to GB/T 18487.1 - 2023, when the rated insulation voltage is from 690V to 800V, the Hi-Pot testing voltage is 2830V.

During the 2830V DC Hi-Pot test, which lasts for 60s, the avalanche current is limited to 3mA for the TPSI2240T-Q1 device. The voltage across the SSR is clamped to 1300V (1300V is the specification of the minimum avalanche voltage in the datasheet), so the resistance value required to limit the current is no less than 765kΩ [Equation 3].

$$0.5 \times R_{st} + R_{in} \geq \frac{V_{HiPot} - V_{SSR}}{I_{AVA}} = 765k\Omega \quad (4)$$

2.2.2 Maximum Resistance

The maximum resistance value is dependent on the capacitance value and response time requirements of the AC side of the system. Usually, the IMD circuits are required to respond within a few grid cycles after an insulation failure occurs, such as 100ms.

Based on the block diagram in Figure 1-2, consider the influence of the capacitor on the AC side and the AC grid voltage (see Figure 2-2). VDC and VAC are the DC bias supply voltage and AC grid voltage, respectively. According to the superposition theorem of circuits, VDC and VAC are two independent power sources that can be considered separately, and the effects of the two power sources ultimately superimpose on V_{in}.

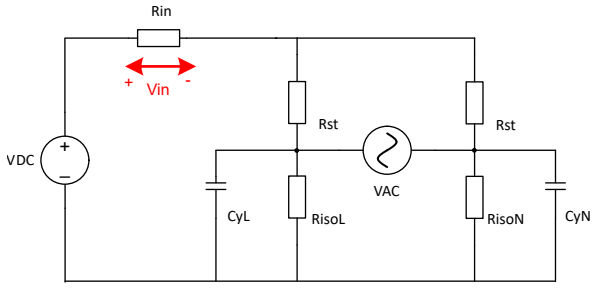

Figure 2-2. Block Diagram With Capacitors and Grid Voltage

$V_{in(AC)}$ is an alternating voltage without any DC offset.

Note

If the AC voltage contains a DC offset, the offset affects the accuracy of the IMD. The answer is to calculate the DC offset when sensing the AC voltage and make a correction in the calculation of the IMD.

During the calculation of the IMD, the influence of $V_{in(AC)}$ can be removed through filtering. After eliminating the influence of the AC voltage, only the effect of VDC is considered. Therefore, the VAC is regarded as short-circuit and the equivalent circuit can be simplified to Figure 2-3.

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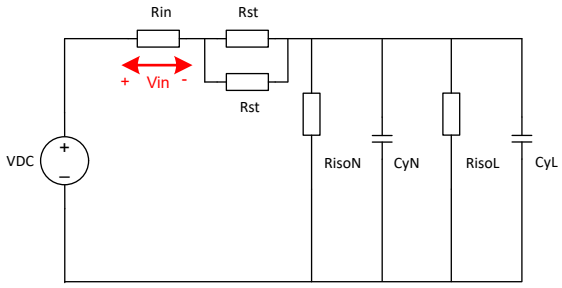

Figure 2-3. Simplified Block Diagram

To eliminate the effects caused by the transient process of charging the Y capacitor, a period of settling time must occur after the resistive branch is switched in, and before the measurement of the insulation voltage is done. The time constant of the resulting RC circuit is:

$$\tau = \left[\left(0.5 \times R_{st} + R_{in}\right) \parallel R_{isoL} \parallel R_{isoN}\right] \times \left(C_{yL} + C_{yN}\right) \quad (5)$$

The settling time between the closing of the switch and the start of the measurement must be at least three times the time constant, because this settling time permits the voltage to settle to 95% of the final value. As an example, if the response time is within 100ms, the time constant must be no more than 33.3ms. In the case of a Y capacitance of 10nF and an insulation resistance of 10MΩ, the switch-in resistance value is no more than 2.46MΩ.

$$0.5 \times R_{st} + R_{in} \leq 2.46M\Omega \quad (6)$$

Generally, a lower resistance value means a shorter response time. Under the premise of passing the Hi-Pot test, the smaller the resistance value, the higher the accuracy of the fixed settling time.

2.2.3 Resistance Ratio

Suppose the total switch-in resistance value is 800kΩ. The resistance ratio between R_{st} and R_{in} is also important; as the ratio affects the weight of VDC and VAC in the IMD circuit and also influences the resolution of the sensed voltage. Define the proportion of R_{in} in total switch-in resistance value as **r**.

$$r = \frac{R_{in}}{R_{st} + R_{in}} \quad (7)$$

The range of **r** is from 0 to 1. To improve the accuracy of the IMD circuit, the best-case situation is that when the insulation failure occurs, the sensed voltage V_{in} deviates as much as possible than when in normal state; meaning, the IMD circuit has a higher resolution on the insulation resistance value. In this document only VDC is used in the insulation resistance calculation, however, the influence of VAC cannot be ignored because $V_{in(AC)}$ affects the scale-down circuit design. To analyze the influence of VAC, the equivalent circuit is shown in Figure 2-4.

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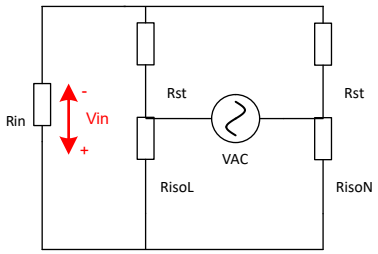

Figure 2-4. The Influence of VAC

R_{st} and R_{in} are the known resistance values, while R_{isoL} and R_{isoN} values are unknown and are changed with insulation status. If R_{isoL} and R_{isoN} are completely symmetrical, V_{in} is not affected by VAC. The worst-case scenario is when R_{isoL} and R_{isoN} have the greatest resistance value difference. That situation is when one resistor is in short circuit and another resistor is in open circuit, at which time $V_{in(AC)}$ reaches maximum AC value.

$$V_{in(AC),\,max} = \frac{R_{in} \parallel R_{st}}{R_{st} + R_{in} \parallel R_{st}} \times V_{AC} = \frac{r}{r+1} \times V_{AC} \tag{8}$$

Regarding $V_{in(DC)}$, the peak voltage value occurs in cases where R_{isoL} and R_{isoN} are short circuit simultaneously.

$$V_{in(DC),\,max} = \frac{R_{in}}{R_{st} \parallel R_{st} + R_{in}} \times V_{DC} = \frac{2r}{r+1} \times V_{DC} \tag{9}$$

Although $V_{in(AC),max}$ and $V_{in(DC),max}$ are not the same scenario, these two worst-case scenarios do not occur simultaneously. To simplify the analysis and leave some margin, the assumption that the voltages occur at the same time for these two worst-case scenarios is used, meaning:

$$V_{in,\,max} = V_{in(DC),\,max} + V_{in(AC),\,max} = \frac{2r}{r+1} \times V_{DC} + \frac{r}{r+1} \times V_{AC} \tag{10}$$

$$V_{in,\,min} = V_{in(DC),\,min} - V_{in(AC),\,max} = -\frac{r}{r+1} \times V_{AC} \tag{11}$$

To cover VIN by the input voltage range of the analog-to-digital converters (ADCs), the range of VIN must be conditioned to 0V to 3.3V.

$$V_{ADC} = \frac{3.3}{V_{in,\,max} - V_{in,\,min}} \times \left(V_{in} - V_{in,\,min}\right) < 3.3V \tag{12}$$

Where V_{in} is the actual voltage between $V_{in,min}$ and $V_{in,max}$.

According to Equation 10, Equation 11, and Equation 12, the range of the resistance ratio can be determined.

$$V_{in,\,max} - V_{in,\,min} = \frac{2r}{r+1} \times (V_{AC} + V_{DC}) < 3.3V \tag{13}$$

Suppose VDC = 40V and VAC = 310V (peak value). The calculated range of **r** is:

$$1/r > 211.1 \tag{14}$$

Under the premise of satisfying the above formula, the value of **r** must be large enough so the difference between $V_{in,max}$ and $V_{in,min}$ is maximized; so the ADC input has the highest resolution. Based on the resistance range analysis and resistance ratio analysis, the resistor value can be selected as Equation 15 and Equation 16:

$$R_{in} = 7.5k\Omega \tag{15}$$

$$R_{st} = 1.6M\Omega \tag{16}$$

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2.3 Bias Supply

From the equivalent circuit in Figure 1-2, the system resistance can be calculated by the sensed voltage $V_{in(DC)}$, as described in Equation 1 and Equation 2. The value of the bias power supply mainly affects the resolution of the ADC reading in insulation monitoring. When no insulation failure occurs, R_{iso_NOR} is at a level above 10MΩ; R_{iso_NOR} is greater than R_{in}. The system-equivalent resistance and the sensed voltage can be expressed as:

$$R_{sys_{NOR}} = 0.5 \times R_{st} + 0.5 \times R_{iso_{NOR}} \quad (17)$$

$$V_{in(DC)_{NOR}} = \frac{R_{in}}{R_{sys_{NOR}} + R_{in}} \times V_{DC} \cong \frac{2 \times R_{in}}{R_{st} + R_{iso_{NOR}}} \times V_{DC} \quad (18)$$

When a single insulation failure occurs at either the line or neutral, and R_{iso} is reduced to the insulation failure threshold of 110kΩ; R_{isoFLT} is less than R_{iso_NOR}. The system-equivalent resistance and the sensed voltage can be expressed as:

$$R_{sys_{FLT}} \cong 0.5 \times R_{st} + R_{iso_{FLT}} \quad (19)$$

$$V_{in(DC)_{FLT}} = \frac{R_{in}}{R_{sys_{FLT}} + R_{in}} \times V_{DC} \cong \frac{R_{in}}{0.5 \times R_{st} + R_{iso_{FLT}}} \times V_{DC} \quad (20)$$

Therefore, under conditions of insulation failure and normal conditions, the difference of the sensed voltage can be expressed as:

$$\Delta V_{in(DC)} = V_{in(DC)_{FLT}} - V_{in(DC)_{NOR}} = R_{in} \times V_{DC} \times \left(\frac{1}{0.5 \times R_{st} + R_{iso_{FLT}}} - \frac{2}{R_{st} + R_{iso_{NOR}}} \right) \quad (21)$$

To achieve the highest resolution in insulation monitoring, the difference in sensed voltage between the fault conditions and normal conditions must be maximized, meaning, $\Delta V_{in(DC)}$ must be maximized.

According to the previous analysis, the smaller the switch in resistance value, the less the switch affects the accuracy of the Y capacitor. According to Equation 13, when V_{AC} is 310V, assuming the total equivalent switch-in resistance is at the minimum value to improve accuracy, the R_{in} and R_{st} values at different values of V_{DC} can be calculated, as summarized in Table 2-2.

Table 2-2. Switch-In Resistance Values in Different DC Bias Voltages

V_{DC}	1 / r	R_{in}	R_{st}	$\Delta V_{in(DC)}$ (Asymmetric insulation failure from R_{iso_NOR} = 10MΩ to R_{iso_FLT} = 110kΩ)
12V	194.2	8.2kΩ	1585kΩ	92mV
24V	201.4	7.9kΩ	1584kΩ	177mV
40V	211.1	7.5kΩ	1580kΩ	282mV
80V	236.0	6.7kΩ	1574kΩ	505mV

For the same VDC, Table 2-2 shows the minimum value of 1 / r, that is the maximum value of R_{in}. If 1 / r continues to decrease, the sensed voltage range exceeds 3.3V.

According to Table 2-2, under different values of V_{DC}, the value of R_{st} is almost the same, while the larger the V_{DC}, the greater the value of $V_{DC} \times R_{in}$. According to Equation 21, the higher the V_{DC}, the higher the $\Delta V_{in(DC)}$, allowing insulation failures to be distinguished more effectively from normal conditions.

Due to the safety requirements of the low-voltage system, the voltage on the low-voltage side cannot be too high, so 40V is ultimately chosen as the DC bias supply voltage. If the low-voltage battery is rated for 48V, this DC bias supply voltage can be derived directly from the low-voltage battery. If the low-voltage battery is rated for 12V, a boost circuit is usually needed to generate 40 volts.

The peak transient current provided by this DC power supply is shown as:

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$$I_{peak} = \frac{V_{DC}}{0.5 \times R_{st} + R_{in}} \quad (22)$$

According to the parameters of a 40V value of V_{DC} in Table 2-2, the calculated I_{peak} is less than 1mA, so the IMD circuit does not have high requirements for the current capacity of the VDC.

The bias power of an OBC and HVLV DC-DC system usually includes a flyback converter. The simplest way to generate the 40V VDC is to leverage the flyback topology by implementing one extra winding, and the LM5155-Q1 device is a common type of flyback controller in OBC bias supply. More details on bias supply architectures can be found in the references section [3] and [4]. Considering the cross-regulation of flyback, the output of the winding needs an LDO or a dump load.

Another implementation method is through the boost converter. The TPS61170-Q1 boost converter offered by TI operates at 1.2MHz, can deliver up to 38V, and maintains good efficiency even at light loads; making the device a potential option for generating a stable VDC for the IMD circuit. More details on this component can be found in the references section [3] and [5].

A charge pump can also be used for generating VDC and can be implemented by the TLC555-Q1 device. Since the square-wave output switches between the supply voltage and GND, with few additional capacitors and diodes, this makes the TLC555-Q1 device appropriate for generating a voltage multiplier. More details on how to boost voltage using the TLC555-Q1 device can be found in the reference section [6].

2.4 Amplifier

The selection of the operational amplifier is related to the position of the MCU and the IMD architecture. This document uses the architecture shown in Figure 1-2 as an example for further analysis.

2.4.1 MCU on the Low Voltage Side

If the MCU for the IMD is placed on the low-voltage battery side, meaning the chassis, then the operational amplifier can be a non-isolated amplifier, with the main requirement being the range of common-mode voltage. As can be seen from Figure 1-2, the non-inverting input of the operational amplifier is VDC, while the inverting input is VDC plus the differential voltage represented by Equation 10 and Equation 11. The INA148-Q1 is a precision, low-power, unity-gain difference amplifier with a 75V common-mode input voltage at a voltage supply of 5V. Since this device has a unity gain, the output of the device can be directly connected to the ADC module of the DSP. The functional block diagram is shown in Figure 2-5. More details on this component can be found in the references section [7].

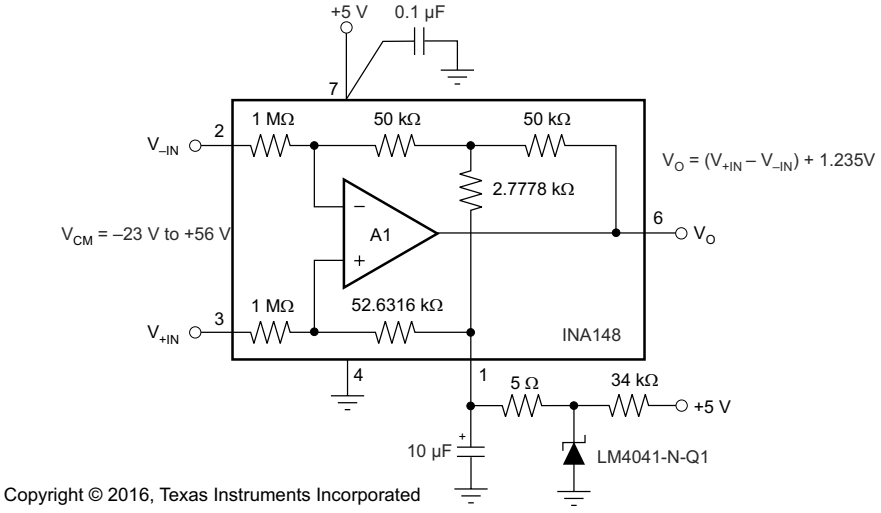

Figure 2-5. Functional Block Diagram of INA148-Q1

According to Equation 10 and Equation 11 and Table 2-2, when the VDC is 40V and the VAC is 310V, the maximum and minimum values of the input voltage are $V_{in,max}$ = 7.8V and $V_{in,max}$ = –1.46V, respectively. Therefore, set the REF pin of the INA148-Q1 device to 1.46V for the INA148-Q1 device to have an output range

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from 0V to 3.3V. As shown in Figure 2-5, PIN 1 of the INA148-Q1 device can be leveraged to generate the 1.46V voltage reference. For high accuracy on the voltage reference, the voltage can be generated by a precision micro-power shunt voltage reference of the LM4041-N-Q1 device. The block diagram is shown in Figure 2-6, V_o is connected to PIN 1 of the INA148-Q1 device as the voltage reference. For a voltage reference of 1.46V, R2 is selected to 10kΩ, and R1 is selected to 1.78kΩ.

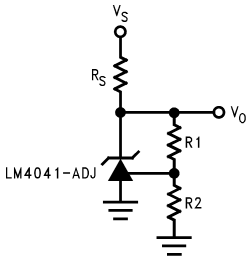

Figure 2-6. Voltage Reference Generation by LM4041-N-Q1

The option of the MCU placed on the LV side is selected for further analysis.

2.4.2 MCU on the AC Side

When the MCU for the IMD is placed on the AC side, isolation is required between the MCU and the IMD circuit. In these cases, TI recommends isolated amplifiers to provide the galvanic isolation. The AMC3330-Q1 is a precision, isolated amplifier with a fully-integrated, isolated DC/DC converter, which allows a single-supply operation from the low-side of the device. The differential output is proportional to the input voltage with a fixed gain of 2V/V. A small difference is that, since the input voltage range is ±1V, the voltage in Equation 12 and Equation 13 must be changed from 3.3V to 2V to calculate R_{in} and R_{st}. The functional block diagram is shown in Figure 2-7. More details on this component can be found in the references section [8]. Because AMC3330-Q1 is in differential output, the device has good anti-interference capability if differential routing is implemented. If differential routing is not implemented, generally, an additional amplifier is used to do the differential to a single-ended conversion, for single-ended ADCs.

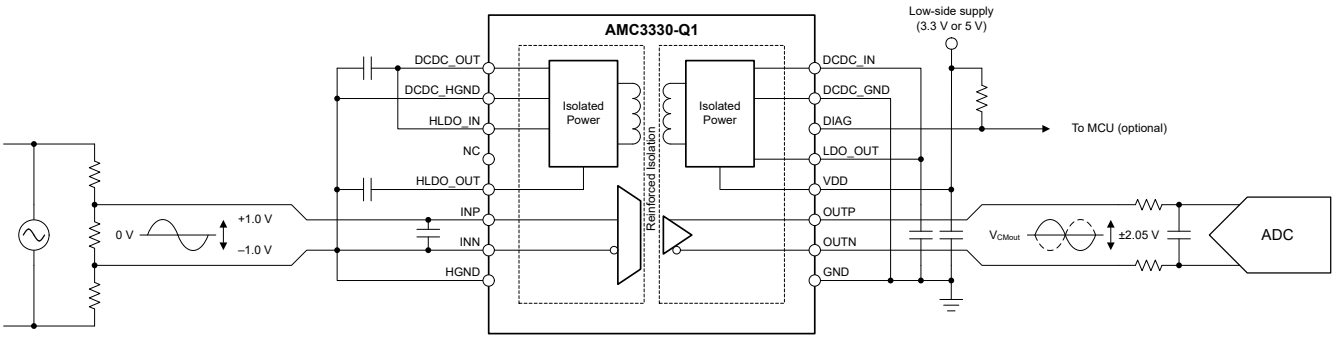

Figure 2-7. Functional Block Diagram of AMC3330-Q1

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3 Software Design

This section mainly introduces the design steps of software control and the impact of various parameters on the performance of the system.

3.1 Settling Time

As shown in Equation 5, the IMD system needs to set a sufficiently long settling time to reduce the impact of the Y capacitor on the accuracy of the IMD. From Equation 5, different insulation resistances correspond to different minimum settling times. When an insulation failure occurs, the settling time requirement is lower than the settling time requirement in a normal state. The settling time worst-case is in a normal state where the insulation resistance is far higher than the switched-in resistance; this case, Equation 5, can be expressed as:

$$\tau = (0.5 \times R_{st} + R_{in}) \times \left(C_{yL} + C_{yN}\right) \tag{23}$$

Suppose VDC is 40V and the Y capacitors are 10nF, and by substituting the resistance value from Table 2-2 into Equation 23, the time constant is 16.15ms, so the minimum settling time is 48.45ms.

The minimum settling time of 48.45ms is the preferred value; because in any scenario, the effect of a 10nF Y-capacitor remains below 5%. However, this scenario results in an excessively long duration of insulation monitoring. In practical applications, calculating the insulation resistance under normal states is not necessary. The insulation resistance only needs to be accurately measured near the insulation failure threshold.

Therefore, assuming that the insulation resistance from 0Ω to 500kΩ is the range of values for which higher measurement accuracy is desired; by substituting R_{isoP} and R_{isoN} with 500kΩ in Equation 5, the required time-constant can be calculated as τ = 6ms, so the minimum settling time is 18ms. Since the moving average block has a window time of 20ms, this means that after the SSR closes, a time duration of at least 20ms occurs to accurately filter out the influence of the AC voltage. Therefore, the settling time is set to 20ms.

3.2 SSR Sequence

Since insulation monitoring is mainly conducted using DC voltage while filtering out the AC grid voltage, the turn-on timing of the SSR is not a critical parameter. The SSR can be turned on to start insulation monitoring at any grid voltage. This is one benefit of this IMD architecture.

Since insulation monitoring requires filtering out the AC grid voltage, the sampling process needs to cover a complete grid voltage cycle, which is 20ms. To prevent false triggering of insulation failure, the SSR can be turned on for multiple grid voltage cycles during insulation monitoring. Considering the response time of insulation monitoring, the turn-on duration of the SSR is designed to be 40ms, which is two grid voltage cycles.

3.3 Voltage Threshold

Based on the parameters in Table 2-2, assuming VDC is 40V, insulation resistance in a normal state is 10MΩ and in an insulation failure state is 110kΩ. Substituting VDC into formula Equation 18 and Equation 20, the input voltage under a normal state and N insulation failure state are:

$$V_{in(DC)_{NOR}} \cong \frac{2 \times R_{in}}{R_{st} + R_{iso_{NOR}}} \times V_{DC} = 0.052V \tag{24}$$

$$V_{in(DC)_{FLT}} \cong \frac{R_{in}}{0.5 \times R_{st} + R_{iso_{FLT}}} \times V_{DC} = 0.33V \tag{25}$$

Considering the effect of the Y capacitor, when the settling time is three times the time constant, there is a 5% error in voltage sensing, so the voltage threshold is set to 0.34V. Since the output of the operational amplifier has a voltage offset of 1.46V, the voltage threshold set in the MCU is meant to be 1.8V.

3.4 Moving Average

As analyzed in Section 3.1, due to the impact of the settling time, some time occurs from the closing of the switch to the start of the IMD calculation. Therefore, the method of filtering out the effect of $V_{in(AC)}$ is through a moving average algorithm, rather than performing the IMD calculation at the zero-crossing point of VAC.

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Within the 40ms closure of the SSR, voltage on R_{in} must be sampled multiple times and averaged to obtain the DC voltage value with the AC grid voltage influence filtered out. According to the Nyquist theorem, the sampling rate must be at least twice the bandwidth. To better restore the voltage signal, the sampling rate is set to 20 times the bandwidth, that is 1000Hz. Within 40ms, the MCU samples a total of 40 points, and the software needs to average the values of these 40 points to obtain the DC voltage value. Using more sampling points for moving average is beneficial for noise immunity.

3.5 Plausibility Check

From Equation 24 and Equation 25, the voltage difference under an insulation failure state and a normal state is about 300mV. If an insulation failure fault is falsely triggered, users can perceive the OBC system as not robust. To prevent insulation failures from falsely triggering, the AC values of the sensed voltage can be leveraged for a plausibility check.

As shown in Figure 2-4, if the system is in a normal state, VAC has no effect on the sensed voltage, that is $V_{in(AC)}$ = 0V. If the system experiences an insulation failure, the worst-case is that the insulation resistance drops to 0Ω, at which case the effect of VAC is as shown in Equation 8. By substituting the parameters from Table 2-2 with VDC is 40V and VAC is 310V, according to Equation 8, the AC voltage influence is $V_{in(AC)}$ = 1.46V.

According to Equation 20, the $V_{in(DC)_{FLT}}$ at this moment can be calculated as $V_{in(DC)_{FLT}}$ = 0.375V. This means that the sensed voltage V_{in} is a DC voltage of 0.375V superimposed with an AC voltage with a peak value of 1.46V, so the voltage range is from –1.085V to 1.835V. Since the output of the operational amplifier has a voltage offset of 1.46V, the actual input voltage to the MCU is from 0.375V to 3.295V.

Therefore, a rule for the plausibility check can be established. When an insulation failure is detected, the maximum input voltage values of 40 sampling points must be checked simultaneously. The voltage threshold of the plausibility check set in the MCU can be set to 2.5V. If any input voltage exceeds 2.5V, this exceedance is considered as an insulation failure has occurred.

The voltage threshold is set to 2.5V, mainly for the following reasons:

- The AC voltage is usually a fluctuating range rather than a stable 310V.
- If the Y capacitor is asymmetric between the line and neutral, the sensed voltage experiences additional AC voltage fluctuations.
- The amplitude of the sensed AC voltage is also affected by the value of the Y capacitor.

However, the plausibility check can only detect asymmetric faults and is not applicable to fully symmetric faults. Therefore, the plausibility check cannot replace average voltage as the main criterion for insulation monitoring. The decision logic is optimized as, when the average voltage drops below the voltage threshold of 1.8V, check whether the peak voltage exceeds 2.5V:

- If peak voltage does exceed 2.5V, immediately determine this event is an asymmetrical fault.
- If peak voltage does not exceed 2.5V, continuously monitor a few more cycles to determine whether this event is a symmetrical fault, depending on the customer's requirements for response time and tolerance for false triggers.

3.6 Control Scheme Summary

Based on the above analysis, the complete insulation monitoring process is shown in Figure 3-1. The x-axis in Figure 3-1 is the time, and the y-axis in Figure 3-1 is the voltage. The green curve VIN represents the ADC input voltage of the MCU, which is the V_{in} voltage plus a 1.46V offset. The orange curve VIN_AVG represents the voltage after applying a moving average from the green curve, which is equivalent to the green curve minus $V_{in(AC)}$, leaving the $V_{in(DC)}$ and the 1.46V offset. The yellow scattered points represent the ADC sampling time, with a total of 40 sampling points over two AC grid cycles.

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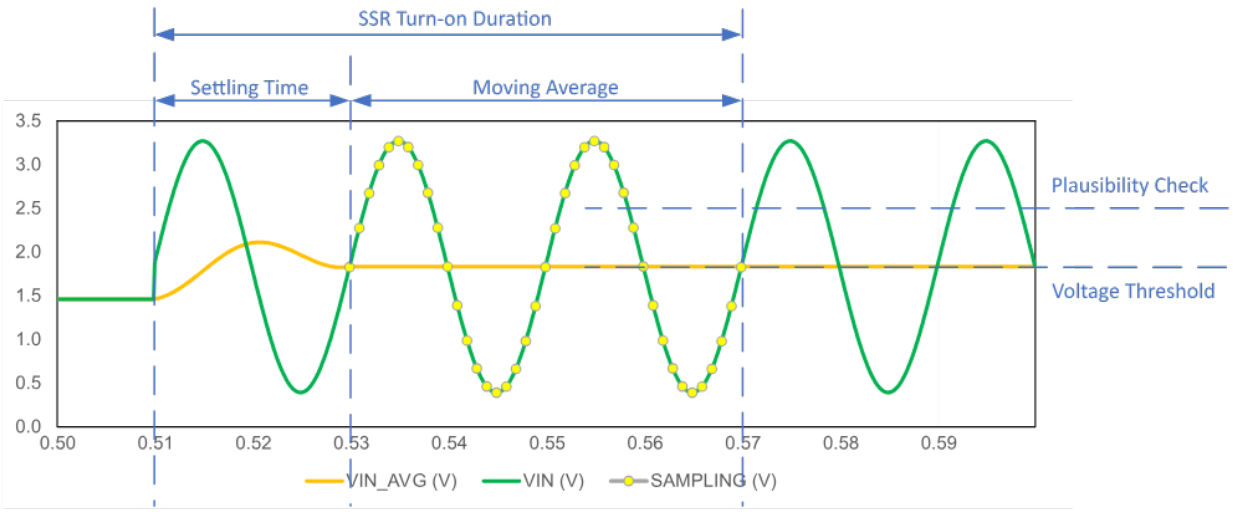

Figure 3-1. Control Scheme Summary

Before t = 0.51s, the SSR was in a disconnected state, so no current flows through R_{in}, and therefore, the voltages of VIN and VIN_AVG are the same, both being a 1.46V voltage bias.

At t = 0.51s, the SSR is turned on, and the IMD circuit enters a transient process in the next 20ms. VIN_AVG follows VIN, but the value is not accurate at this point. Since 20ms is longer than the 18ms settling time, after 20ms, VIN_AVG is already the accurate average voltage of VIN.

At t = 0.53s, the calculation of insulation resistance officially begins. The MCU samples one point every 1ms, so there are a total of 40 sampling points in the next 40ms. From the orange curve, VIN_AVG is 1.78V at this moment, which is below the voltage threshold of 1.8V, and therefore, triggers the plausibility check. From the yellow scatter points, within 40ms, 14 out of 40 points exceeded the plausibility check threshold of 2.5V, and therefore, the system is immediately identified as an asymmetric insulation failure.

At t = 0.57s, SSR is disconnected, one insulation monitoring cycle has ended. However, if the peak voltage does not exceed 2.5V during the period from 0.53s to 0.57s, this indicates that the system potentially experienced a symmetrical insulation failure. If this is the case, at 0.57s, the SSR continues to conduct for some grid cycles, for example, for 40ms. During this time, the VIN_AVG voltage continues to be monitored until VIN_AVG is considered accurate enough. The time frame depends on the customer's requirements for response time and tolerance for false triggers.

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4 Simulation Results

This section mainly verifies the effectiveness of the proposed hardware design and software control scheme. The simulation is built based on PLECS, and the simulation parameters are shown in Table 4-1.

Table 4-1. Simulation Parameters

Parameter	Value
AC Voltage Magnitude	310V
AC Voltage Frequency	50Hz
DC Voltage	40V
Resistor Divider Branch (R_{st})	1.6MΩ
Voltage Sense Resistor (R_{in})	7.5kΩ
Insulation Resistance (R_{iso_NOR})	10MΩ
Insulation Resistance (R_{iso_FLT})	110kΩ

4.1 Settling Time

According to the analysis in Section 3.1, the required settling time is the longest under a normal state, and the settling time required becomes shorter when an insulation fault occurs. To eliminate the effect of AC voltage on the moving average, the settling times under a normal state and symmetric insulation failure state are compared.

Figure 4-1 is the settling time in a normal state. Before t = 0.51s, the VIN_AVG voltage was 1.46V. After t = 0.65s, the VIN_AVG voltage is stabilized in 1.512V. After t = 0.60s, which is around five times the time constant, the sensed voltage VIN reaches the steady-state value.

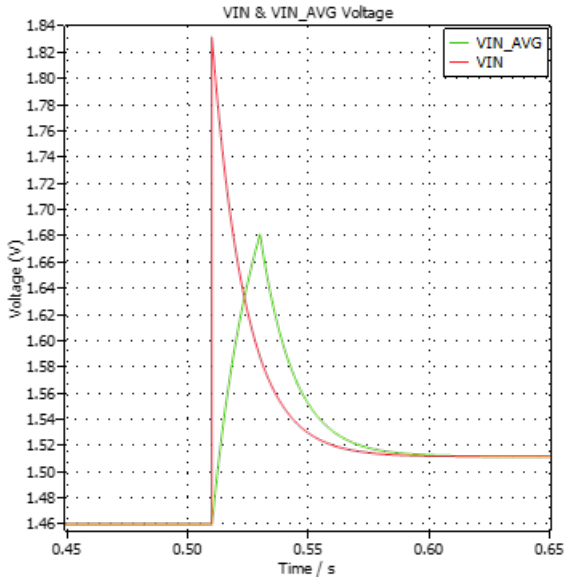

Figure 4-1. Simulation Results on Settling Time (Normal State)

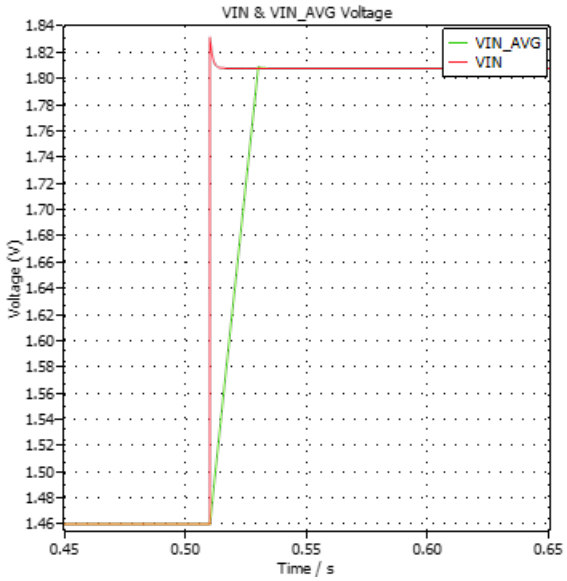

Figure 4-2. Simulation Results on Settling Time (Symmetric Insulation Failure State)

Figure 4-2 is the settling time in a symmetric insulation failure state. According to Equation 5, the time constant in this case is 1ms. Before t = 0.51s, the AVG voltage is 1.46V. After t = 0.65s, the AVG voltage is stabilized in 1.808V. After t = 0.515s, which is around five times the time constant, the sensed voltage VIN reaches the steady-state value.

By comparing Figure 4-1 and Figure 4-2, some conclusions can be drawn:

- First, the higher the insulation resistance value, the higher the requirement for the settling time. In theory, the normal state is meant to be treated as the worst. To improve the response time, asymmetric faults must also be treated as the objects of analysis.

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- Second, five times the time constant is the preferred settling time. To improve the response time, three times the time constant can be used in practical applications.
- Finally, when the settling time is greater than the moving average time window of 20ms (for example, 90ms in Figure 4-1), set the settling time to the actual value. When the settling time is less than the moving average window time of 20ms (for example, 5ms in Figure 4-2), set the settling time to 20ms.

4.2 Input Voltage Range

According to the analysis in Section 2.2 and Section 2.3, the selection of the resistor and DC voltage values must maintain an input voltage range between 0V and 3.3V for the ADC. When the insulation resistance of the line and neutral to PE is at the worst symmetry, the range of input voltage is the largest. Therefore, the worst-case occurs when one insulation resistor is open and the other insulation resistor is shorted, with the waveform shown in Figure 4-3 and Figure 4-4.

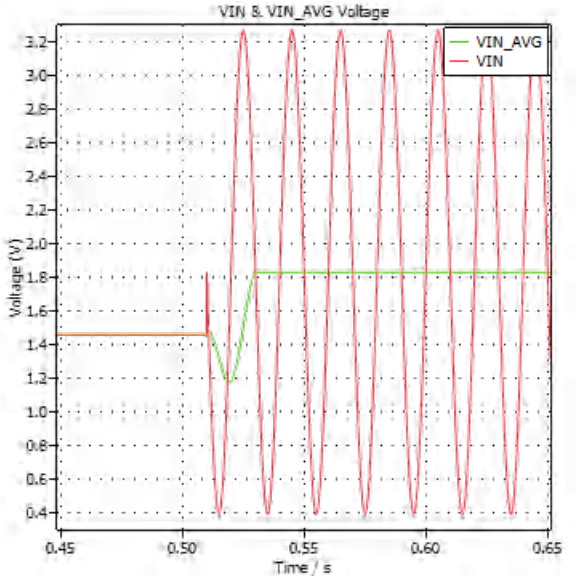

Figure 4-3. Simulation Results on Input Voltage Range (Insulation Failure on Line)

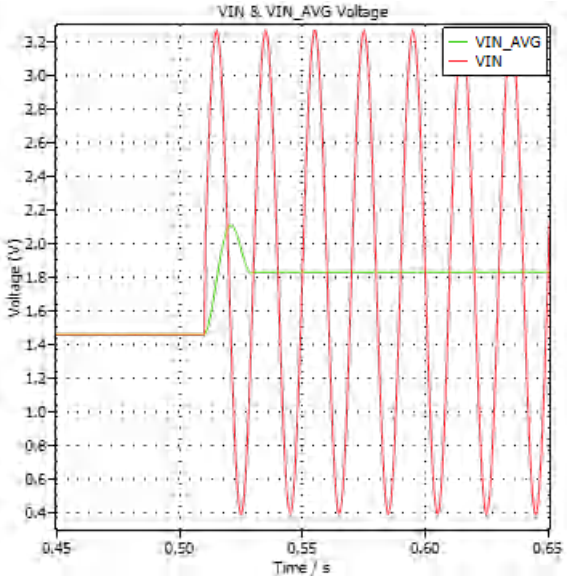

Figure 4-4. Simulation Results on Input Voltage Range (Insulation Failure on Neutral)

From Figure 4-3 and Figure 4-4, the steady-state voltage of VIN_AVG is 1.83V. In either an insulation failure on the line or an insulation failure on neutral, the minimum voltage of VIN is 0.39V, and the maximum voltage of VIN is 3.27V, so the input voltage is within the ADC voltage range. The minimum voltage still has a certain margin from 0V because Equation 10 and Equation 11 assume that $V_{in(DC),max}$ and $V_{in(AC),max}$ occur simultaneously, whereas in practical applications, these two values do not occur under the same scenario.

4.3 Plausibility Check

According to the analysis in Section 3.5, the plausibility check can be used to determine the asymmetric insulation failure. From Figure 4-1, during symmetrical insulation failure, plausibility checks are not applicable, because the maximum value of the VIN does not exceed 2.5V. From Figure 4-3, in the event of an asymmetric fault and the insulation resistance drops to 110kΩ, the plausibility check is applicable because the maximum voltage exceeds 2.5V. Table 4-2 shows the VIN peak voltage and VIN_AVG when the asymmetric insulation resistance falls into different values.

Table 4-2. Plausibility Check in Different Insulation Resistance

R_{isoL}	R_{isoN}	VIN Peak	VIN_AVG	Plausibility Check Applicable	Insulation Failure
10MΩ	10MΩ	1.51V	1.51V	No	No
10MΩ	1MΩ	1.83V	1.63V	No	No
10MΩ	500kΩ	2.08V	1.69V	No	No
10MΩ	200kΩ	2.54V	1.76V	Yes	No
10MΩ	90kΩ	2.93V	1.80V	Yes	Yes

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Table 4-2. Plausibility Check in Different Insulation Resistance (continued)

R_{isoL}	R_{isoN}	VIN Peak	VIN_AVG	Plausibility Check Applicable	Insulation Failure
10MΩ	0kΩ	3.27V	1.83V	Yes	Yes

From Table 4-2, as the insulation resistance decreases, the peak value of VIN increases. When the insulation resistance drops below approximately 200kΩ, the peak value of VIN exceeds the 2.5V threshold, activating the plausibility check. This means that when the insulation resistance is below 200kΩ, the plausibility check helps to detect asymmetrical insulation failures.

4.4 Accuracy

The accuracy of the IMD is related to many factors, such as the precision of resistors, the value of Y capacitors, the deviation of the DC bias supply, the error on the amplifier, and the settling time. The most reliable way to assess the accuracy of the IMD is through hardware testing. The simulation is only used to verify whether insulation failures can be detected under several typical operating conditions.

For the case of an asymmetric insulation failure, as can be seen from Table 4-2, when the insulation resistance drops below 90kΩ, VIN_AVG exceeds the 1.8V threshold, and the insulation failure is detected. When the insulation resistance is greater than 200kΩ, even if VIN_AVG exceeds 1.8V due to various errors, the peak value of VIN is still below the 2.5V threshold, which means a plausibility check prevents false reporting of an insulation failure.

For the case of a symmetric insulation failure, the VIN peak voltage and VIN_AVG can be found in Table 4-3. When the insulation resistance drops below 90kΩ, VIN_AVG exceeds the 1.8V threshold, and the insulation failure is detected. When the insulation resistance is greater than 500kΩ, the VIN_AVG is 60mV lower than the 1.8V threshold, so an insulation failure is not falsely triggered.

Table 4-3. Sensed Voltage in Different Insulation Resistance

R_{isoL}	R_{isoN}	VIN Peak	VIN_AVG	Plausibility Check Applicable	Insulation Failure
10MΩ	10MΩ	1.51V	1.51V	No	No
1MΩ	1MΩ	1.69V	1.69V	No	No
500kΩ	500kΩ	1.74V	1.74V	No	No
200kΩ	200kΩ	1.79V	1.79V	No	No
90kΩ	90kΩ	1.81V	1.81V	No	Yes
0kΩ	0kΩ	1.83V	1.83V	No	Yes

The trickiest situation occurs when a symmetric insulation failure happens, and the insulation resistances are both around 200kΩ. This is because 1.79V VIN_AVG is very close to the 1.8V threshold, so making an insulation failure falsely trigger can easily occur.

A false trigger at 200kΩ is not so bad, since the insulation resistance is expected to be megaohms and the threshold is 110kΩ, so if the insulation is 200kΩ there is already something wrong in the system. As mentioned in Section 3.5, for this kind of scenario, the proposal is to sample a longer time and take the average to minimize the impact of dynamic errors on sampling accuracy.

4.5 Influence of the Y Capacitor

According to the analysis in Section 1.1, the effect of the Y capacitor is mainly reflected in the settling time. Figure 4-1 shows the voltage waveform of a 10nF capacitor under a normal state and Figure 4-3 shows the voltage waveform of 10nF Y capacitors under an asymmetric insulation failure state. For comparison, Figure 4-5 and Figure 4-6 show the voltage waveforms of a normal state and an asymmetric insulation failure state with 20nF Y capacitors.

From Figure 4-5, after t = 0.68s, the VIN_AVG voltage is stabilized in 1.512V. Compared to Figure 4-1, the steady-state voltage of VIN_AVG is the same, but the time to reach the steady state has doubled.

From Figure 4-5, after t = 0.53s, the VIN_AVG voltage stabilized in 1.83V. The minimum voltage of VIN is 0.39V, and the maximum voltage of VIN is 3.27V. Compared to Figure 4-3, the steady-state voltage of VIN_AVG is the same, the minimum and maximum VIN is the same, and the time to reach the steady state is also the same.

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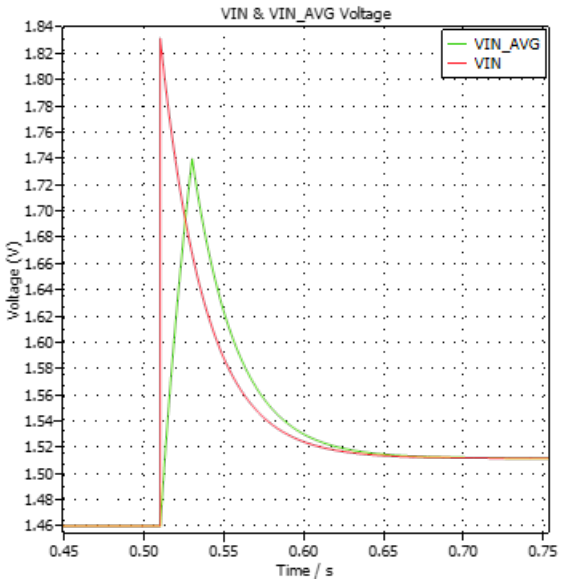

Figure 4-5. Simulation Results With 20nF Y Capacitors (Normal State)

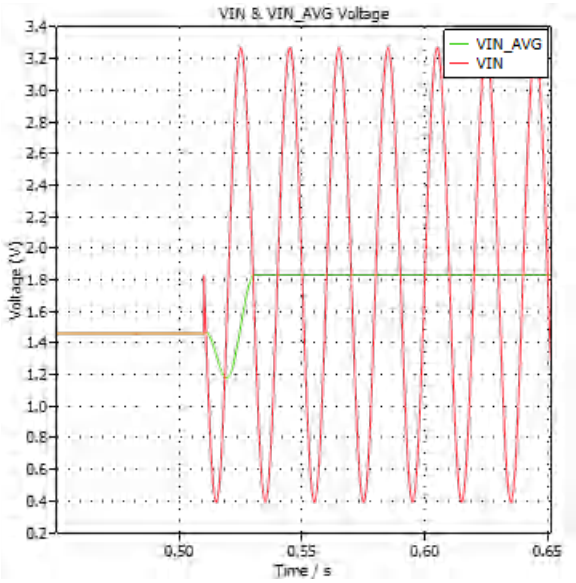

Figure 4-6. Simulation Results With 20nF Y Capacitors (Insulation Failure on Line)

Figure 4-3 and Figure 4-5 are the worst cases where one insulation resistor is open, and the other insulation resistor is shorted. To more realistically reflect the impact of the RC time constant, Figure 4-7 and Figure 4-8 show the situation when one insulation resistance is 10MΩ and the other is 110kΩ. Figure 4-7 and Figure 4-8 show the voltage waveforms when the Y capacitance is 10nF and 20nF, respectively.

Figure 4-7, after t = 0.537s, the VIN_AVG voltage stabilized in 1.78V. The minimum voltage of VIN is 0.72V, and the maximum voltage of VIN is 2.85V. From Figure 4-8, after t = 0.554s, the VIN_AVG voltage stabilized in 1.78V. The minimum voltage of VIN is 0.99V, and the maximum voltage of VIN is 2.58V. Compare Figure 4-7 and Figure 4-8; the steady-state voltage of VIN_AVG is the same, while at 20nF Y capacitors the peak-to-peak value of VIN is smaller, and the time to reach the steady state is longer.

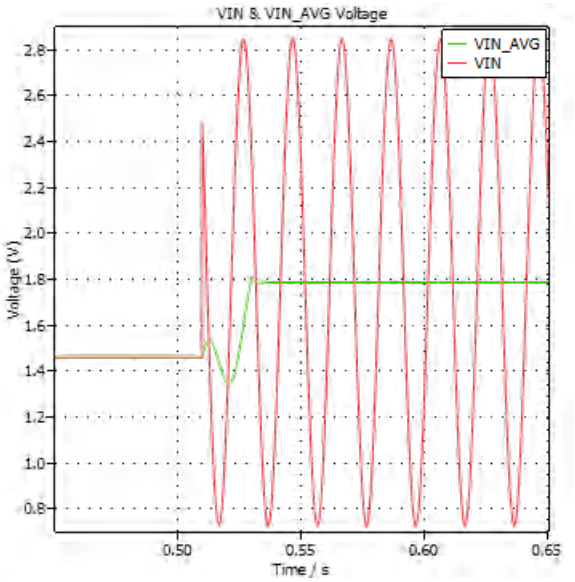

Figure 4-7. Simulation Results With 110kΩ Insulation Failure (10nFY Capacitors)

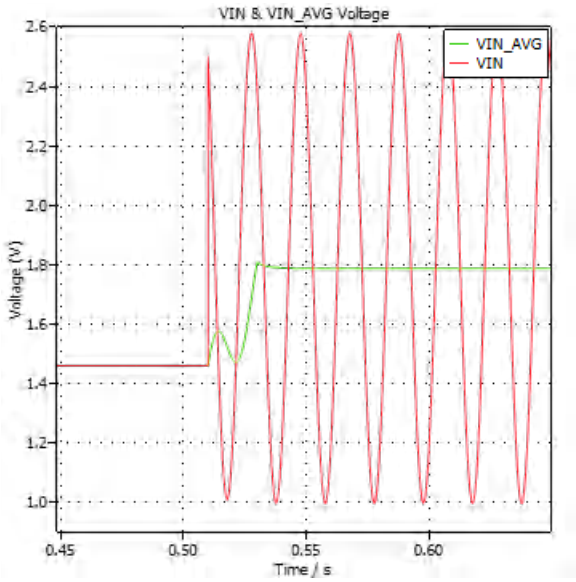

Figure 4-8. Simulation Results With 110kΩ Insulation Failure (20nFY Capacitors)

From above waveforms, several conclusions can be drawn:

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- First, whether in a normal state or in an insulation failure state, the Y capacitor does not affect the steady-state VIN_AVG, which means that the steady-state voltage threshold for detecting an insulation failure is independent of the value of the Y capacitor. Therefore, the phase-delay on $V_{in(AC)}$ caused by Y capacitors does not impact the accuracy of the IMD, and the Y capacitor only impacts the time constant, which can be resolved by setting a sufficient settling time. This is an advantage of this IMD architecture, as the accuracy based on VIN_AVG is not affected by the Y capacitance.
- Second, the value of the Y capacitor affects the time constant of the system, thereby influencing the settling time. In the normal state, the time constant is the largest and exceeds 20ms. Therefore, after doubling the Y capacitor, the settling time also doubles. When the insulation failure resistance is 0kΩ, the time constant is at the minimum and is much less than 20ms. Even if the Y capacitor doubles, causing the time constant to double, the settling time is still less than 20ms, so the Y capacitor has no effect on the settling time of the system. When the insulation failure resistance is 110kΩ, the doubled Y capacitor increases the settling time slightly, but less than in a normal state.
- Finally, the peak-to-peak voltage of VIN is influenced by Y capacitance, which influences the voltage threshold for a plausibility check. From Figure 2-4, when the insulation resistance drops to 0Ω during an asymmetric insulation failure, the peak-to-peak voltage of VIN is not affected by the Y capacitance, because the Y capacitor can be considered directly parallel to VAC. However, when the insulation resistance does not drop to 0Ω, increasing the Y-capacitor causes the peak-to-peak voltage of VIN to decrease. This means that when the Y capacitor is larger, the voltage threshold for the plausibility check needs to be lowered slightly.

If the system Y capacitance reaches several hundred nano-farads or even microfarads, the IMD settling time is very long, and the voltage threshold for the plausibility check is very low. For this kind of application scenario, refer to the reference design in the references section [9]. This reference design measures capacitance for high-voltage DC systems with a large Y capacitance.

5 Summary

This design guide introduces common IMD architectures in bidirectional OBCs. The active single-switch architecture proposed in this paper has advantages, such as the ability to detect symmetrical insulation failures, operation independent of AC voltage, potentially lower isolation costs, and the steady-state voltage threshold independent to the Y capacitor; offering significant benefits in OBC applications. This paper elaborates on the hardware design of this solution, including SSRs, resistors, operational amplifiers, and DC power supplies. This paper also introduces the software design of this solution, including control sequencing, voltage thresholds, data processing and how to configure the settling time to reduce the impact of the Y capacitor on the transient state. Finally, the effectiveness of this solution is verified through simulation. The target of these analyses is to provide step-by-step design guidance of an IMD design.

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