Application Note

Using the TAC5x1x-Q1 Audio Codec in Automotive Infotainment Systems

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ABSTRACT

With the rapid development of in-vehicle infotainment systems, the demand for high-performance audio codecs in automotive applications is increasing significantly. TI's TAC5X1X-Q1 audio codec delivers high audio quality, reliability and rich features for modern vehicle audio needs. This application report focuses on the headset-related applications using the TAC5X1X-Q1 series, covering key aspects such as schematic design (including analog input/output hardware design, AC-/DC-coupling considerations) and headset detection implementation. It details the hardware and software methods for headset insertion detection, addresses critical issues like debounce processing and real-time performance optimization, and briefly introduces other advanced features of the TAC5X1X-Q1 family. The content provided example configurations for engineers involved in the design and development of automotive audio systems using the TAC5X1X-Q1 series codecs.

Note: There is no automotive TAC5212-Q1. Any references to TAC5212 in this app note refer only to the industrial version of TAC5212.

The schematic design parts described in this application note are applicable to the codec families:

- TAC5112-Q1, TAC5111-Q1, TAC5212
- TAC5412-Q1, TAC5312-Q1, TAC5411-Q1, TAC5311-Q1

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1 Introduction

In recent years, the automotive industry has witnessed a profound transformation driven by the advancement of intelligent connectivity and in-vehicle infotainment technologies. Modern vehicles are no longer just means of transportation but have evolved into mobile smart spaces, where passengers demand high-quality audio for entertainment, communication, and navigation. This shift has led to a surge in the demand for automotive-grade audio codecs, which serve as the core components responsible for audio signal encoding, decoding, and processing in in-vehicle audio systems.

The TAC5X1X-Q1 family of high-performance automotive audio codecs offer a wide range of features, including multiple analog input/output channels, high SNR, low THD+N, and support for various audio formats. This makes them ideal for use in car radios, infotainment head units, rear-seat entertainment systems, and other automotive audio applications.

Headset functionality is a key feature in many automotive audio systems, enabling private audio listening for passengers without disturbing others. As such, reliable headset insertion detection is crucial for ensuring a seamless user experience. This application note provides a comprehensive guide on the design and implementation of automotive audio systems using TAC5X1X-Q1 with a focus on headset applications. It covers schematic design considerations for analog interfaces, detailed implementation methods for headset insertion detection, and optimization techniques for detection performance.

Figure 1-1. Automotive 3.5mm Headphone Jack

2 Detailed Description

2.1 Analog Input Hardware Design

TAC5X1X-Q1 is a codec with single/dual-channel analog-to-digital converters whose input pins (IN1P/IN1M and IN2P/IN2M) are configurable as differential or single-ended inputs with AC- or DC-coupling. See Figure 2-1 to Figure 2-4 for the various typical input configurations.

2.1.1 Selection of External Bias Resistor

For the selection of external components, it is recommended to choose the value of external bias resistor R1 according to the microphone impedance. For single-ended input, it is recommended that the external bias resistor matches the microphone impedance. If it is a standard headset interface, the MIC impedance is typically 2.2kΩ, so R1 should be selected as 2.2kΩ. For differential input, it is recommended that the external bias resistor value be half of the microphone impedance. If it is a headset MIC, R1 can be selected as 1.1kΩ.

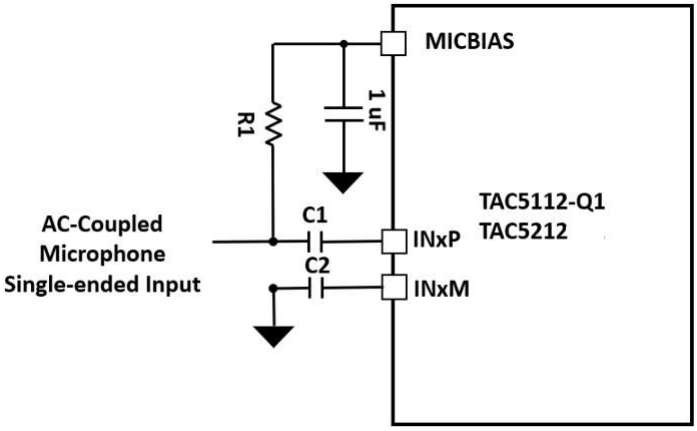

Figure 2-1. AC-Coupled Single-Ended Mic Input Hardware Design: TAC5212 & TAC5112-Q1

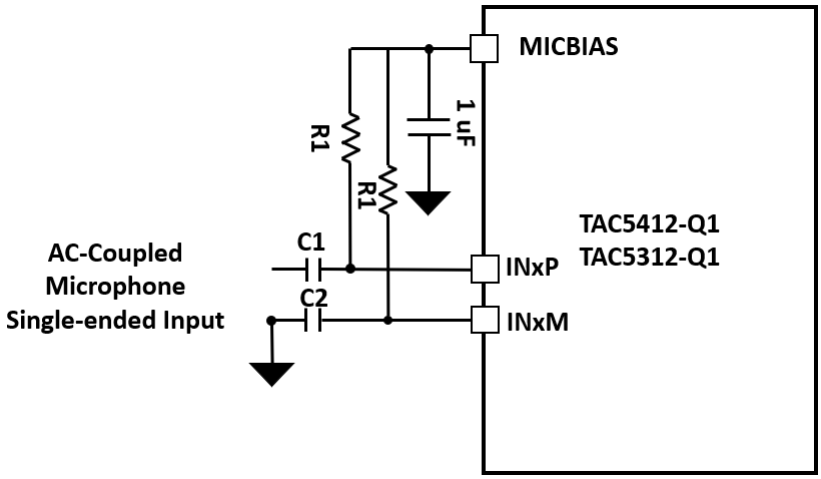

Figure 2-2. AC-Coupled Single-Ended Mic Input Hardware Design: TAC5412-Q1 & TAC5312-Q1

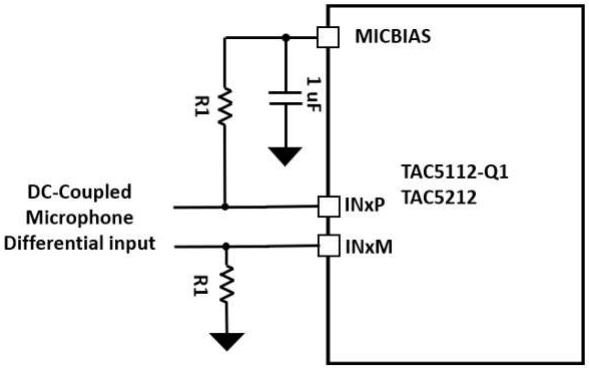

Figure 2-3. DC-Coupled Differential Mic Input Hardware Design: TAC5212 & TAC5112-Q1

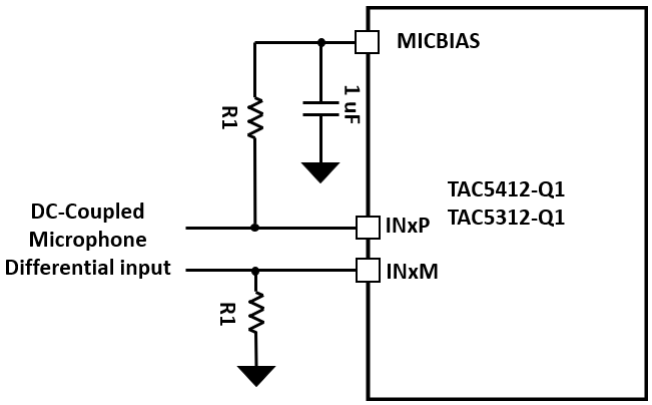

Figure 2-4. DC-Coupled Differential Mic Input Hardware Design: TAC5412-Q1 & TAC5312-Q1

TAC5212 & TAC5112-Q1 bias the ADC through an internal pull-up circuit, which means its MICBIAS pin is only used to power the microphone. The TAC5(3/4)12-Q1 operates differently: the device requires the voltage common-mode to be set externally. This can be done with the integrated MICBIAS or driven by the signal source. In the AC-coupled input configuration, reference Figure 2-1 and Figure 2-2, the MICBIAS pin of the TAC5(3/4)12-Q1 must be connected to the side of the AC-coupling capacitor close to the chip to achieve ADC biasing; in this case, the microphone must be powered by another power supply. Therefore, in terms of input mode compatibility, DC-coupling is the optimal choice for the TAC5(3/4)12-Q1 — in this mode, the MICBIAS can both power the microphone and provide proper biasing for the ADC input. The main advantage for DC-coupling the input signal is to use the input fault diagnostics, with more information found in TAx5xxx-Q1 Fault Diagnostic Features.

Since the performance of the devices changes with the input configuration, it is recommended to use the lowest common-mode setting possible that still satisfies the tolerance required by the system. For best performance in TAC5212 & TAC5112-Q1, AC-coupling is recommended.

2.1.2 Selection of Coupling Capacitor

In AC-coupled mode, the value of the coupling capacitor must be so chosen that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. At power-up, before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage.

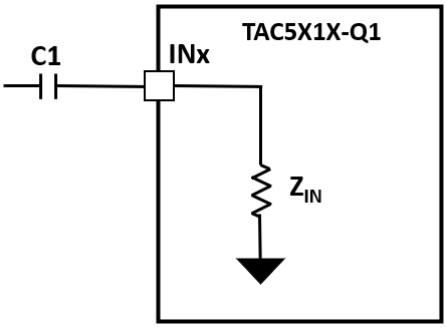

Figure 2-5. AC Equivalent Circuit of Input Pin

Figure 2-5 describes the equivalent circuit for the input pin. The coupling capacitor C and Z_{IN} form a high pass filter. This filter blocks DC and very low frequencies from reaching the input pin. For audio frequencies the capacitor acts as a short circuit. The cutoff frequency is calculated as follows:

$$F_c = \frac{1}{2 \times 3.14 \times C1 \times Z_{IN}} \quad (1)$$

To pass audio frequencies audible to humans, choose F_{min} = 20Hz, Z_{IN} is the input impedance on the INxP/INxM pins. For TAC5212 & TAC5112-Q1, this is typically 5kΩ and can be changed to 10kΩ/40kΩ by register settings.

$$C > \frac{1}{2 \times 3.14 \times F_{min} \times Z_{IN}} = 1.6\mu F \quad (2)$$

Having a smaller capacitor is possible if the input impedance or F_{min} is set higher.

On power-up, the coupling capacitor is charged to the common-mode voltage. This charge is done by connecting an internal 800Ω resistor from pin to AVDD/2. Figure 2-6 describes the equivalent circuit for the input pin quick charge feature. This connection is done for a duration of 2.5ms, enough to charge a 1µF capacitor to AVDD/2. The audio output from the ADC is valid only after the coupling capacitors are charged to the steady state value.

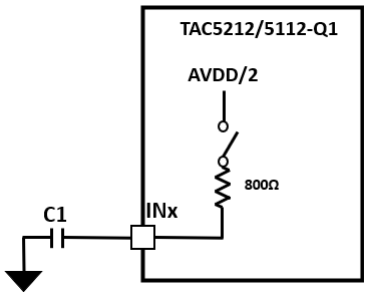

Figure 2-6. Quick Charge Circuit

The formula for calculating the charging time of the AC-coupling capacitor is as follows:

$$T = R \times C \times \ln\left(\frac{1}{1 - \frac{V_{percentage}}{100}}\right) \quad (3)$$

Here, $V_{percentage}$ is the desired voltage percentage, R=800Ω, and C is the coupling capacitor value you choose.

If you want to calculate the time needed to charge to 95% (time constant is 3), here is an example:

$$T = R \times C \times 3 = 800 \times 1\mu f \times 3 = 2.4ms \quad (4)$$

$$T = R \times C \times 3 = 800 \times 4.7\mu f \times 3 = 11.3ms \quad (5)$$

For a 1µF capacitor, you can choose a charging time of 2.5ms. For a 4.7µF capacitor, charge time can be increased to the 12.5ms setting by MISC_CFG1 Register (P0 R5).

7.1.1.6 MISC_CFG1 Register (Address = 0x5) [Reset = 0x15]

MISC_CFG1 is shown in Table 7-8.

Return to the Summary Table.

This register configures the miscellaneous configuration register 1.

Table 7-8. MISC_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	INCAP_QCHG[1:0]	R/W	00b	The duration of the quick-charge for the external AC-coupling capacitor is set using an internal series impedance of 800Ω. 0d = INxP, INxM quick-charge duration of 2.5ms (typical) 1d = INxP, INxM quick-charge duration of 12.5ms (typical) 2d = INxP, INxM quick-charge duration of 25ms (typical) 3d = INxP, INxM quick-charge duration of 50ms (typical)
5-4	SHDN_CFG[1:0]	R/W	01b	Shutdown configuration. 0d = DREG is powered down immediately after IOVDD is deasserted 1d = DREG remains active to enable a clean shut down until a time-out (DREG_KA_TIME) is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved; Don't use
3-2	DREG_KA_TIME[1:0]	R/W	01b	These bits set how long DREG remains active after IOVDD is deasserted. 0d = DREG remains active for 30ms (typical) 1d = DREG remains active for 25ms (typical) 2d = DREG remains active for 10ms (typical) 3d = DREG remains active for 5ms (typical)

Figure 2-7. MISC_CFG1 Register Description

2.2 Analog Output Hardware Design

The TAC5X12-Q1 family consists of two pairs of analog output pins (OUTxP and OUTxM). For headset applications, these pins can be configured as differential or single-ended outputs for playback channels. See Figure 2-8 to Figure 2-11 for the various typical output configurations. The TAC5X12-Q1 family automatically measures the load, whether 16Ω, 32Ω, 10kΩ, etc. and adjusts the output swing.

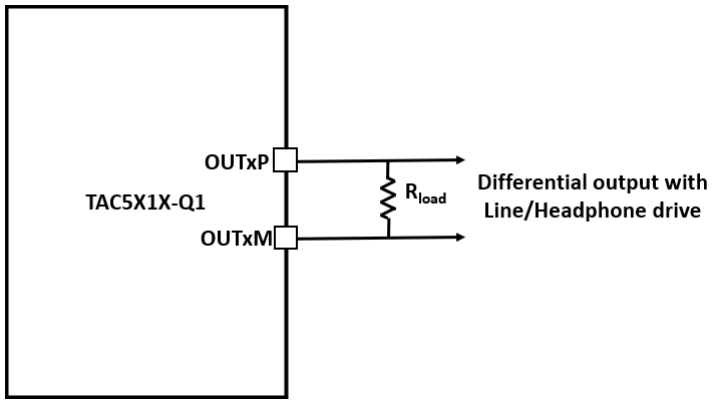

Figure 2-8. Differential DC-Coupled Output

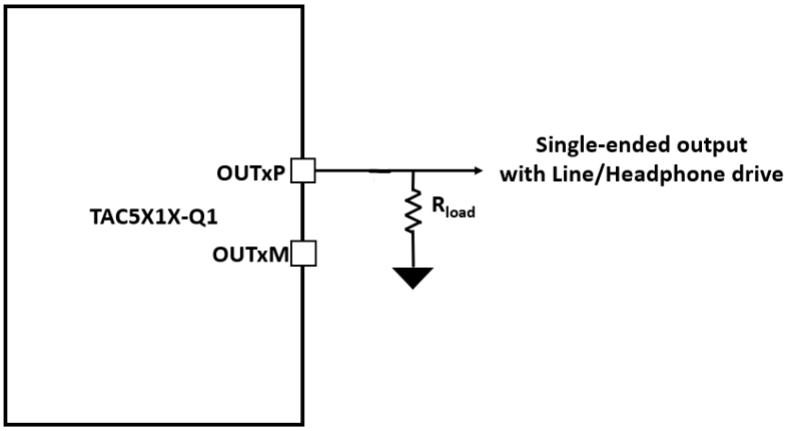

Figure 2-9. Mono Single-ended DC-Coupled Output

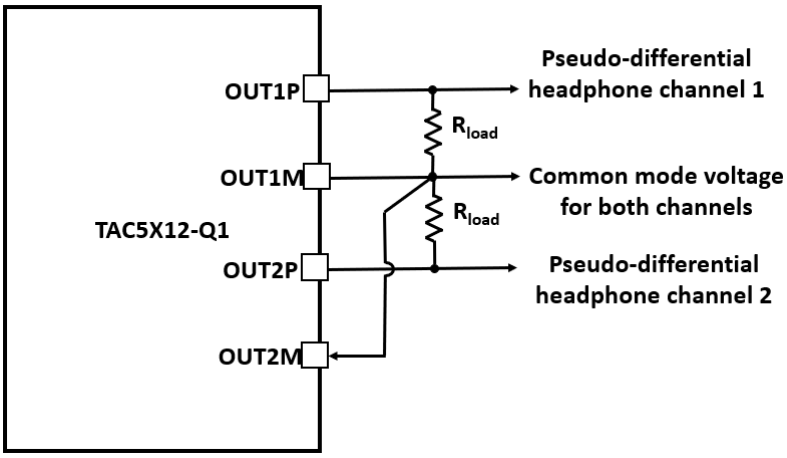

Figure 2-10. Pseudo-Differential Output

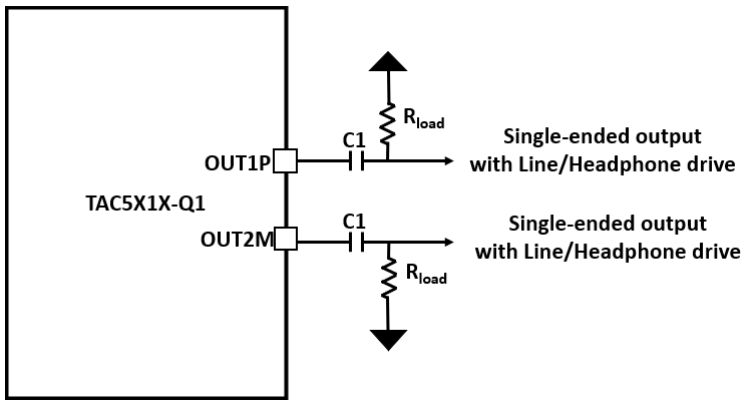

Figure 2-11. Single-ended AC-Coupled Output

Most consumer-grade headphones are single-ended designs (3.5mm/6.35mm interface, requiring only one signal path + ground wire). If using a codec to drive headphones, single-ended mode should be selected. For headset/headphone applications, single-ended AC-coupling is recommended.

For DC-coupled applications, pseudo-differential mode is recommended, because the single-ended mode will contain a DC common-mode voltage. This results in high power consumption, and hence DC-coupled single-ended mode is not recommended.

2.2.1 Selection of Output Coupling Capacitor

The AC-coupling capacitor forms a high-pass filter with the load. If a smaller value capacitor is selected, lower audio frequencies will be attenuated. Hence, a large AC-coupling capacitor is needed to block the DC bias from the DAC output. The cutoff frequency is calculated as follows:

$$F_C = \frac{1}{2 \times 3.14 \times C \times Z_{load}} \quad (6)$$

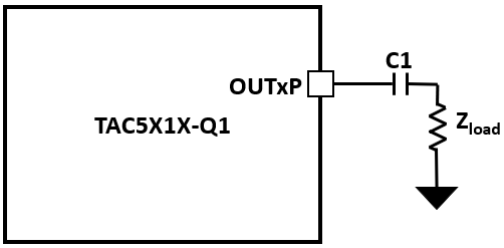

Figure 2-12. AC Equivalent Circuit of Output Pin

For headset (16–32Ω) applications: Use ≥470µF (32Ω) and ≥680–1000µF (16Ω) to maintain F_c = 10–15Hz.

For Line-out loads (≥10kΩ): The capacitor can be small (typically 1–4.7µF).

To avoid the big/expensive caps (and optimize BOM):

1. Use pseudo-differential / cap-less drive (OUTxP/OUTxM both driven): no series caps needed; best for headphones and keeps bass. Configure OUT1x_CFG for pseudo-differential.
2. If single-ended is required:

- Raise the load impedance (use a line receiver/headphone amp with high Z_{in}) so the coupling cap can be 1–4.7µF instead of hundreds of µF
- Select the smallest cap that hits your bass target:
- 32Ω: 470µF approximately 10.6Hz; 680µF approximately 7.4Hz; 1000µF approximately 5Hz
- 16Ω: 680µF ≈ 14.7Hz; 1000µF ≈ 10Hz.
- Prefer aluminum and polymer electrolytic, + terminal toward the DAC (positive common-mode)

3. For line-level outputs:

- Use 1–2.2µF X7R MLCC (cost-effective) or film for lowest THD. 47 µF is overkill for ≥10kΩ loads
- Or DC-couple if the receiver tolerates the DAC V_{CM}.

2.2.2 Output Capacitor Summary

- Headphones/Headset: Use pseudo-differential (cap-less) if possible; otherwise size the electrolytic per F_c target
- Line-out: small 1–4.7µF or DC-couple; ceramics are fine here.

2.2.3 How to Select ESD for Audio Ports

For the ESD protection of the headphone jack, the ESD protection device must be placed near the audio jack connector rather than on the IC side; the microphone (MIC) pin must also be equipped with an ESD protection device. TI recommends using a unidirectional TVS diode with a trigger voltage of approximately 8V and a clamping voltage of about 5V.

2.3 AC-Coupled and DC-Coupled

2.3.1 AC-Coupled Systems

- Coupling capacitors used at the ADC input form a high-pass filter with the input impedance of the ADC limiting the low frequency response of the system. For audio applications, the capacitors are sized such that frequencies as low as 20 Hz can be digitized.
- A coupling capacitor must be charged to a steady state value on power-up. Until the time the capacitor reaches this value, the input audio signal is not passed properly to the ADC. Sometimes this situation is heard as a pop in the audio output.
- A coupling capacitor needs to behave as a short circuit for all AC signals in the audio range. In practice, the capacitance value and the capacitive impedance can change with signal amplitude across the capacitor. This value can result in non-linear behavior and harmonic distortion in ADC output at low frequencies
- Some capacitors also display microphony. When experiencing vibration, the capacitor can induce a voltage in the AC path due to the Piezo Effect.

2.3.2 DC-Coupled Systems

DC-coupled systems eliminate coupling capacitors. The DC-coupled system has the following advantages:

- Lower bill of material cost and less board space
- Performance degradation due to non-linear effects in capacitors can be eliminated including THD degradation at low frequency and board vibration effects
- Start-up pop is eliminated
- The ADC output is valid to DC which allows for the possibility to do measurements such as voltage and current for test and measurement

DC-coupling also has some disadvantages:

- The DC biasing of the input pins is not determined by the ADC circuit but by the external source. Since the biasing is not always optimum, the ADC can display a reduced signal handling

2.4 TAC5212 and TAC5112-Q1 Headset Detection Design

2.4.1 How to Implement Headset Detection

The TAC5212 & TAC5112-Q1 feature comprehensive audio interface monitoring capabilities, enabling status monitoring of headphones, microphones, and headphone jacks, as well as detection of audio plug insertion and identification of the connected headphone type. For TAC5(3/4)12-Q1, headset detection is not supported since the high-voltage analog input requires extra circuitry.

The headset detection function of the TAC5212 & TAC5112-Q1 has clear connection requirements: the microphone (MIC) input (which can be IN1P or IN1M) must be AC-coupled; the output connection of the Digital-to-Analog Converter (DAC) supports both AC-Coupled and DC-Coupled modes. The MICDET signal needs to be connected to the IN2M pin of the device. For headset detection to work, IN2M needs to be DC-coupled; it will not work for AC-coupled inputs. Due to differences in signal transmission characteristics between different output coupling modes, the corresponding headset insertion detection logic also varies. Since CTIA jack headphones are more common, this application note uses the CTIA jack as an example. The core distinction between the CTIA and OMTP standards is the reversed pin assignment for the ground and microphone pins on a 3.5 mm headphone connector.

2.4.1.1 Headset Detection in AC-Coupled Output Mode

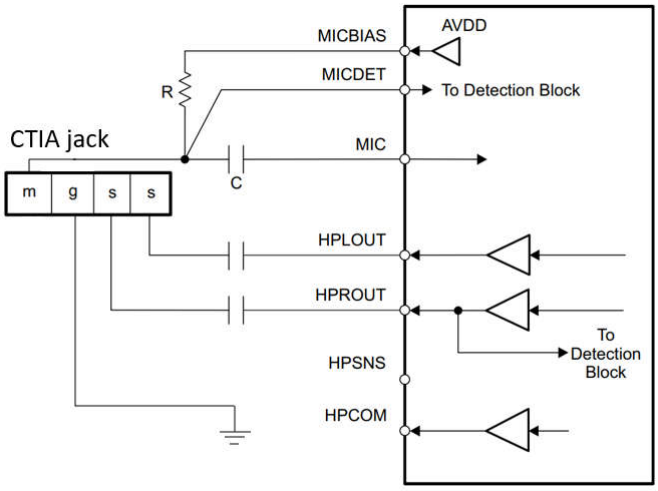

Figure 2-13. Headset Detection Principle in AC-Coupled Output Mode

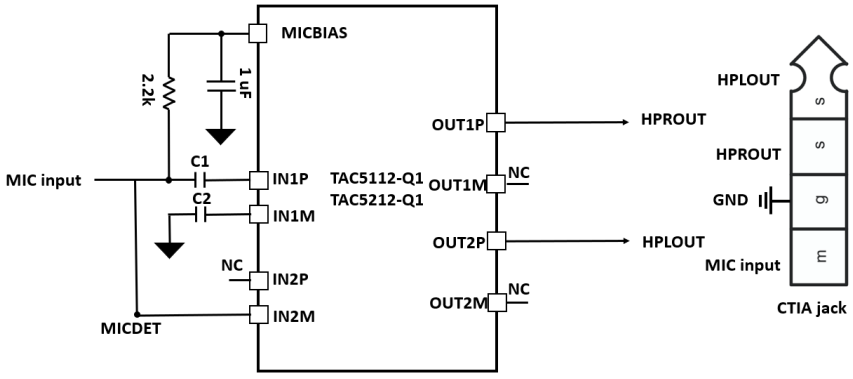

Figure 2-14. Schematic Design in AC-Coupled Output Mode

For the AC-coupled output DAC connection configuration, the headset insertion detection function of TAC5212 & TAC5112-Q1 is implemented by monitoring the voltage change on the MICDET pin to identify whether a headset is inserted and the specific type of the headset. It should be noted that the MICDET pin is connected to the IN2M pin (i.e., MICDET=IN2M), and the IN2M pin is specifically used for headset insertion detection. For a more

detailed description of the principle, please refer to Headset Detection for TAx52xx Family. Regarding the use of the IN2M pin, there is no need to enable Channel 2, as the headset insertion detection circuit is directly connected to the IN2M pin at the physical level.

Detection Sequence – Capacitor Interface

Enable headset detection scheme and set AC-coupled interface (Page 1, Reg 0x1A)

Table 2-1. Principle of Headset Detection in AC-Coupled Output Mode

MICDET Voltage	Headset Detection Result
MICDET < V2	Insertion detected
MICDET > V2	No insertion
MICDET > V1	Headset with mic
MICDET < V1	Headset without mic
Given headset with mic is already detected	
MICDET > V3	No button press
MICDET < V3	Button press detected

V2=(MICBIAS-ref)*(4/5)+ref , V1=(MICBIAS-ref)*(1/5)+ref, and V3=(MICBIAS - ref)*(0.2 or 0.3)+ref, where ref = VSS = 0V.

2.4.1.2 Headset Detection in DC-Coupled Output Mode

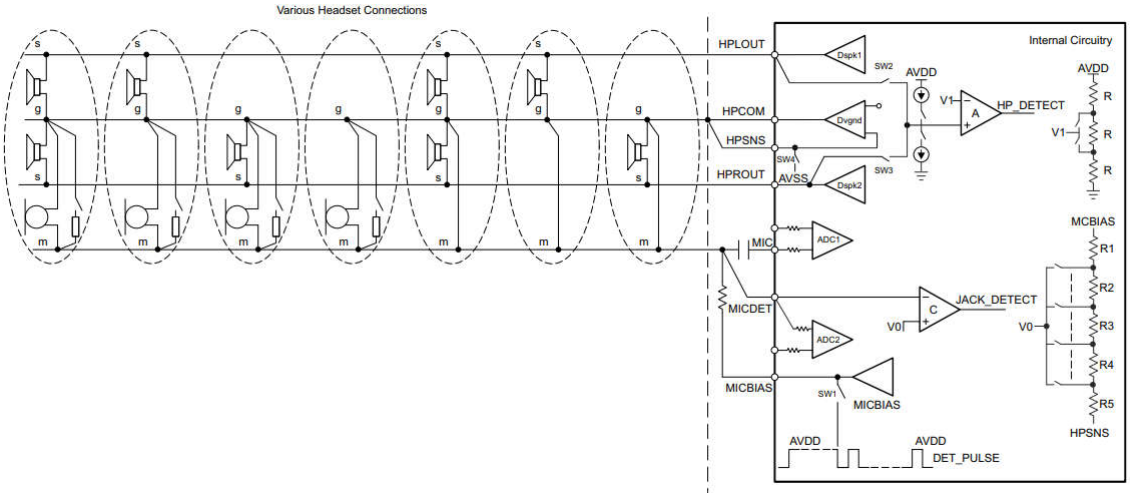

Figure 2-15. Circuit Diagram of Detection Scheme for DC-Coupled Output Mode

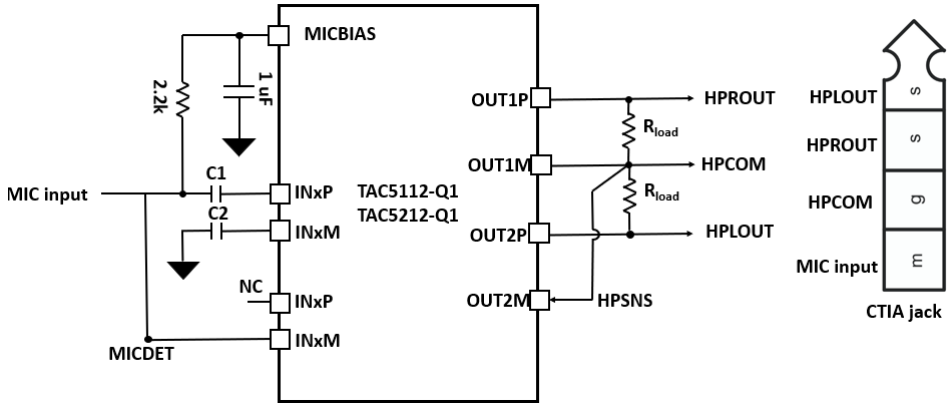

Figure 2-16. Headset Detection Schematic Design in Pseudo-Differential mode

For the pseudo-differential output DAC connection configuration, the headset insertion detection function of TAC5212 & TAC5112-Q1 is implemented by monitoring the voltage changes on the MICDET pin and HPSNS (i.e., OUT2M pin) to identify the insertion status and specific type of the headset. It should be noted that the corresponding relationships of each pin are as follows: MICDET=IN2M, HPSNS=OUT2M, HPROUT=OUT1P, HPLOUT=OUT2P, HPCOM=OUT1M. Use differential/pseudo-differential drive (OUTxP / OUTxM both driven): no series caps needed; best for headphones and keeps bass.

Detection Sequence – Capacitor-less Interface

Enable headset detection scheme and set DC-Coupled (Page 1, Reg 0x1A)

Table 2-2. Principle of Headset Detection in DC-Coupled Output Mode

MICDET Voltage	Headset Detection Result
MICDET < V2	Insertion detected
MICDET > V2	No insertion
MICDET > V1	Headset with mic
MICDET < V1	Headset without mic
Given headset with mic is already detected	
MICDET > V3	No button press
MICDET < V3	Button press detected

V2=(MICBIAS-ref)*(22/25)+ref, V1=(MICBIAS-ref)*(11/100)+ref, and V3=MICBIAS*(11/100)+ref, where ref = HPSNS = Output common-mode voltage.

2.4.2 Debounce and Detection Real-Time Performance of Headset Detection

Physical jitter between the plug and interface during headset insertion/removal causes voltage fluctuations on the detection pin; debouncing filters this interference to prevent false triggers and ensure accurate and stable detection. TAC5212 & TAC5112-Q1 integrates a debounce function for headset detection, enabling accurate detection of the headset type under scenarios with normal insertion and removal speeds. The debounce time can be set by JACK_DET_CFG2 Register (Page 1, Reg 0x1B).

Table 7-120. JACK_DET_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved bit; Write only reset value
6	HPDET_DEB	R/W	0b	Headphone Detection Debounce Programmability 0d = No Debounce 1d = Debounce of 3 detections
5-3	JACK_DET_DEB_INSERT[2:0]	R/W	000b	Headset Insert Detection Debounce Programmability 0d = Debounce Time = 16ms 1d = Debounce Time = 32ms 2d = Debounce Time = 64ms 3d = Debounce Time = 128ms 4d = Debounce Time = 256ms 5d = Debounce Time = 512ms 6d = Reserved 7d = No Debounce
2	JACK_DET_DEB_REMOVAL	R/W	0b	Headset Removal Detection Debounce Programmability 0d = Debounce of 5 detections 1d = Debounce of 3 detections

Figure 2-17. Headset Insert Detection Debounce Configuration

DET_PULSE, which is generated using an internal oscillator, is used for hook button detection. DET_PULSE frequency is 0.5HZ,1Hz,7.5Hz or 15Hz based on reg map control with the high time of 4 or 32ms based on capacitor value on MICBIAS. If the hook button detection needs to be more sensitive, the detection frequency can be increased.

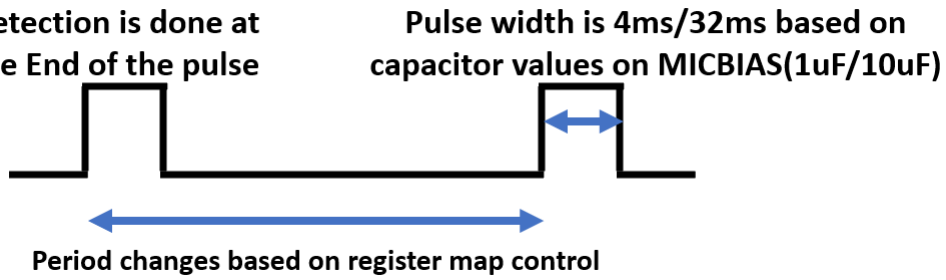

Figure 2-18. Pulse Scheme

Table 7-118. JACK_DET_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	JACK_DET_MONITOR_FREQ[1:0]	R/W	00b	Headset Detection Pulse Frequency 0d = 0.5Hz 1d = 1Hz 2d = 7.5Hz 3d = 15Hz
5	JACK_DET_PULSE_WIDTH	R/W	0b	Detector Pulse High Width 0d = 4ms (MICBIAS PIN Cap = 1 uF) 1d = 32ms (MICBIAS PIN Cap = 10 uF)
4	RESERVED	R	0b	Reserved bit; Write only reset value
3	RESERVED	R	0b	Reserved bit; Write only reset value
2-1	HPDET_CLOCK_SEL[1:0]	R/W	00b	Headphone Detection Clock Time period Select 0d = 1ms 1d = 2ms 2d = 4ms 3d = Reserved
0	RESERVED	R	0b	Reserved bit; Write only reset value

Figure 2-19. Detection Pulse Setting Register

The JACK_DET_CFG1 register is used to control the enablement of headset detection, the coupling type setting for headphone detection, and the hook press detection setting.

Table 7-119. JACK_DET_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	JACK_DET_COMP_CTRL2	R/W	0b	Hook Press Threshold Control in Fixed External Resistance case, controls the choice of Lowest Microphone impedance to be supported or Highest Hook button Impedance to be supported 0d = Minimum Microphone resistance supported, R_Mic = 800 Ωs and Max Hook button impedance supported, R_Hook = 320 Ωs for AC coupled Headphones R26<3> = 0 (else, when R26<3> = 1, R_hook = 150 Ωs) 1d = Max Hook button impedance supported, R_hook = 680 Ωs and Minimum Microphone resistance supported, R_Mic = 1350 Ωs for AC coupled Headphones R26<3> = 0 (else, when R26<3> = 1, R_Mic = 1750 Ωs)
5-4	JACK_DET_COMP_CTRL3[1:0]	R/W	00b	Hook Pressed Jack Insertion support, valid only for External Resistor Type P0_R25_D4 = 0 else Don't care. 0d = supports minimum Hook button impedance of 150 Ωs for Hook Pressed Jack Insertion detection 1d = supports minimum Hook button impedance of 100 Ωs for Hook Pressed Jack Insertion detection 2d = supports minimum Hook button impedance of 50 Ωs for Hook Pressed Jack Insertion detection 3d = Reserved
3	HPDET_COUPLING	R/W	0b	Headphone detect coupling 0d = AC coupled 1d = DC coupled
2	HPDET_USE_2x_CURR	R/W	0b	Headset detect current sel config 0d = 2x current for headphone detection disabled 1d = 2x current for headphone detection enabled
1	JACK_DET_EN	R/W	0b	Headset Detection Enable 0d = Headset Detection Disabled 1d = Headset Detection Enabled
0	RESERVED	R	0b	Reserved bit; Write only reset value

Figure 2-20. Headset Detection Enable and Coupling Type Setting Register

Headset Detection result will update in JACK_DET_CFG2 Register (Address = 0x1B):

Table 7-121. JACK_DET_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	JACK_TYPE_FLAG[1:0]	R	00b	Headset Jack type flag 0d = Jack is not inserted 1d = Jack is inserted without Microphone 2d = Reserved. Do not use 3d = Jack is inserted with Microphone
5-4	HEADSET_TYPE_DET[1:0]	R	00b	Headset type 0d = Headset is not inserted 1d = Jack is inserted with mono-HS (RIGHT) 2d = Jack is inserted with mono-HS (LEFT) 3d = Jack is inserted with stereo-HS
3-0	RESERVED	R	0b	Reserved bits; Write only reset value

Figure 2-21. Headset Detection Result Indicator Register

The way the headset detection scheme works is it detects the insertion first, then starts the Headphone detection with debounce, after the headphones are confirmed, it goes about detecting microphones. Ones this is done an interrupt is generated. Then the flags can be read for status.

After the insertion interrupt is raised, there are no further checks on the type of jack. Headphone type detection is ONE time, during insertion and not real time.

The insertion, removal, and button press status of the headset are detected in real time; while the headset type detection (e.g., stereo headset, mono headset, stereo headset with microphone, mono headset with

microphone) is a one-time detection, which is only updated when the headset is inserted, and the detection result is automatically cleared after removal. In addition, the button press detection function is only activated when a headset with a microphone is detected.

2.4.3 TAC5X1X-Q1 Family Other Advanced Features

1. Support the LOOPBACK function

TAC5X1X-Q1 supports the LOOPBACK function, which refers to the operation of feeding electronic signals or data streams back to the sender unchanged. Loopback is the *self-diagnostic tool* of a codec, enabling users to quickly locate faults and easily verify the overall performance of the codec.

Common Loopback Types:

Digital Loopback

- Path: Digital input signal → Internal digital link of the codec → Directly looped back to digital output (bypassing ADC/DAC analog conversion)
- Applicable Scenarios: Verifying digital interfaces (for example., I2S, TDM), digital codec algorithms, and internal digital filtering circuits
- Automotive Application Example: Verifying the I2S communication link between the on-board SoC and codec (SoC transmits digital audio → codec performs digital loopback → SoC receives it, ensuring communication without frame loss or bit error)

Digital Loopback Configuration can be set by INTF_CFG1 Register (P0 R16):

Table 7-17. INTF_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DOUT_SEL[3:0]	R/W	0101b	DOUT select configuration. 0d = DOUT is disabled 1d = DOUT is configured as input 2d = DOUT is configured as a general-purpose output (GPO) 3d = DOUT is configured as a chip interrupt output (IRQ) 4d = DOUT is configured as a PDM clock output (PDMCLK) 5d = DOUT is configured as primary ASI DOUT 6d = DOUT is configured as primary ASI DOUT2 7d = DOUT is configured as secondary ASI DOUT 8d = DOUT is configured as secondary ASI DOUT2 9d = DOUT is configured as secondary ASI BCLK output 10d = DOUT is configured as secondary ASI FSYNC output 11d = DOUT is configured as general purpose CLKOUT 12d = DOUT is configured as PASI DOUT and SASI DOUT muxed 13d = DOUT is configured as DAISY_OUT for DIN Daisy 14d = DOUT is configured as DIN (LOOPBACK) 15d = Reserved
3	DOUT_VAL	R/W	0b	DOUT output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1
2-0	DOUT_DRV[2:0]	R/W	010b	DOUT output drive configuration. 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved; Don't use

Figure 2-22. Digital Loopback Configuration Register

Analog Loopback

- Path: Analog input (microphone analog signal) → ADC converts to digital signal → DAC converts back to analog signal → Looped back to analog output (complete analog + digital link)
- Applicable Scenarios: Verifying ADC/DAC conversion performance (Total THD+N of ADC + DAC), analog amplification circuits (PGA), and anti-interference capability (analog signal fidelity in the on-board high electromagnetic environment)
- Automotive Application Example: Testing the on-board microphone input link (analog audio → codec → analog loopback output, verifying no noise and compliant gain)

Analog Loopback AC-Couple Single-ended IN1 to HP path Configuration Example

w a0 00 00 # Set page 0

w a0 01 01 # Software Reset

w a0 02 09 # Wake up with AVDD > 2v and all VDDIO level

w a0 50 50 # ADC Ch1 s-e input, 10KOhm, 1Vrms ac-coupled, audio band

w a0 64 4c # Configure OUT1M as mono single-ended in Analog Bypass path (Analog Loopback setting)

w a0 66 60 # Configure OUT1M as Headphone Driver

w a0 76 cc # Enable Input and Output Ch1 and Ch2 channels

w a0 78 e0 # Power up ADC, DAC and MICBIAS

Note: For single-ended loopback, IN1P is routed to OUT1M.

2. Flexible Slot Adjustment Function

TAC5X1X-Q1 supports up to two analog input channels and four analog output channels, which can be configured on the main ASI bus to map their audio data to Slots 0 to 31 of the bus.

3 Summary

This application note focuses on the core design content of the TAC5X1X-Q1 in automotive headset scenarios, aiming to provide clear design guidelines for hardware engineers. This document first elaborates on the hardware schematic design specifications of the analog input and output terminals of the chip, including the selection of key circuit parameters and the application scenarios of AC-/DC-Coupled methods. Then, the document focuses on explaining the implementation logic of the headset insertion detection function, the design of the debounce mechanism, and the key points of real-time performance optimization to ensure the reliable identification and rapid response of headset plug-in and plug-out operations. At the same time, this application note briefly introduces other advanced features of this series of chips to help engineers fully tap the chip potential.

3.1 Configuration Example

Below is an example of headphone configuration. The best way to generate the initial configuration is to use TI's PurePath™ Console (graphical interface) for setup.

Differential Headphone Playback through Stereo OUT1P and OUT2P, Headset Detection enabled

Target Mode, TDM, 16-bit, Primary ASI only, multiple of 48KHz Sampling

w a0 0x00, 0x00 # Select page 0

w a0 0x01, 0x01 # Software Reset

w a0 0x02, 0x09 # Wake up with AVDD > 2v and all VDDIO level

w a0 0x10, 0x52 # DOUT is configured as primary ASI DOUT & select Drive active low and weak high

w a0 0x19, 0x40 # Config 2 data outputs for Primary ASI

w a0 0x1a, 0x04 # ASI BCLK polarity: Inverted polarity with respect to standard protocol

w a0 0x1e, 0x20 # PASI_TX_CH1_CFG, config as TDM slot 0

w a0 0x1f, 0x01 # PASI_TX_CH2_CFG, config Primary ASI channel 2 output in a tri-state condition

w a0 0x28, 0x20 # PASI_RX_CH1_CFG, config as TDM slot 0

w a0 0x29, 0x28 # PASI_RX_CH2_CFG, config as TDM slot 8

w a0 0x50, 0x50 # ADC_CH1_CFG0. Analog single-ended input & AC-coupled input

w a0 0x52, 0xe7 # Record digital volume up to 35db

w a0 0x64, 0x28 # OUT1x_CFG: 2d = Mono single-ended with output at OUT1P only (DAC1A + DAC1B -> OUT1P) & OUT1x_VCOM: 0.6 * Vref

w a0 0x65, 0x60 # OUT1P_DRIVE: 1d = Headphone driver with minimum 16ohm single ended impedance

w a0 0x6b, 0x28 # OUT2x_CFG: 2d = Mono single-ended with output at OUT1P only (DAC1A + DAC1B -> OUT1P) & OUT1x_VCOM: 0.6 * Vref

w a0 0x6c, 0x60 # OUT2P_DRIVE: 1d = Headphone driver with minimum 16o single ended impedance

w a0 0x76, 0x8c # CH_EN Register: IN_CH1_EN = 1, OUT_CH1_EN = 1, OUT_CH2_EN = 1

w a0 0x00, 0x01 # Select page 1

w a0 0x19, 0x84 # Set Headset Detection Pulse Frequency = 7.5Hz and Clock Time = 4ms

w a0 0x1A, 0x02 # Headset Detection Enabled, AC coupled

w a0 0x1B, 0x28 # Debounce Time = 512ms

w a0 0x00, 0x00 # Select page 0

w a0 0x78, 0xe0 # Power up MICBIAS & Power up all enabled DAC channels & Power up all enabled ADC and PDM channels

4 References

1. Texas Instruments, *TAC5112-Q1 Automotive low-power stereo audio codec with 105 dB dynamic range ADC and 114 dB dynamic range DAC datasheet*, datasheet.
2. Texas Instruments, *TAC5412-Q1 Automotive Stereo Audio Codec with 112 dB ADC, 120 dB DAC, High-Voltage Input, Micbias and Diagnostics datasheet* datasheet.
3. Texas Instruments, *Headset Detection for TAx52xx Family* application note.
4. Texas Instruments, *Working With Analog Inputs in the TLV320ADCX120 and PCMX120-Q1 Family* application note.
5. Texas Instruments, *Analog Input Configurations, Mixing and Muxing of TAx5x1x Devices* application note.
6. Texas Instruments, *TAx5xxx-Q1 Fault Diagnostic Features*, application note.

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