

Atul Patel

Most engineers are familiar with the classic open drain level shifting implementation that uses simple MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) and a combination of a few discrete components (see [Example Singel Bit Discrete Open-Drain Level Translation Implementation](#)). Given the implementation simplicity and low cost, variations of the MOSFET based open drain level shifter circuits have been used by engineers for a very long time and this approach remains a frequently used tool in a design engineer's tool box.

Using a discrete open drain level shifter implementation does require designers to accept compromises such as reduced data rates, higher levels of power consumption, and large implementation size. Historically, these compromises might not have had a critical impact on the target application enabling designers to accept the compromises of the traditional discrete approach. However, today design engineers are challenged with designing systems that are not only lower cost but also lower power, higher performance, and much smaller in terms of form factor.

The modern system design challenges that system designers face can make using traditional discrete open drain level shifting difficult if not impossible in many cases. See [Table 1](#). For example, a battery operated [video doorbell](#) is not likely to have the needed board area and power budget to implement a traditional discrete open drain level shifter design. Similarly, a hand-held [Mobile Point of Sale \(POS\) terminal](#), that needs to maximize battery life while still maintaining a small form factor, cannot afford the compromises a discrete design can require.

How can system designers enjoy many of the benefits of discrete open drain level translation while meeting the modern system design challenges of smaller system form factors, power efficiency, and higher performance? The simple answer is to use power efficient integrated level shifter circuits that are now [available in small uQFN packaging technologies](#). The [latest integrated open drain level shifters](#) enable designers to implement 0.95-V to 5.5-V open drain level shifting with the flexibility of external resistor

components, that engineers are accustomed to, but without the large MOSFET footprint.

Integrated open drain level shifters can replace MOSFET based open drain level shifting implementations as shown in [Figure 1](#). The benefit of using new integrated level shifters is that the devices are now widely available in small uQFN packages that are considerably smaller than SOT packaging of low-cost MOSFETs enabling much smaller circuit implementations. uQFN packages are more than three times smaller than the SOT-23 package commonly used for MOSFETs. In addition, an integrated level shifter device consumes much lower power and supports higher data rates than discrete based implementations. Unlike MOSFETs, integrated open drain level shifters are designed not to suffer from high leakage that is common with traditional MOSFET designs. Given the always on nature of MOSFET based implementations, discrete implementations can greatly reduce the battery life of the application they are used in.

Integrated level shifter devices also have additional benefits not found with MOSFET based implementations such as built-in ESD protection and deterministic data sheet specifications such as switching characteristics that enable more robust higher performance designs. For example, [LSF0101DTQR](#) (single channel), [PCA9306DQER](#) (dual channel) and [LSF0102DQER](#) (dual channel) open drain level shifters from TI enable system designers to achieve smaller, power efficient and higher performance designs while still maintaining the flexibility of external resistors of the discrete approach that designers might want.

TI's [TXS family](#) of open drain level translators offers the added benefit of integrated pull-up resistors further reducing component count. Devices like [TXS0102DQER](#) can be used for level shifting interfaces such as I<sup>2</sup>C in space constrained use cases. The cost benefit of discrete designs is greatly diminished when cost of additional components and ESD protection is considered. The benefits of using integrated open drain level shifters, for example, are multiplied when you consider that most systems

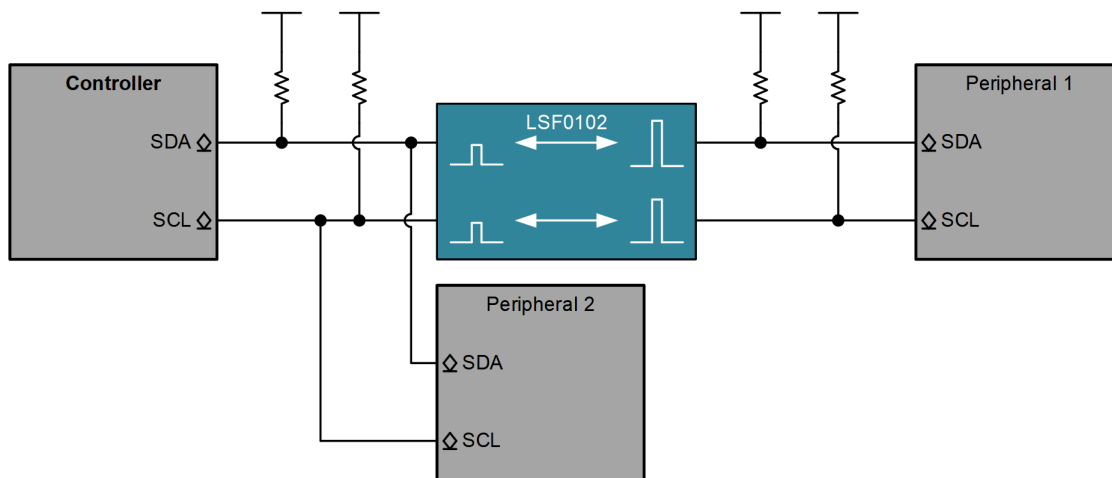
have multiple bits or interfaces that need open drain level shifting. Using discrete devices to implement multiple level shifting channels dramatically increases the number of components that need to be sourced and implemented for a design.

Level shifter devices such as LSF0101DTQR, PCA9306DQER, and LSF0102DQER enable

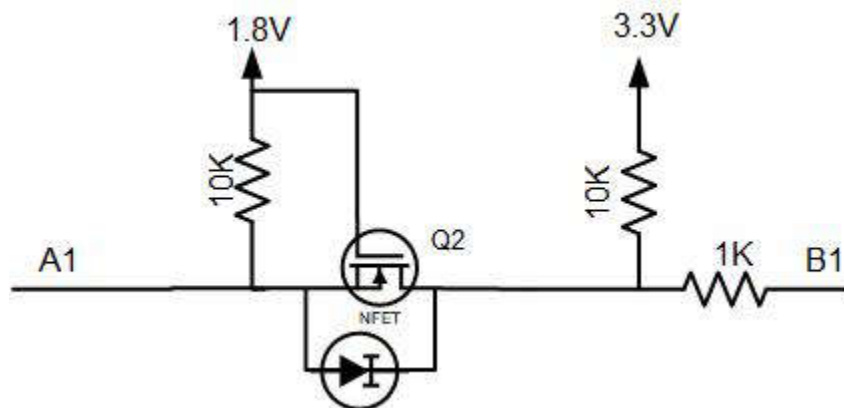
designers to implement more robust and efficient open drain translation in the next generation of system designs while helping designers achieve modern system design goals. For more information on the [LSF series](#), [PCA/TCA series](#), and [TXS series](#) of level translation designs, please visit [TI's level translation landing page](#).

**Table 1. Integrated vs. Discrete Level Translation**

	Integrated Level Translation	Discrete Level Translation
Implementation Complexity	Low	High
Component Count	Low	High
Power Dissipation/Bit	Low	High
Known Rise/Fall Times	Yes	No
Higher Data Rate Support	Yes	Limited
Signal Glitching	No	Likely
External ESD Needed	No	Yes
Power Sequencing Needed	No	Yes



**Figure 1. Integrated Level Translation using LSF0102 Level Translator**



**Figure 2. Example Single Bit Discrete Open-Drain Level Translation Implementation**

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated