Functional Safety Information

TPS37-Q1 and TPS38-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

1 Overview.....2
2 Functional Safety Failure In Time (FIT) Rates.....3
3 Failure Mode Distribution (FMD).....4
4 Pin Failure Mode Analysis (Pin FMA).....5

Trademarks

1 Overview

This document contains information for TPS37-Q1 and TPS38-Q1 (DSK package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

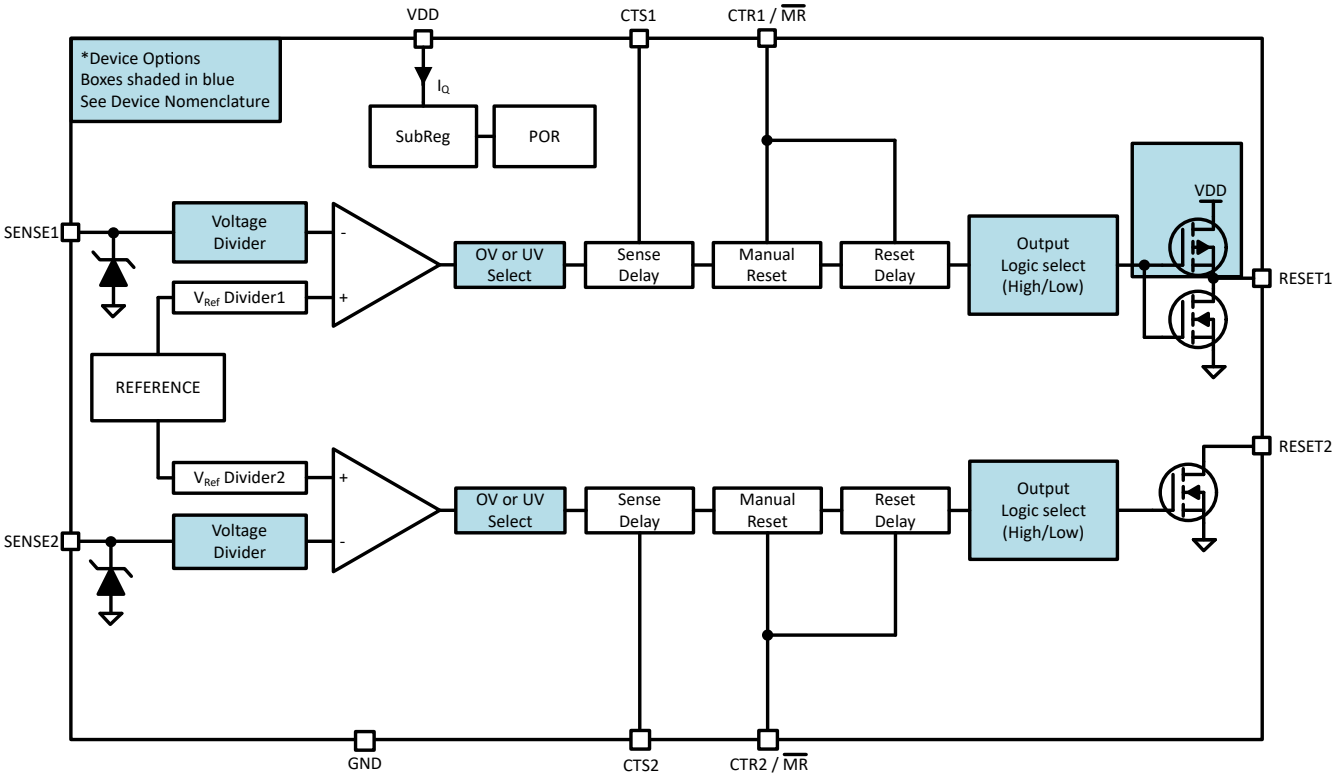

Figure 1-1. Functional Block Diagram

TPS37-Q1 and TPS38-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS37-Q1 and TPS38-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5
Die FIT Rate	2
Package FIT Rate	3

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 364 µW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS37-Q1 and TPS38-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
RESET1_XXXX / fails to trip	8%
RESET1_XXXX / false trip	8%
RESET1_XXXX / trip outside specification (voltage or time)	31%
RESET1_XXXX / delay outside specification	3%
RESET2_XXOD / fails to trip	8%
RESET2_XXOD / false trip	8%
RESET2_XXOD / trip outside specification (voltage or time)	31%
RESET2_XXOD / delay outside specification	3%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS37-Q1 and TPS38-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS37-Q1 and TPS38-Q1 pin diagram. For a detailed description of the device pins please refer to *TPS37-Q1* or *TPS38-Q1* in the *Pin Configuration and Functions* section of the data sheet.

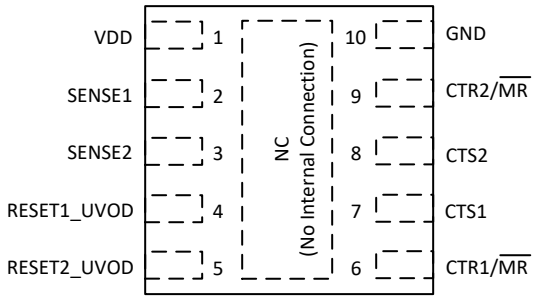

Figure 4-1. Pin Diagram DSK Package 10-Pin WSON

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- RESET1_UVOD and RESET2_UVOD are pictured as active high, some configurations ($\overline{\text{RESET1}}$_UVOD and $\overline{\text{RESET2}}$_UVOD) will be active low. RESET1_UVOD in Figure 4-1 is shown as open-drain, some configurations will be push-pull. Refer to *TPS37-Q1* or *TPS38-Q1* *Pin Configuration and Functions* section of the data sheet.
- At $V_{DD\ (MIN)} \leq VDD \leq V_{DD\ (MAX)}$, CTR1 / $\overline{\text{MR}}$ = CTR2 / $\overline{\text{MR}}$ = CTS1 = CTS2 = Open
- Output reset Pullup Resistor (R_{PULLUP}) = 10 kΩ, Output reset pullup voltage (V_{PULLUP} = 5.5 V, output reset load (C_{LOAD}) = 10 pF.
- Tables valid over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted.
- Typical values are at T_A = 25°C, VDD = 16 V, and V_{IT} = 6.5 V (V_{IT} refers to V_{ITN} or V_{ITP}) unless stated otherwise.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
VDD	1	VDD short to GND Fault	B
SENSE1	2	Functionality affected if intent is not to monitor GND	B
SENSE2	3	Functionality affected if intent is not to monitor GND	B
RESET1_UVOD	4	If open drain option: Unreliable device operation if not shorted to V_{OH}	B
		If push pull option: Not recommended condition	A
RESET2_UVOD	5	Unreliable device operation if not shorted to V_{OH}	B
CTR1 / $\overline{MR}$	6	Normal operation, RESET1_UVOD will be asserted.	D
CTS1	7	Normal operation, RESET1_UVOD will be asserted.	D
CTS2	8	Normal operation, RESET2_UVOD will be asserted.	D
CTR2 / $\overline{MR}$	9	Normal operation, RESET2_UVOD will be asserted.	D
GND	10	Normal operation	D
Central Pad	PAD	Normal operation, Pad is not internally connected	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
VDD	1	Device Unpowered	B
SENSE1	2	For fixed voltage threshold option where the applied voltage to SENSE1 is less than 2.7 V, SENSE1 pin will detect a short to GND. For 800 mV SENSE1 voltage option, the input state will be undetermined.	B
SENSE2	3	For fixed voltage threshold option where the applied voltage to SENSE2 is less than 2.7 V, SENSE2 pin will detect a short to GND. For 800 mV SENSE2 voltage option, the input state will be undetermined.	B
RESET1_UVOD	4	Unreliable RESET1_UVOD	B
RESET2_UVOD	5	Unreliable RESET2_UVOD	B
CTR1 / $\overline{MR}$	6	Normal operation	D
CTS1	7	Normal operation	D
CTS2	8	Normal operation	D
CTR2 / $\overline{MR}$	9	Normal operation	D
GND	10	Device Unpowered	B
Central Pad	PAD	Normal operation, pad is not internally connected	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

PIN NAME	PIN NO.	SHORTED TO	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
VDD	1	SENSE1	Functionality affected if intent is not to monitor VDD	B
SENSE1	2	SENSE2	Functionality affected if intent is not to monitor SENSE2	B
SENSE2	3	RESET1_UVOD	Functionality affected if intent is not to monitor RESET1_UVOD	B
RESET1_UVOD	4	RESET2_UVOD	If open drain option: Unreliable device operation if not shorted to V_{OH}	B
RESET1_UVOD	4	RESET2_UVOD	If push pull option: Not recommended condition	A
CTR1 / $\overline{MR}$	6	CTS1	Unreliable timing	B
CTS1	7	CTS2	Unreliable timing	B
CTS2	8	CTR2 / $\overline{MR}$	Unreliable timing	B
CTR2 / $\overline{MR}$	9	GND	Normal operation, a reset event will be asserted.	D
Central Pad	PAD	N/A	N/A	N/A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
VDD	1	Normal operation	D
SENSE1	2	Functionality affected if intent is not to monitor VDD	B
SENSE2	3	Functionality affected if intent is not to monitor VDD	B
RESET1_UVOD	4	Open drain option: Pullup resistor required. Short directly to VDD will affect pullup voltage functionality	B
		Push pull option: Not recommended condition	A
RESET2_UVOD	5	Pullup resistor required. Short directly to VDD will affect pullup voltage functionality	B
CTR1 / $\overline{MR}$	6	May damage device if VDD is greater than the pin's recommended operating condition	A
CTS1	7	May damage device if VDD is greater than the pin's recommended operating condition	A
CTS2	8	May damage device if VDD is greater than the pin's recommended operating condition	A
CTR2 / $\overline{MR}$	9	May damage device if VDD is greater than the pin's recommended operating condition	A
GND	10	VDD short to GND Fault	B
Central Pad	PAD		D

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