Functional Safety Information

UCC27531-Q1
Functional Safety FIT Rate, FMD, and Pin FMA

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Trademarks

1 Overview

This document contains information for UCC27531-Q1 (SOT-23 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

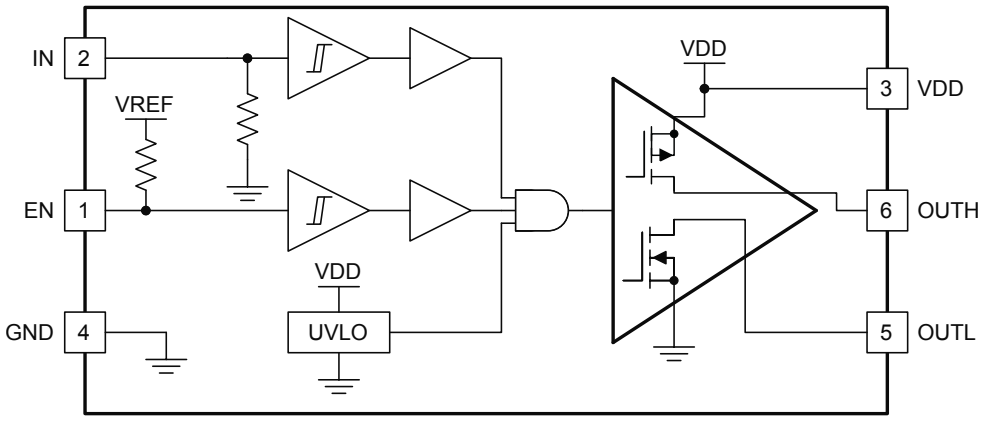

Figure 1-1. Functional Block Diagram

UCC27531-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for UCC27531-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate (15 mW, 150 mW)	5,8
Die FIT Rate (15 mW, 150 mW)	3,6
Package FIT Rate (15 mW, 150 mW)	2,2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 15 mW, 150 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC27531-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUTH stuck on. OUTL stuck off	33%
OUTH stuck on. OUTL stuck off	33%
OUTH and OUTL level undefined.	33%
UVLO not functioning or other failures	<1%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the UCC27531-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the UCC27531-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC27531-Q1 data sheet.

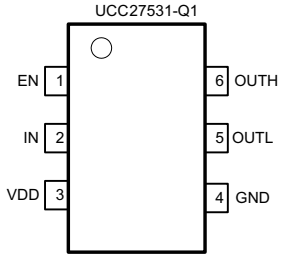

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Pin short across the package is not considered.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	OUTH and OUTL always enabled and follows IN.	B
IN	2	OUTL is on. OUTH is off.	B
VDD	3	Device is unpowered.	B
GND	4	Short to same potential. No impact.	D
OUTL	5	OUTL is always pull down to GND. Possible OUTH and OUTL driver damage.	A
OUTH	6	OUTH is always pull down to GND. Possible OUTH and OUTL driver damage.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	OUTH and OUTL are always enabled.	B
IN	2	OUTH is off and OUTL is on.	B
VDD	3	Device is unpowered.	B
GND	4	OUTH and OUTL are pulled to VDD level.	B
OUTL	5	OUTL is not connected to power FET.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUTH	6	OUTH is not connected to power FET.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	IN	Externally driven input pins shorted. Device responds according to voltage applied to the pins.	B
IN	2	VDD	OUTH is always on and OUTL is always off.	B
GND	4	OUTL	OUTL is always pull down to GND. Possible OUTH and OUTL driver damage.	A
OUTL	5	OUTH	OUTH and OUTL output voltages are unknown. Possible OUTH and OUTL driver damage.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	Case1: Device is always enabled. Case2: Possible device damage VDD > 27 V.	Case1:B Case2:A
IN	2	Case1: OUTH is ON and OUTL is off. Case2: Possible device damage VDD > 27 V.	Case1:B Case2:A
VDD	3	Short to same potential. No impact.	D
GND	4	Device is unpowered.	B
OUTL	5	Possible OUTH and OUTL driver damage.	A
OUTH	6	Possible OUTH and OUTL driver damage.	A

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