Functional Safety Information

OPA858-Q1
Functional Safety FIT Rate and Pin FMA

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Trademarks

1 Overview

This document contains information for OPA858-Q1 (WSON-8 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Pin failure mode analysis (Pin FMA)

OPA858-Q1 shows the device functional block diagram for reference.

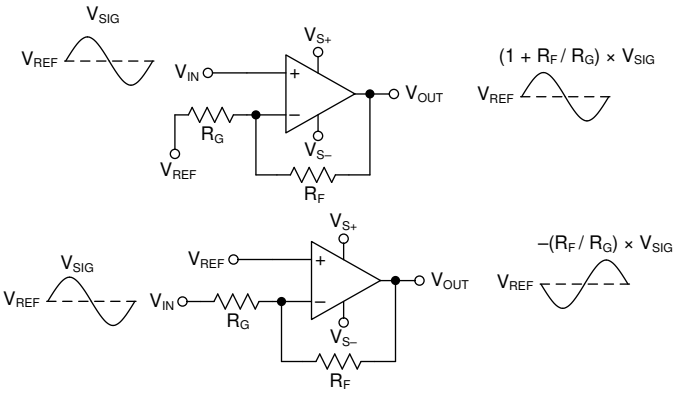

Figure 1-1. Functional Block Diagram

OPA858-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for OPA858-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5
Die FIT Rate	3
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 120 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op Amp, Comparators, Voltage Monitors	4	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the OPA858-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 3-2)
- Pin open-circuited (see Table 3-3)
- Pin short-circuited to an adjacent pin (see Table 3-4)
- Pin short-circuited to V+ (see Table 3-5)

Table 3-2 through Table 3-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 3-1.

Table 3-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 3-1 shows the OPA858-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the OPA858-Q1 data sheet.

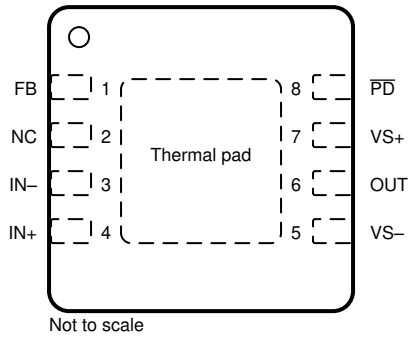

Figure 3-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Total supply voltage of 5 V with VS+ connected to 5 V and VS- connected to ground
- Input and output pins biased to 2.5 V reference point
- Device is configured with feedback network in gain greater than or equal to 7 V/V

Table 3-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1	FB	May cause device to overheat.	A
2	NC	No internal connection to die; normal operation. Not recommended because of potential coupling.	C
3	IN-	Input at VS- (GND) is valid input; however, desired application result is unlikely.	C
4	IN+	Input at VS- (GND) is valid input; however, desired application result is unlikely.	C
5	VS-	Normal operation, unless dual supply voltage was intended.	D
6	OUT	May cause device to overheat.	A
7	VS+	Diodes from input to VS+ may turn on due to input signal and cause electrical overstress (EOS).	A
8	$\overline{PD}$	Power-down connection is set to logic low. Amplifier is disabled, output is placed in a high-impedance state, and power consumption is reduced.	B

Table 3-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1	FB	Feedback pin can be left open. There is no effect on the IC, since the pin is internally connected to the output of the amplifier.	C
2	NC	No internal connection to die; normal operation. Leaving this pin floating leads to best overall application performance.	D
3	IN-	Floating input; circuit will likely not function as expected.	C
4	IN+	Floating input; circuit will likely not function as expected.	C
5	VS-	Lowest voltage pin will try to power the device's VS- pin.	B
6	OUT	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
7	VS+	Highest voltage pin will try to power the device's VS+ pin.	B
8	$\overline{PD}$	Power-down pin can be left open. The pin will be pulled to VS+ through the internal 75 kΩ, which will enable the amplifier. This is not recommended because of potential coupling.	C

Table 3-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
1	FB	NC	NC has no internal connection to die, and FB is internally connected to the output of the amplifier. There is no damage to device, but circuit might not function as expected.	C
2	NC	IN-	No damage to device. Application circuit will not work.	C
3	IN-	IN+	No damage to device. Application circuit will not work.	C
4	IN+	VS-	Input at VS- (GND) is valid input; however, desired application result is unlikely. Pins are not adjacent to each other.	C
5	VS-	OUT	May cause device to overheat.	A
6	OUT	VS+	May cause device to overheat.	A
7	VS+	$\overline{PD}$	Power-down connection is set to logic high. Amplifier is enabled and operates normally.	D
8	$\overline{PD}$	FB	Depending on the voltage at the output of the amplifier, the amplifier might be disabled or enabled following the voltage threshold specified in the device data sheet. Pins are not adjacent to each other.	B

Table 3-5. Pin FMA for Device Pins Short-Circuited to VS+

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1	FB	May cause device to overheat.	A
2	NC	No internal connection to die; normal operation. Not recommended because of potential coupling.	C
3	IN-	Input at VS+ is a valid input; however, desired application result is unlikely.	C
4	IN+	Input at VS+ is a valid input; however, desired application result is unlikely.	C
5	VS-	Diodes from input to VS- may turn on due to input signal and cause electrical overstress (EOS).	A
6	OUT	May cause device to overheat.	A
7	VS+	Normal operation.	D
8	$\overline{PD}$	Power-down connection is set to logic high. Amplifier is enabled and operates normally.	D

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