Functional Safety Information

LM5021
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

All trademarks are the property of their respective owners.

1 Overview

This document contains information for the LM5021 (VSSOP and PDIP packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

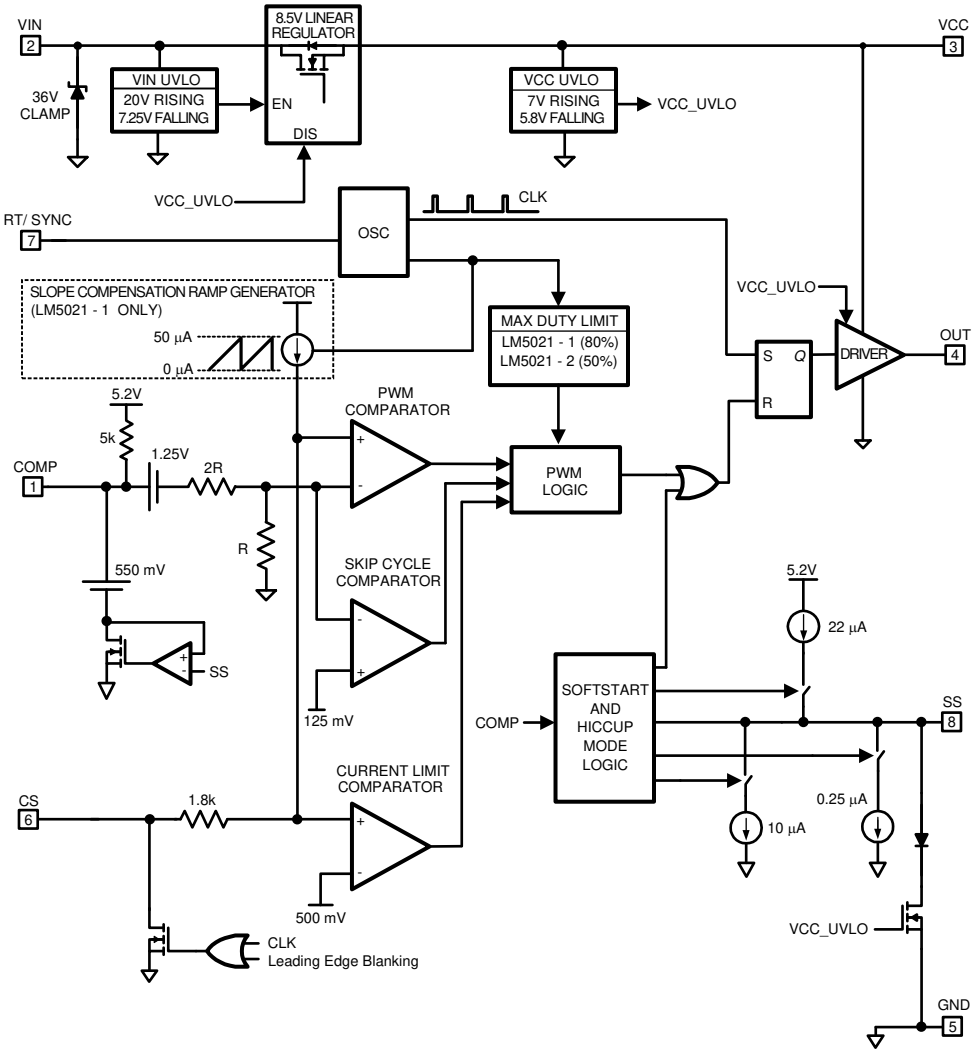

Figure 1-1. Functional Block Diagram

The LM5021 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VSSOP Package

This section provides functional safety failure in time (FIT) rates for the VSSOP package of the LM5021 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate (150 mW, 30 mW)	9, 7
Die FIT rate (150 mW, 30 mW)	5, 3
Package FIT rate (150 mW, 30 mW)	4, 4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 150 mW, 30 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 PDIP Package

This section provides functional safety failure in time (FIT) rates for the PDIP package of the LM5021 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate (150 mW, 30 mW)	22, 21
Die FIT rate (150 mW, 30 mW)	3, 3
Package FIT rate (150 mW, 30 mW)	19, 18

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 150 mW, 30 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM5021 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT operates with wrong duty cycle	30
OUT operates with wrong frequency	10
OUT stays low	28
OUT stays high	8
No effect	24

The FMD in Table 3-1 excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM5021 (VSSOP and PDIP packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6.)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The circuit connection is based on LM5021 data sheet *Figure 14. Typical Application Circuit*.
- VIN is considered as the supply pin.

4.1 VSSOP Package

Figure 4-1 shows the LM5021 pin diagram for the VSSOP package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM5021 data sheet.

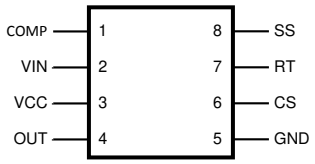

Figure 4-1. Pin Diagram (VSSOP) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	OUT remains low. Converter has no output.	B
VIN	2	IC is not biased. OUT remains low. Converter has no output.	B
VCC	3	IC is not biased. OUT remains low. Converter has no output.	B
OUT	4	OUT remains low. Converter has no output. IC might get damaged.	A
GND	5	No effect.	D
CS	6	OUT operates with maximum duty cycle. Power stage might get damaged. Once power stage is damaged, the IC might get damaged.	A
RT	7	OUT operates with maximum frequency. Converter might have no output. Over load protection might be triggered. OUT remains low after protection is triggered. OUT keeps retrying.	B
SS	8	OUT remains low. Converter has no output.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	Over load protection is triggered. OUT remains low. OUT keeps retrying. Converter has no output.	B
VIN	2	IC is not biased. OUT remains low. Converter has no output.	B
VCC	3	VCC linear regulator might become unstable. UVLO will be triggered and converter has no output.	B
OUT	4	Converter has no gate driver voltage. Converter has no output.	B
GND	5	IC behavior is unpredictable. IC damage is possible.	A
CS	6	OUT operates with minimum on time. Converter has no power handling capability. Over load protection might be triggered. OUT remains low after protection is triggered. OUT keeps retrying.	B
RT	7	Converter operates with minimum switching frequency. Converter has no output. Over load protection might be triggered. OUT remains low after protection is triggered. OUT keeps retrying.	B
SS	8	Lost soft start function.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	VIN	COMP pin stays high, OUT duty cycle is maximum. Converter output loses regulation. Over load protection might be triggered. OUT remains low after protection is triggered. OUT keeps retrying. IC might get damaged.	A
VIN	2	VCC	VCC loses linear regulation function. IC damage is possible.	A
VCC	3	OUT	OUT remains high. Power stage will be damaged. IC damage is possible.	A
OUT	4	N/A		
GND	5	CS	OUT operates with maximum duty cycle. Power stage damage is possible. Once power stage is damaged, IC damage is possible.	A
CS	6	RT	OUT operates with maximum frequency. Converter might have no output. Over load protection might be triggered. OUT remains low after protection is triggered. OUT keeps retrying.	B
RT	7	SS	OUT operates with maximum frequency. Converter might have no output. Over load protection might be triggered. OUT remains low after protection is triggered. OUT keeps retrying.	B
SS	8	N/A		

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	COMP pin stays high, OUT duty cycle is maximum. Converter output loses regulation. IC might get damaged. Over load protection might be triggered. OUT remains low after protection is triggered. OUT keeps retrying.	A
VIN	2	No effect.	D
VCC	3	VCC loses linear regulation function. IC damage is possible.	A
OUT	4	OUT remains high. Power stage will be damaged. IC damage is possible.	A
GND	5	IC is not biased. OUT remains low. Converter has no output.	B
CS	6	OUT has minimum on time. IC damage is possible.	A
RT	7	OUT remains low. IC damage is possible.	A
SS	8	Soft start function is lost. IC damage is possible.	A

4.2 PDIP Package

Figure 4-2 shows the LM5021 pin diagram for the PDIP package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM5021 data sheet.

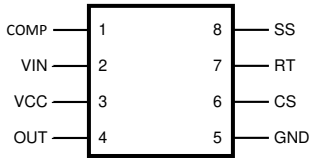

Figure 4-2. Pin Diagram (PDIP Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	OUT remains low. Converter has no output.	B
VIN	2	IC is not biased. OUT remains low. Converter has no output.	B
VCC	3	IC is not biased. OUT remains low. Converter has no output.	B
OUT	4	OUT remains low. Converter has no output. IC might get damaged.	A
GND	5	No effect.	D
CS	6	OUT operates with maximum duty cycle. Power stage might get damaged. Once power stage is damaged, the IC might get damaged.	A
RT	7	OUT operates with maximum frequency. Converter might have no output. Over load protection might be triggered. OUT remains low after protection is triggered. OUT keeps retrying.	B
SS	8	OUT remains low. Converter has no output.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	Over load protection is triggered. OUT remains low. OUT keeps retrying. Converter has no output.	B
VIN	2	IC is not biased. OUT remains low. Converter has no output.	B
VCC	3	VCC linear regulator might become unstable. UVLO will be triggered and converter has no output.	B
OUT	4	Converter has no gate driver voltage. Converter has no output.	B
GND	5	IC behavior is unpredictable. IC damage is possible.	A
CS	6	OUT operates with minimum on time. Converter has no power handling capability. Over load protection might be triggered. OUT remains low after protection is triggered. OUT keeps retrying.	B
RT	7	Converter operates with minimum switching frequency. Converter has no output. Over load protection might be triggered. OUT remains low after protection is triggered. OUT keeps retrying.	B
SS	8	Lost soft start function.	C

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	VIN	COMP pin stays high, OUT duty cycle is maximum. Converter output loses regulation. Over load protection might be triggered. OUT remains low after protection is triggered. OUT keeps retrying. IC might get damaged.	A
VIN	2	VCC	VCC loses linear regulation function. IC damage is possible.	A
VCC	3	OUT	OUT remains high. Power stage will be damaged. IC damage is possible.	A
OUT	4	N/A		
GND	5	CS	OUT operates with maximum duty cycle. Power stage damage is possible. Once power stage is damaged, IC damage is possible.	A
CS	6	RT	OUT operates with maximum frequency. Converter might have no output. Over load protection might be triggered. OUT remains low after protection is triggered. OUT keeps retrying.	B
RT	7	SS	OUT operates with maximum frequency. Converter might have no output. Over load protection might be triggered. OUT remains low after protection is triggered. OUT keeps retrying.	B
SS	8	N/A		

Table 4-9. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	COMP pin stays high, OUT duty cycle is maximum. Converter output loses regulation. IC might get damaged. Over load protection might be triggered. OUT remains low after protection is triggered. OUT keeps retrying.	A
VIN	2	No effect.	D
VCC	3	VCC loses linear regulation function. IC damage is possible.	A
OUT	4	OUT remains high. Power stage will be damaged. IC damage is possible.	A
GND	5	IC is not biased. OUT remains low. Converter has no output.	B
CS	6	OUT has minimum on time. IC damage is possible.	A
RT	7	OUT remains low. IC damage is possible.	A
SS	8	Soft start function is lost. IC damage is possible.	A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265