Functional Safety Information

# *ISO6763/ISO6763-Q1 Functional Safety FIT Rate, FMD and Pin FMA*

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# 1 Overview

This document contains information for ISO6763/ISO6763-Q1 (16-DW package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the functional block diagram of one channel of ISO6763/ISO6763-Q1 for reference.

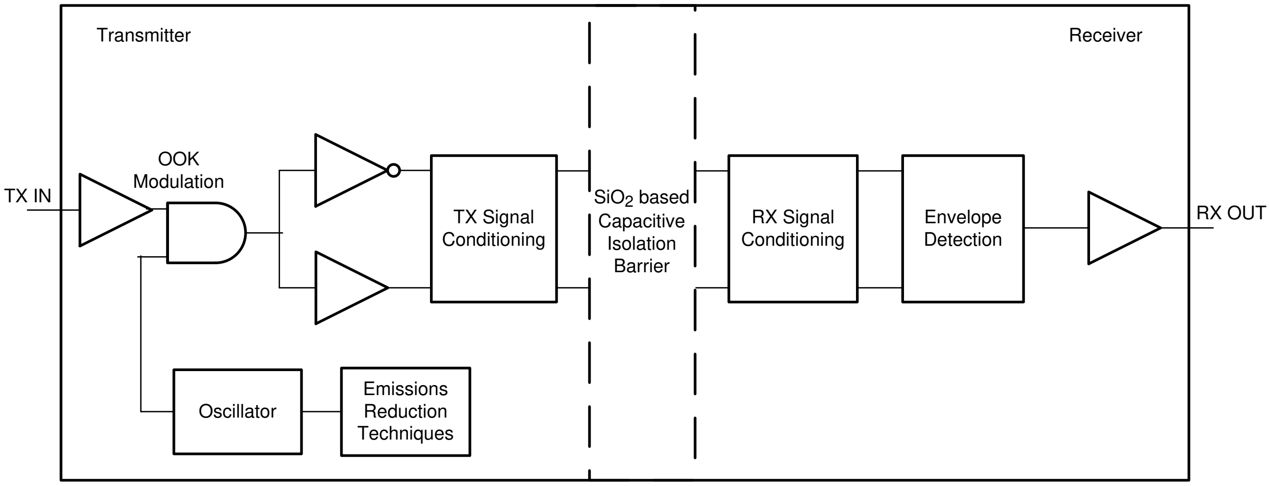

**Figure 1-1. Functional Block Diagram**

ISO6763/ISO6763-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

# 2 Functional Safety Failure In Time (FIT) Rates

## 2.1 16-SOIC (wide-body SOIC) Package

This section provides Functional Safety Failure In Time (FIT) rates for the 16-SOIC package of ISO6763/ ISO6763-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 28 |
| Die FIT Rate | 3 |
| Package FIT Rate | 25 |

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 196 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS, BICMOS<br>Digital, analog / mixed | 25 FIT | 55 °C |

The Reference FIT Rate and Reference Virtual $T_J$ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

## 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ISO6763/ISO6763-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| OUT state undetermined | 25% |
| OUT not in timing or voltage specification | 40% |
| OUT stuck to default state | 25% |
| OUT stuck high | 5% |
| OUT stuck low | 5% |

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the ISO6763/ISO6763-Q1 (16-DW package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (seeTable 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1. Note that when pin short to ground case is discussed, only same side ground shorts are considered.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality |
| B | No device damage, but loss of functionality |
| C | No device damage, but performance degradation |
| D | No device damage, no impact to functionality or performance |

## 4.1 16-QSOP (SSOP) and 16-DW (wide-body SOIC) Package

Figure 4-1 shows the ISO6763/ISO6763-Q1 pin diagram for 16-DW packages. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ISO6763/ISO6763-Q1 data sheet.

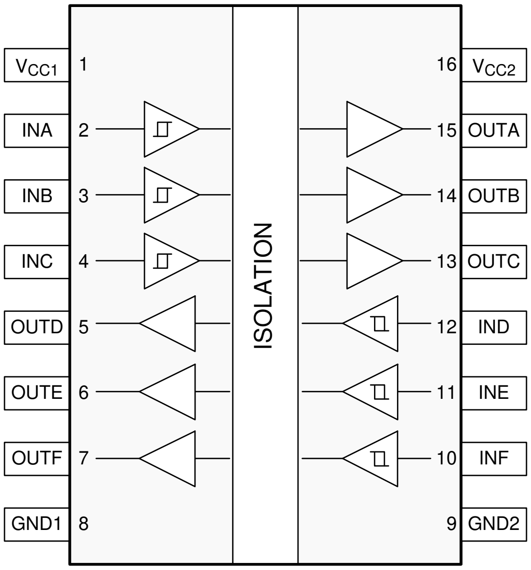

**Figure 4-1. Pin Diagram 16-DW Package**

### Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| $V_{CC1}$ | 1 | No power to the device on side-1. OUTA-OUTC go to default state, while OUTD-OUTF undetermined state. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage may be plausible. | A |
| INA | 2 | Input signal shorted to ground, so output (OUTA) stuck to low. Communication from INA to OUTA corrupted. | B |
| INB | 3 | Input signal shorted to ground, so output (OUTB) stuck to low. Communication from INB to OUTB corrupted. | B |
| INC | 4 | Input signal shorted to ground, so output (OUTC) stuck to low. Communication from INC to OUTC corrupted. | B |
| OUTD | 5 | OUTD stuck low. Data communication from IND to OUTD lost. Device damage possible if IND is driven high for extended period of time. | A |
| OUTE | 6 | OUTE stuck low. Data communication from INE to OUTE lost. Device damage possible if INE is driven high for extended period of time. | A |
| OUTF | 7 | OUTF stuck low. Data communication from INF to OUTF lost. Device damage possible if INF is driven high for extended period of time. | A |
| GND1 | 8 | Device continues to function as expected. Normal operation. | D |
| GND2 | 9 | Device continues to function as expected. Normal operation. | D |
| INF | 10 | Input signal shorted to ground, so output (OUTF) stuck to low. Communication from INF to OUTF corrupted. | B |
| INE | 11 | Input signal shorted to ground, so output (OUTE) stuck to low. Communication from INE to OUTE corrupted. | B |
| IND | 12 | Input signal shorted to ground, so output (OUTD) stuck to low. Communication from IND to OUTD corrupted. | B |
| OUTC | 13 | OUTC stuck low. Data communication from INC to OUTC lost. Device damage possible if INC is driven high for extended period of time. | A |
| OUTB | 14 | OUTB stuck low. Data communication from INB to OUTB lost. Device damage possible if INB is driven high for extended period of time. | A |
| OUTA | 15 | OUTA stuck low. Data communication from INA to OUTA lost. Device damage possible if INA is driven high for extended period of time. | A |
| $V_{CC2}$ | 16 | No power to the device on side-2. OUTA to OUTC pins state undetermined. OUTD-OUTF in default state. | B |

### Table 4-3. Pin FMA for Device Pins Open-Circuited

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| $V_{CC1}$ | 1 | Operation undetermined. Either device is unpowered and OUTA to OUTC=default logic state or through internal ESD diode on any IN pin, device can power up if any IN is driven to logic high. If IN has current sourcing capability to provide regular operating current of device, ESD diode conducts that current and device damage plausible. | A |
| INA | 2 | No communication to INA channel possible. OUTA stuck to default state (High for ISO6763-Q1 and Low for ISO6763F-Q1). | B |
| INB | 3 | No communication to INB channel possible. OUTB stuck to default state (High for ISO6763-Q1 and Low for ISO6763F-Q1). | B |
| INC | 4 | No communication to INC channel possible. OUTC stuck to default state (High for ISO6763-Q1 and Low for ISO6763F-Q1). | B |
| OUTD | 5 | State of OUTD undetermined. Data communication from IND to OUTD lost. | B |
| OUTE | 6 | State of OUTE undetermined. Data communication from INE to OUTE lost. | B |
| OUTF | 7 | State of OUTF undetermined. Data communication from INF to OUTF lost. | B |
| GND1 | 8 | Device unpowered on side1. OUTx on side2 go to default state. OUTx on side1 state undetermined. | B |
| GND2 | 9 | Device unpowered on side2. OUTx on side2 state undetermined. OUTx on side1 go to default state. | B |

**Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| INF | 10 | No communication to INF channel possible. OUTF stuck to default state (High for ISO6763-Q1 and Low for ISO6763F-Q1). | B |
| INE | 11 | No communication to INE channel possible. OUTE stuck to default state (High for ISO6763-Q1 and Low for ISO6763F-Q1). | B |
| IND | 12 | No communication to IND channel possible. OUTD stuck to default state (High for ISO6763-Q1 and Low for ISO6763F-Q1). | B |
| OUTC | 13 | State of OUTC undetermined. Data communication from INC to OUTC lost. | B |
| OUTB | 14 | State of OUTB undetermined. Data communication from INB to OUTB lost. | B |
| OUTA | 15 | State of OUTA undetermined. Data communication from INA to OUTA lost. | B |
| $V_{CC2}$ | 16 | Device unpowered on side-2 and state of OUTx on side-2 undetermined. OUTx on side-1 go to default state. | B |

### Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| $V_{CC1}$ | 1 | INA | Input signal shorted to supply, so output (OUTA) stuck to high. Communication from INA to OUTA corrupted. | B |
| INA | 2 | INB | Communication corrupted for either INA or INB channel. | B |
| INB | 3 | INC | Communication corrupted for either INC or INB channel. | B |
| INC | 4 | OUTD | Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage. | A |
| OUTD | 5 | OUTE | Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage. | A |
| OUTE | 6 | OUTF | Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage. | A |
| OUTF | 7 | GND1 | OUTF stuck low. Data communication from INF to OUTF lost. Device damage possible if INF is driven high for extended period of time. | A |
| GND1 | 8 | OUTF | Already considered in above row. | B |
| GND2 | 9 | INF | Input signal shorted to ground, so output (OUTF) stuck low. Communication from INF to OUTF corrupted. | B |
| INF | 10 | INE | Communication corrupted for either INE or INF channel. | B |
| INE | 11 | IND | Communication corrupted for either INE or IND channel. | B |
| IND | 12 | OUTC | Communication corrupted for either OUTD or OUTC channel. Device damage possible if INC and IND try to drive opposite logic state for extended duration creating a short between supply and ground on side-2. | A |
| OUTC | 13 | OUTB | Communication corrupted for either OUTC or OUTB channel. Device damage possible if INC and INB try to drive opposite logic state for extended duration creating a short between supply and ground on side-2. | A |
| OUTB | 14 | OUTA | Communication corrupted for either OUTA or OUTB channel. Device damage possible if INA and INB try to drive opposite logic state for extended duration creating a short between supply and ground on side-2. | A |
| OUTA | 15 | $V_{CC2}$ | OUTA stuck high. Data communication from INA to OUTA lost. Device damage possible if INA is driven low for extended period of time. | A |
| $V_{CC2}$ | 16 | OUTA | Already considered in above row. | A |

### Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| $V_{CC1}$ | 1 | No effect. Normal operation. | D |
| INA | 2 | INA pin stuck high. Communication corrupted. OUTA state high. | B |
| INB | 3 | INB pin stuck high. Communication corrupted. OUTB state high. | B |
| INC | 4 | INC pin stuck high. Communication corrupted. OUTC state high. | B |
| OUTD | 5 | OUTD stuck high. Communication disrupted. If IND is low for extended duration, OUTD being stuck high creates a short and can damage the device. | A |
| OUTE | 6 | OUTE stuck high. Communication disrupted. If INE is low for extended duration, OUTE being stuck high creates a short and can damage the device. | A |
| OUTF | 7 | OUTF stuck high. Communication disrupted. If INF is low for extended duration, OUTF being stuck high creates a short and can damage the device. | A |
| GND1 | 8 | Device unpowered on side1. OUTx on side-2 go to default state. OUTx on side-1 state undetermined. | B |
| GND2 | 9 | Device unpowered on side2. OUTx on side-2 state undetermined. OUTx on side-1 go to default state. | B |
| INF | 10 | INF pin stuck high. Communication corrupted. OUTF state high. | B |
| INE | 11 | INE pin stuck high. Communication corrupted. OUTE state high. | B |

### Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| IND | 12 | IND pin stuck high. Communication corrupted. OUTD state high. | B |
| OUTC | 13 | OUTC stuck high. Communication disrupted. If INC is low for extended duration, OUTC being stuck high creates a short and can damage the device. | A |
| OUTB | 14 | OUTB stuck high. Communication disrupted. If INB is low for extended duration, OUTB being stuck high creates a short and can damage the device. | A |
| OUTA | 15 | OUTA stuck high. Communication disrupted. If INA is low for extended duration, OUTA being stuck high creates a short and can damage the device. | A |
| $V_{CC2}$ | 16 | Device continues to function as expected. Normal operation. | D |

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