Functional Safety Information

LM749x0-Q1 and LM74910H-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for LM749x0-Q1 and LM74910H-Q1 to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

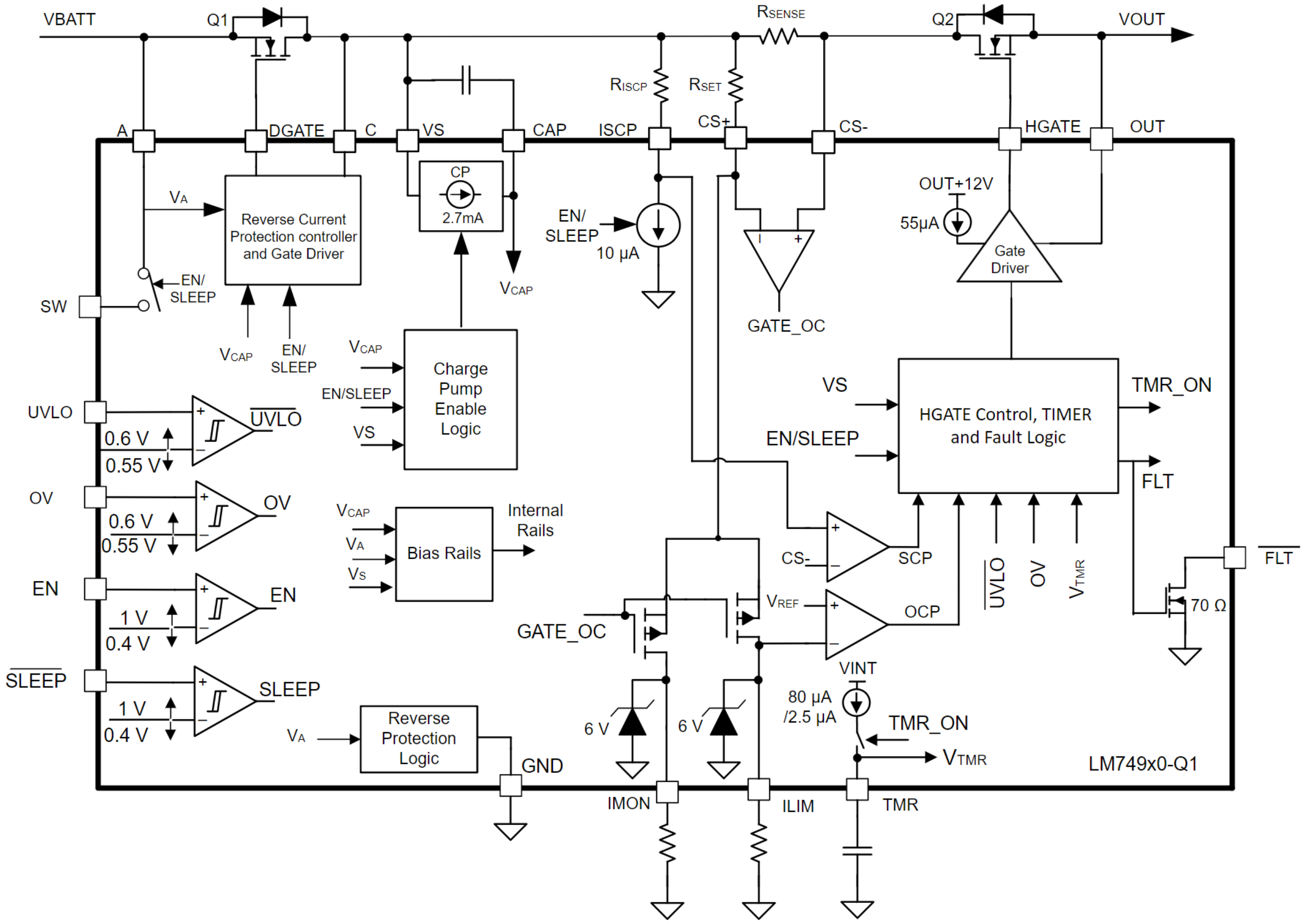

Figure 1-1. Functional Block Diagram

LM749x0-Q1 and LM74910H-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM749x0-Q1 and LM74910H-Q1 (LM74900-Q1, LM74910-Q1, and LM74910H-Q1) based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	14
Die FIT rate	3
Package FIT rate	11

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 42mW
- Climate type: World-wide from table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS logic	25	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM749x0-Q1 and LM74910H-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
DGATE stuck at low	20
DGATE voltage or timing not in specification	20
HGATE stuck at low	25
HGATE voltage or timing not in specification	25
OUT voltage or timing not in specification	5
Pin-to-pin short	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of LM74900-Q1, LM74910-Q1, and LM74910H-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM749x0-Q1 and LM74910H-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM749x0-Q1 and LM74910H-Q1 datasheets.

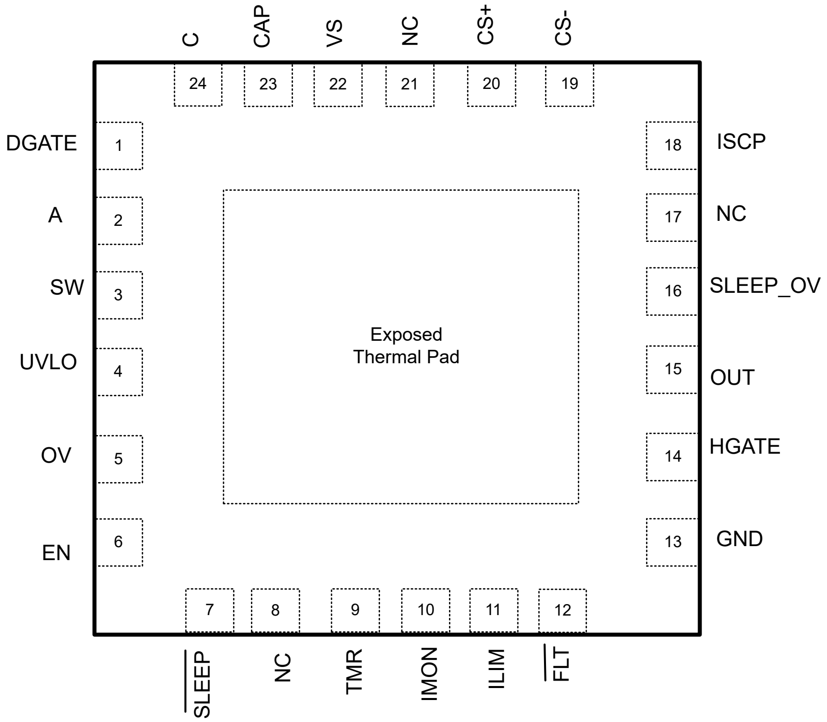

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is operating under the specified ranges within the *Recommended Operating Conditions* section of the data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DGATE	1	The device is damaged due to internal conduction. The external DGATE FET can also be damaged due to a violation of the maximum VGS rating.	A
A	2	The input supply is shorted to ground. The device not functional.	B
SW	3	The device is damaged if enabled.	A
UVLO	4	The HGATE drive of the device is off.	B
OV	5	Overvoltage protection functionality is disabled.	B
EN	6	The device is in shutdown mode.	B
$\overline{\text{SLEEP}}$	7	The device is in SLEEP mode.	B
NC	8	No effect on device operation.	D
	17		
	21		
TMR	9	Timer functionality is not be available.	B
IMON	10	The current monitoring output is not available.	B
ILIM	11	Overcurrent protection with circuit breaker feature is not be available.	B
$\overline{\text{FLT}}$	12	Fault indication functionality is not available.	B
GND	13	No impact on device functionality.	D
HGATE	14	The device is damaged.	A
OUT	15	The external FET VGS (maximum) rating can be exceeded and damage the external FET. The device can experience an increase in quiescent current.	D
SLEEP_OV	16	Overvoltage protection during SLEEP mode is not available.	B
ISCP	18	Device damage is expected due to internal current flow.	A
CS-	19	Device damage is expected due to internal current flow.	A
CS+	20	Device damage is expected due to internal current flow.	A
VS	22	The device does not power up.	B
CAP	23	The device is damaged due to internal conduction between VS and CAP.	A
C	24	Linear regulation and reverse current blocking functionality is not available. The quiescent current of the device can increase.	B
RTN	—	The input reverse polarity protection feature is not available.	B

Table 4-3. Pin FMA for Device Pins Open Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DGATE	1	The diode FET cannot be controlled. The reverse current blocking feature is not available. Load current flows through the body diode of the FET.	B
A	2	The diode FET is turned off due to a linear regulation sink current. Load current flows through the body diode of the FET.	B
SW	3	The battery voltage monitoring feature is not available.	B
UVLO	4	The HGATE drive of the device is off due to internal pulldown on the UVLO pin.	B
OV	5	Overvoltage protection functionality is disabled as the OV pin is internally pulled low.	B
EN	6	The device is in shutdown mode as the EN pin is internally pulled low.	B
$\overline{\text{SLEEP}}$	7	The SLEEP mode feature is not available.	B
NC	8	No effect on device operation.	D
	17		
	21		
TMR	9	The operation of the device is a default timer operation. The automatic retry timer cannot be set using an external timer capacitor.	B
IMON	10	The current monitoring output is not available.	B
ILIM	11	The ILIM pin is pulled high and the device is in overcurrent protection mode.	B
$\overline{\text{FLT}}$	12	Fault indication functionality is not available.	B
GND	13	The device does not power up.	D
HGATE	14	HGATE control to turn the external FET on or off is not available.	B
OUT	15	HGATE control to turn the external FET on or off is not available.	D
SLEEP_OV	16	Overvoltage protection during SLEEP mode is not available.	B
ISCP	18	The short circuit protection feature is not available.	B
CS-	19	The device is in overcurrent protection mode and the HGATE drive is turned off.	B
CS+	20	Overcurrent protection and the current monitoring output is not available.	B
VS	22	The device does not power up.	B
CAP	23	The charge pump does not build up and the DGATE and HGATE drives are disabled.	B
C	24	The DGATE drive remains off.	B
RTN	—	No effect on device operation.	D

Table 4-4. Pin FMA for Device Pins Short Circuited to Adjacent Pin

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DGATE	1	The diode FET is off. Load current flows through the body diode of the FET.	B
A	2	No effect on device operation.	D
SW	3	The UVLO feature is not available.	B
UVLO	4	The OV or UVLO comparator trigger and HGATE is off.	B
OV	5	The HGATE drive is off in case the device is enabled (EN = High).	B
EN	6	No effect on device operation.	D
$\overline{\text{SLEEP}}$	7	No effect on device operation.	D
NC	8	No effect on device operation.	D
	17		
	21		
TMR	9	Timer (TMR) and current monitoring (IMON) functionality are out of data sheet specification.	B
IMON	10	The current monitoring output is out of data sheet specification.	B
ILIM	11	The device is in overcurrent protection mode based on the $\overline{\text{FLT}}$ voltage level.	B
$\overline{\text{FLT}}$	12	No effect on device operation.	D
GND	13	GND is shorted to HGATE and can cause device damage.	A
HGATE	14	The HGATE FET is off as the HGATE is shorted to OUT causing a VGS short condition.	B
OUT	15	No effect on device operation. The device only supports overvoltage clamp operation during SLEEP mode.	B
SLEEP_OV	16	No effect on device operation.	B
ISCP	18	No effect on device operation.	D
CS-	19	Short circuit and overcurrent protection is not available.	B
CS+	20	Overcurrent limit; current monitoring output parameters are out of specification.	B
VS	22	The charge pump of the device does not come up. The DGATE and HGATE drives are off.	B
CAP	23	The charge pump of the device does not come up. The DGATE and HGATE drives are off.	B
C	24	No effect on device operation.	B
RTN	—	No effect on device operation.	D

Table 4-5. Pin FMA for Device Pins Short Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DGATE	1	The DGATE is shorted to supply. The diode FET remains off.	B
A	2	No effect on device operation.	D
SW	3	The battery voltage monitoring feature is available irrespective of the status of the EN pin.	B
UVLO	4	UVLO functionality is not available.	B
OV	5	The HGATE is turned off due to the OV comparator input going high.	B
EN	6	The device is always on as the EN is pulled to supply.	B
$\overline{\text{SLEEP}}$	7	The SLEEP mode feature is not available.	B
NC	8	No effect on device operation.	D
	17		
	21		
TMR	9	The device is damaged if the supply voltage level >5.5V.	A
IMON	10	The device is damaged if the supply voltage level >5.5V.	A
ILIM	11	The device is damaged if the supply voltage level >5.5V.	A
$\overline{\text{FLT}}$	12	Fault indication functionality is not available.	B
GND	13	The device does not power up due to supply being shorted to GND.	D
HGATE	14	The HGATE control to turn the external FET on or off is not available. The quiescent current of the device can increase.	B
OUT	15	Supply is shorted to output. The diode (DGATE) and load disconnect (HGATE) features are not functional as the supply is shorted to output.	B
SLEEP_OV	16	The device is only able to provide overvoltage cut-off functionality during SLEEP mode.	B
ISCP	18	The device has a default short circuit protection threshold of 20mV.	B
CS-	19	Overcurrent protection functionality is not available.	B
CS+	20	The device is in overcurrent protection mode.	B
VS	22	No effect on device operation.	B
CAP	23	The charge pump does not build up and the DGATE and HGATE drives are disabled.	B
C	24	Diode functionality is not available (reverse current blocking).	B
RTN	—	No effect on device operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 27, 2024 to March 30, 2026 (from Revision * (February 2024) to Revision A (March 2026))	**Page**
• Added the LM74910H-Q1 GPN	2
• Removed advanced information note	2
• Updated for production data	2

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Last updated 10/2025