Functional Safety Information

LM5171-Q1, LM5171
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the LM5171-Q1 and LM5171 (PHP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Functional Block Diagram shows the device functional block diagram for reference.

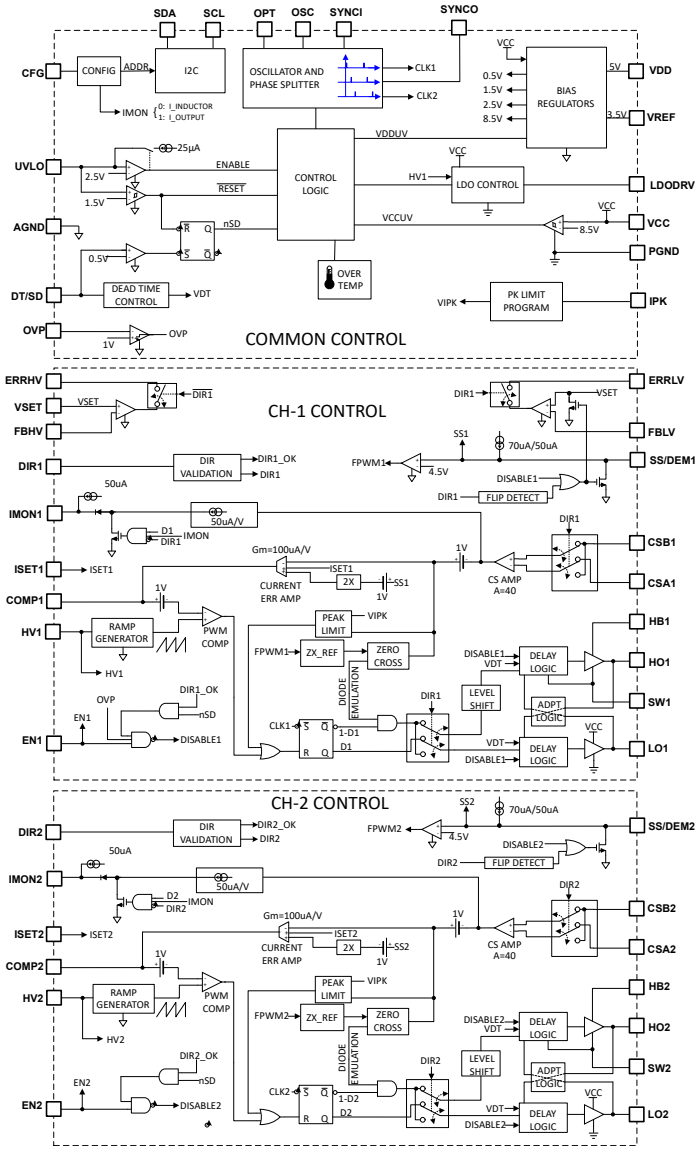

Figure 1-1. Functional Block Diagram

The LM5171-Q1, LM5171 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LM5171-Q1 and LM5171 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	34
Die FIT rate	3
Package FIT rate	31

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 800 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog and Mixed HV >50V supply	30	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM5171-Q1 and LM5171 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
HO or LO gate driver stuck on	10
HO or LO gate driver stuck off	20
HO or LO gate driver open (high-Z)	5
VOUT voltage not in specification	55
LDODRV stuck low and External clock synchronization not functioning	5
IMON is inaccurate	5

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM5171-Q1 and LM5171. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Pin FMA for Device Pins Short-Circuited to Ground)
- Pin open-circuited (see Pin FMA for Device Pins Open-Circuited)
- Pin short-circuited to an adjacent pin (see Pin FMA for Device Pins Short-Circuited to Adjacent Pin)

Table 4-2 through Table 4-3 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Pin Diagram shows the LM5171-Q1/LM5171 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM5171-Q1/LM5171 data sheet.

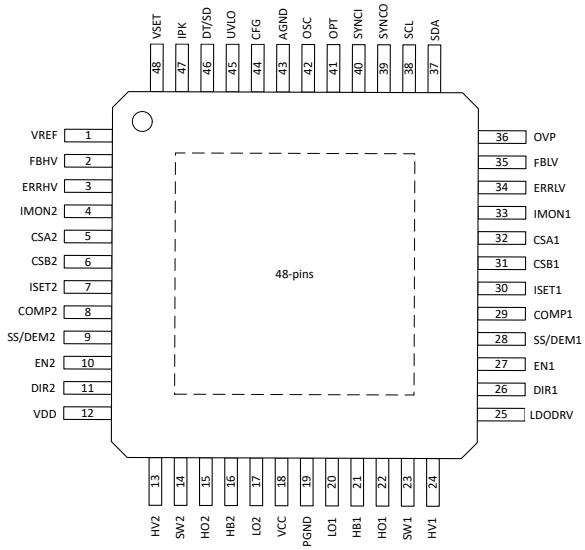

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the *Recommended Operation Conditions* and the *Absolute Maximum Ratings* found in the LM5171-Q1 or LM5171 data sheet.
- For the analysis, the typical application as shown in the *Typical Application* section of the LM5171-Q1 or LM5171 is used.
- $V_{supply} = V_{cc} = 10$ V
- $V_{OUT} = 12$ V

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin No	Pin Name	Description of Potential Failure Effect (s)	Failure Effect Class
1	VREF	No switching	B
2	FBLV	No switching	B
3	ERRLV	No switching	B

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin No	Pin Name	Description of Potential Failure Effect (s)	Failure Effect Class
4	IMON2	Normal operation, but loss of CH-2 current monitor	D
5	CSA2	Invalid current sense, and 12V Rail is shorted to GND	B
6	CSB2	Invalid current sense, and 12V Rail is shorted to GND	B
7	ISET2	Loss of current setting command in CH-2	B
8	COMP2	No switching in CH-2	B
9	SS/DEM2	No switching in CH-2	B
10	EN2	No switching in CH-2	B
11	DIR2	CH-2 can only operate in Boost Mode, no Buck Mode possible	C
12	VDD	Unable to startup	B
13	HV2	CH-2 Unable to Startup	B
14	HB2	No CH-2 high-side boot voltage; not able to run CH-2 in buck mode	B
15	HO2	CH-2 high side driver may be damaged	B
16	SW2	Switch Node of CH-2 grounded	B
17	LO2	Overloading of the CH-2 low side driver	B
18	PGND	Normal operation	D
19	VCC	Loss of VCC bias supply. Unable to start up	B
20	LO1	Overloading of the CH-1 low side driver	B
21	SW1	Switch Node of CH-1 grounded	B
22	HO1	CH-1 high side driver may be damaged	B
23	HB1	No CH-1 high-side boot voltage; not able to run CH-1 in buck mode	B
24	HV1	CH-1 Unable to Startup	B
25	LDODRV	Normal operation, but VCC pin must be supplied externally	D
26	DIR1	CH-1 can only operate in Boost Mode, no Buck Mode possible	C
27	EN1	No switching in CH-1	B
28	SS/DEM1	No switching in CH-1	B
29	COMP1	No switching in CH-1	B
30	ISET1	Loss of current setting command in CH-1	B
31	CSB1	Invalid current sense, and 12V Rail is shorted to GND	B
32	CSA1	Invalid current sense, and 12V Rail is shorted to GND	B
33	IMON1	Normal operation, but loss of CH-1 current monitor	D
34	EERHV	No switching	B
35	FBHV	No switching	B
36	OVP	Normal operation. Loss of 48V OVP in CH-1 or both channels in parallel operation	D
37	SDA	Normal operation but no I2C communication	D
38	SCL	Normal operation but no I2C communication	D
39	SYNCO	Normal operation, loss of synchronization for responder phases	D
40	SYNCI	Normal operation, loss of synchronization	D
41	OPT	Normal operation, loss of synchronization	D
42	OSC	Clock frequency is higher, unpredictable switching behavior	B

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin No	Pin Name	Description of Potential Failure Effect (s)	Failure Effect Class
43	AGND	Normal operation	D
44	CFG	Normal operation, but current monitor only possible for Boost mode for single I2C address	D
45	UVLO	Unable to startup	B
46	DT/SD	Unable to startup	B
47	IPK	No switching	B
48	VSET	No switching	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin No	Pin Name	Description of Potential Failure Effect (s)	Failure Effect Class
1	VREF	No switching	B
2	FBLV	No switching	B
3	ERRLV	No switching	B
4	IMON2	Normal operation, but loss of CH-2 current monitor	D
5	CSA2	Loss of CH-2 current regulation	B
6	CSB2	Loss of CH-2 current regulation	B
7	ISET2	Loss of current setting command in CH-2	B
8	COMP2	Loss of CH-2 loop compensation and loss of loop stability	B
9	SS/DEM2	No soft-start or DEM mode operation in CH-2	B
10	EN2	No switching in CH-2	B
11	DIR2	Invalid DIR command and no switching in CH-2	B
12	VDD	Normal operation can not be ensured	B
13	HV2	CH-2 Unable to startup	B
14	HB2	Loss of CH-2 Buck Mode Operation	C
15	HO2	Loss of CH-2 Buck Mode Operation	C
16	SW2	Loss of CH-2 Buck Mode Operation	C
17	LO2	Loss of CH-2 Buck Mode Operation	C
18	PGND	No switching	B
19	VCC	No switching	B
20	LO1	Loss of CH-1 Boost Mode Operation	C
21	SW1	Loss of CH-1 Boost Mode Operation	C
22	HO1	Loss of CH-1 Boost Mode Operation	C
23	HB1	Loss of CH-1 Boost Mode Operation	C
24	HV1	CH-1 Unable to Startup	B
25	LDODRV	Normal operation, but VCC pin must be supplied externally	D
26	DIR1	Invalid DIR command and no switching in CH-1	B
27	EN1	No CH-1 switching	B
28	SS/DEM1	No soft-start or DEM mode operation in CH-1	B
29	COMP1	Loss of CH-1 loop compensation and loss of loop stability	B
30	ISET1	Loss of current setting command in CH-1	B

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Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin No	Pin Name	Description of Potential Failure Effect (s)	Failure Effect Class
31	CSB1	Loss of CH-1 current regulation	B
32	CSA1	Loss of CH-1 current regulation	B
33	IMON1	Normal operation, but loss of CH-1 current monitor	D
34	EERHV	No switching	B
35	FBHV	No switching	B
36	OVP	Normal operation. Loss of 48V OVP in CH-1 or both channels in parallel operation	D
37	SDA	Normal operation but no I2C communication	D
38	SCL	Normal operation but no I2C communication	D
39	SYNCO	Normal operation, loss of synchronization	D
40	SYNCI	Normal operation, loss of synchronization	D
41	OPT	Normal operation, in 120 degree interleaving	D
42	OSC	Loss of clock function, No switching	B
43	AGND	Loss of analog reference ground. No switching	B
44	CFG	Normal operation, but loss of current monitor and I2C Interface	D
45	UVLO	Unable to startup	B
46	DT/SD	Normal switching with built-in adaptive dead time scheme	D
47	IPK	No switching	B
48	VSET	No switching	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin No	Pin Name	Description of Potential Failure Effect (s)	Failure Effect Class
1	VREF	Loss of loop control and no switching activity in Buck Mode	C
2	FBLV	Loss of loop control and no switching activity in Buck Mode	C
3	ERRLV	Loss of loop control and no switching activity in Buck Mode	C
4	IMON2	Pin voltage rating is exceeded and may cause pin damage when shorted to 12V rail	B
5	CSA2	Loss of current sense and loss of CH-2 current regulation	B
6	CSB2	Loss of current sense and loss of CH-2 current regulation	B
7	ISET2	Loss of current setting command, Pin voltage rating is exceeded and may cause pin damage when shorted to CSB2	B
8	COMP2	Loop compensation may be altered by SS capacitor and causing instable operation	B
9	SS/DEM2	Normal operation without soft-start or DEM mode operation in CH-1	D
10	EN2	Normal operation in Buck Mode, no Boost Mode in CH-2	C
11	DIR2	Normal operation in Buck Mode, no Boost Mode in CH-2	C
12	VDD	Normal operation in Buck Mode, no Boost Mode in CH-2	C
13	HV2	No switching in CH-2	B
14	HB2	Pin voltage rating is exceeded and may cause pin damage when shorted to HV2	B
15	HO2	Pin voltage rating is exceeded and may cause pin damage when shorted to SW2	B
16	SW2	No switching in CH-2	B
17	LO2	Pin voltage rating is exceeded and may cause pin damage when shorted to HV2	B

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin No	Pin Name	Description of Potential Failure Effect (s)	Failure Effect Class
18	PGND	No switching on LO2 when LO2 is shorted to ground rail. Unable to startup when VCC rail is shorted to ground rail	B
19	VCC	Unable to startup when VCC rail is shorted to ground rail. No switching on LO1 when LO1 is shorted to VCC rail	B
20	LO1	Pin voltage rating is exceeded and may cause pin damage when shorted to SW1	B
21	SW1	No switching in CH-1	B
22	HO1	Pin voltage rating is exceeded and may cause pin damage when shorted to SW1	B
23	HB1	Pin voltage rating is exceeded and may cause pin damage when shorted to HV1	B
24	HV1	No switching in CH-1	B
25	LDODRV	Normal operation	D
26	DIR1	Normal operation in Buck Mode, no Boost Mode in CH-1 when shorted to EN1, Pin voltage rating is exceeded and may cause pin damage when shorted to LDODRV	C
27	EN1	Normal operation in Buck Mode, no Boost Mode in CH-1	C
28	SS/DEM1	Normal operation without soft-start or DEM mode operation in CH-1	D
29	COMP1	Loop compensation may be altered by SS capacitor and causing instable operation	B
30	ISET1	Loss of current setting command, Pin voltage rating is exceeded and may cause pin damage when shorted to CSB1	B
31	CSB1	Loss of current sense and loss of CH-1 current regulation	B
32	CSA1	Loss of current sense and loss of CH-1 current regulation	B
33	IMON1	Normal operation with loss of CH-1 current monitor, Pin voltage rating is exceeded and may cause pin damage when shorted to CSA1	D
34	EERHV	Loss of loop control and no switching activity in Boost Mode	C
35	FBHV	Loss of loop control and no switching activity in Boost Mode	C
36	OVP	Normal operation. Loss of 48V OVP in CH-1 or both channels in parallel operation	D
37	SDA	Normal operation but no I2C communication	D
38	SCL	Normal operation but no I2C communication	D
39	SYNCO	Normal operation, loss of synchronization	D
40	SYNCI	Normal operation, loss of synchronization	D
41	OPT	Unreliable clock interleaving may affect operation	B
42	OSC	Unpredictable clock function, unpredictable switching behavior	B
43	AGND	Unpredictable clock function, unpredictable switching behavior	B
44	CFG	Normal operation, but current monitor function not available	D
45	UVLO	Normal operation with unpredictable DT setting when shorted to DT/SD pin	D
46	DT/SD	Normal operation with unpredictable DT setting when shorted to DT/SD pin	D
47	IPK	Unreliable peak current setting and unpredictable switching behavior	B
48	VSET	Unpredictable switching behavior	B

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