Functional Safety Information

TPS1213-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for TPS1213-Q1 (VSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

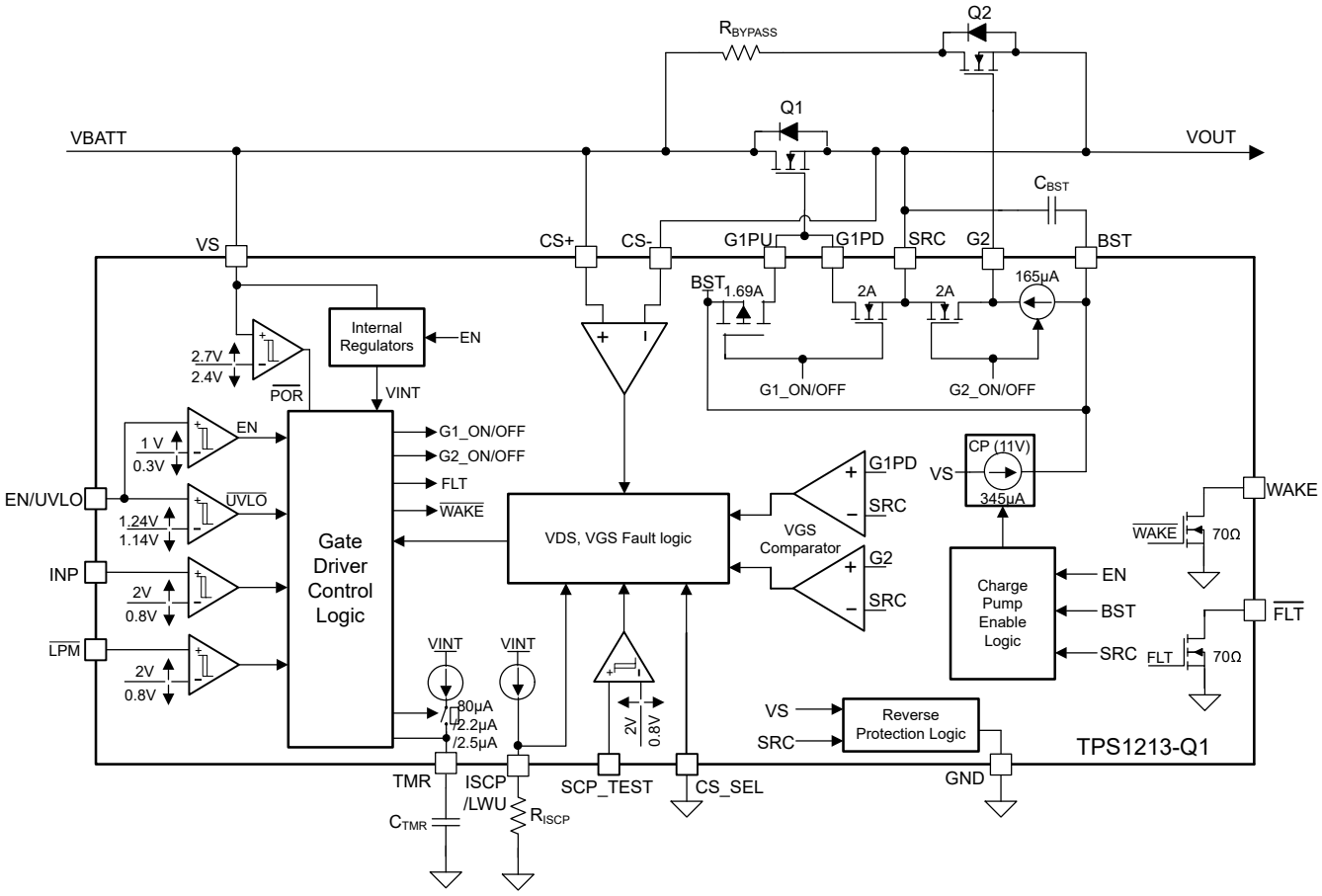

Figure 1-1. Functional Block Diagram

TPS1213-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS1213-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	3
Package FIT rate	6

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 0.6mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS1213-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Gate output stuck high	10
Gate output stuck low	45
Gate output functional, not in specification voltage or timing	34
Short circuit protection fails to trip or false trip	5
UVLO fails to trip or false trip	1
Pin-to-pin short any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS1213-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS1213-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS1213-Q1 data sheet.

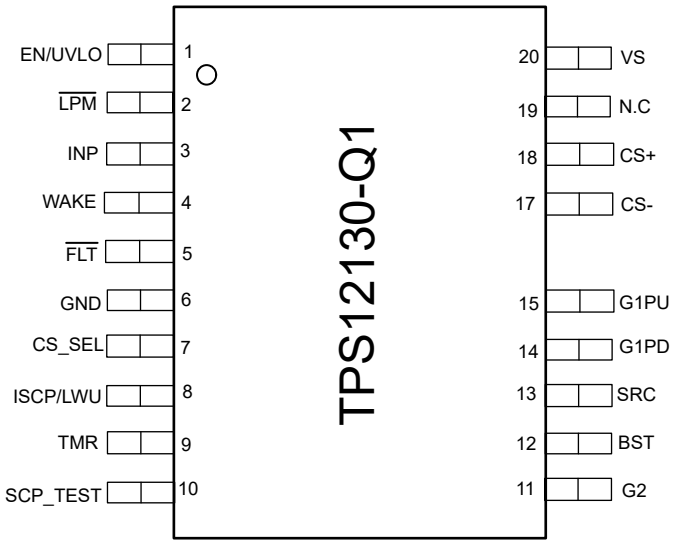

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The data sheet recommendations for operating conditions, external component selection, and PCB layout are followed.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/UVLO	1	Normal operation. The device is disabled.	B
$\overline{\text{LPM}}$	2	Normal operation. The devices operates in low-power mode.	B
INP	3	Normal operation. The G1PD output is low and the external FET is off.	B
WAKE	4	WAKE event cannot be reported.	B
$\overline{\text{FLT}}$	5	Overcurrent, UVLO, charge pump UVLO fault diagnostic cannot be reported.	B
GND	6	Normal operation.	D
CS_SEL	7	Normal operation.	D
ISCP/LWU	8	Load wakeup and SCP threshold sets to minimum threshold.	B
TMR	9	Overcurrent does not get detected, hence overcurrent protection gets disabled.	B
SCP_TEST	10	Normal operation.	B
G2	11	With G2 grounded, if the pin voltage between SRC and G exceeds the data sheet range for the pin, the exceedance can cause device damage due to voltage breakdown on the ESD circuit.	A
BST	12	Gate driver supply does not come up. FETs remain OFF.	B
SRC	13	Short to GND protection starts.	B
G1PD	14	With G1PD grounded, if the pin voltage between SRC and PD exceeds the data sheet range for the pin, the exceedance can cause device damage due to voltage breakdown on the ESD circuit.	A
G1PU	15	Gate driver supply gets short circuited. FETs remain OFF.	B
CS-	17	Short to GND protection starts.	B
CS+	18	With CS+ grounded, if the pin voltage between CS+ and CS– exceeds the data sheet range for the pin, the exceedance can cause device damage due to voltage breakdown on the ESD circuit.	A
N.C	19	Normal operation.	D
VS	20	Device supply grounded. Device does not power up.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/UVLO	1	Internal pulldown brings EN/UVLO to low, disabling the device.	B
$\overline{\text{LPM}}$	2	Internal pulldown brings $\overline{\text{LPM}}$ to low, and the device can operate in low-power mode.	B
INP	3	Internal pulldown brings INP to low, pulling G1PD output low.	B
WAKE	4	WAKE event cannot be reported.	B
$\overline{\text{FLT}}$	5	Overcurrent, UVLO, charge pump UVLO fault diagnostic cannot be reported.	B
GND	6	Device does not power up and is disabled.	B
CS_SEL	7	Internal pulldown brings CS_SEL to low, resulting in normal operation.	D
ISCP/LWU	8	Load wakeup and SCP threshold sets to maximum threshold.	B
TMR	9	Overcurrent response time and auto-retry duration gets reduced to device minimum setting.	C
SCP_TEST	10	Internal pulldown brings SCP_TEST to low, resulting in normal operation.	B
G2	11	G2 output is not get controlled.	B
BST	12	External FET can turn ON and OFF repetitively due to no capacitor connection at the BST pin.	B
SRC	13	The external FET is not turned OFF as the FET source is disconnected from the internal pulldown driver.	B
G1PD	14	The external FET does not turn OFF, as the FET GATE disconnects from the internal pulldown driver.	B
G1PU	15	The external FET does not turn OFF, as the FET GATE disconnects from the internal pulldown driver.	B
CS-	17	CS- gets internally clamped to CS+ minus two diode drops. If ISCP/LWU feature is used, the external FET not turning ON is possible due to false overcurrent detection.	B
CS+	18	ISCP/LWU feature does not work.	B
N.C	19	Normal operation.	D
VS	20	Device does not get powered up and is disabled.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
EN/UVLO	1	2 ($\overline{\text{LPM}}$)	If EN/UVLO is driven high then $\overline{\text{LPM}}$ is detected high making the device function in active mode.	B
$\overline{\text{LPM}}$	2	3 (INP)	If $\overline{\text{LPM}}$ is driven high then INP is detected high making the device function in active mode.	B
INP	3	4 (WAKE)	If device is in active state then FET turns OFF as WAKE is low in active mode	B
WAKE	4	5 ($\overline{\text{FLT}}$)	WAKE and $\overline{\text{FLT}}$ are ORed together.	B
$\overline{\text{FLT}}$	5	6 (GND)	Fault events are not indicated.	B
GND	6	7 (CS_SEL)	Normal operation.	D
CS_SEL	7	8 (ISCP/LWU)	With CS_SEL grounded, load wakeup and SCP threshold sets to minimum threshold.	C
ISCP/LWU	8	9 (TMR)	TMR and ISCP/LWU thresholds are affected. External FET shuts off at a different threshold than set by ISCP/LWU. During an overcurrent fault the device is in latch-off mode if ISCP/LWU has a < 100kΩ resistor.	C
TMR	9	10 (SCP_TEST)	SCP_TEST feature gets disabled.	B
G2	11	12 (BST)	When $\overline{\text{LPM}}$ is driven low, BST (gate driver supply) gets loaded through the internal G2 pulldown switch. Gate driver UVLO hits resulting in turning off the external FETs.	B
BST	12	13 (SRC)	Gate drive supply gets shorted and external FETs do not turn ON.	B
SRC	13	14 (G1PD)	Shorting of the pulldown switch (between G1PD and SRC) of the internal gate driver. External FET remains OFF.	B
G1PD	14	15 (G1PU)	Turn ON and OFF speeds of the external FETs can get impacted.	C
CS-	17	18 (CS+)	Bypasses the external current sense resistor or FET VDS sensing based on application circuit. SCP features get disabled.	B
CS+	18	19 (N.C)	Normal operation.	D
N.C	19	20 (VS)	Normal operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/UVLO	1	EN/UVLO pin is supply rated. Device remains enabled.	B
$\overline{\text{LPM}}$	2	$\overline{\text{LPM}}$ pin is supply rated. Device operates in active mode depending on supply voltage level.	B
INP	3	INP pin is supply rated and is treated driven high.	B
WAKE	4	If pin voltage exceeds the data sheet range for the pin, the exceedance can cause device damage due to voltage breakdown on the ESD circuit.	A
$\overline{\text{FLT}}$	5	If pin voltage exceeds the data sheet range for the pin, the exceedance can cause device damage due to voltage breakdown on the ESD circuit.	A
GND	6	Supply power is bypassed and device does not turn on.	B
CS_SEL	7	CS_SEL pin is supply rated. If pin voltage exceeds the data sheet range for the pin, the exceedance can cause device damage due to voltage breakdown on the ESD circuit.	B
ISCP/LWU	8	If pin voltage exceeds the data sheet range for the pin, the exceedance can cause device damage due to voltage breakdown on the ESD circuit.	A
TMR	9	If pin voltage exceeds the data sheet range for the pin, the exceedance can cause device damage due to voltage breakdown on the ESD circuit.	A
SCP_TEST	10	If pin voltage exceeds the data sheet range for the pin, the exceedance can cause device damage due to voltage breakdown on the ESD circuit.	A
G2	11	If pin voltage exceeds the data sheet range for the pin, the exceedance can cause device damage due to voltage breakdown on the ESD circuit.	A
BST	12	If pin voltage exceeds the data sheet range for the pin, the exceedance can cause device damage due to voltage breakdown on the ESD circuit.	A
SRC	13	Output stuck on to supply.	B
G1PD	14	If pin voltage exceeds the data sheet range for the pin, the exceedance can cause device damage due to voltage breakdown on the ESD circuit.	A
G1PU	15	If pin voltage exceeds the data sheet range for the pin, the exceedance can cause device damage due to voltage breakdown on the ESD circuit.	A
CS-	17	In the application, the external sense resistor or FET VDS sensing gets bypassed. Short circuit protection does not work.	A
CS+	18	No effect. Normal operation.	D
N.C	19	No effect. Normal operation.	D
VS	20	No effect. Normal operation.	D

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265