Functional Safety Information

DAC539G2-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the DAC539G2-Q1 (RTE package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

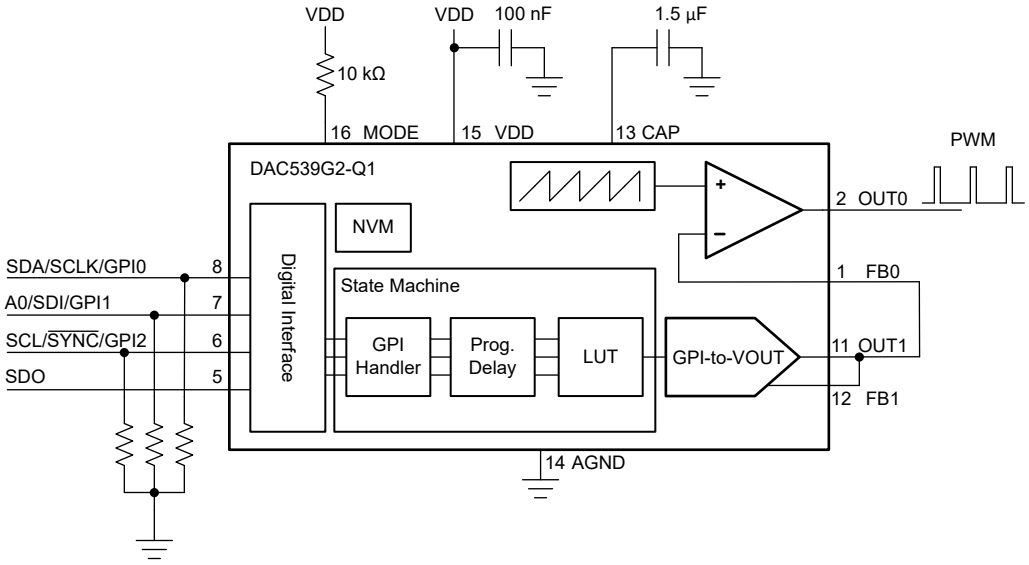

Figure 1-1. Functional Block Diagram

The DAC539G2-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the DAC539G2-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	8
Die FIT rate	2
Package FIT rate	6

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 8.25 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the DAC539G2-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or over stress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Digital core - digital interface (communication loss)	25
Digital core - state machine (LUT malfunction)	17
NVM retention loss	13
Voltage to PWM frequency error	5
Voltage to PWM duty cycle error	20
Total unadjusted error (TUE) at output of GPI-to-VOUT	20

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the DAC539G2-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuit to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the DAC539G2-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the DAC539G2-Q1 data sheet.

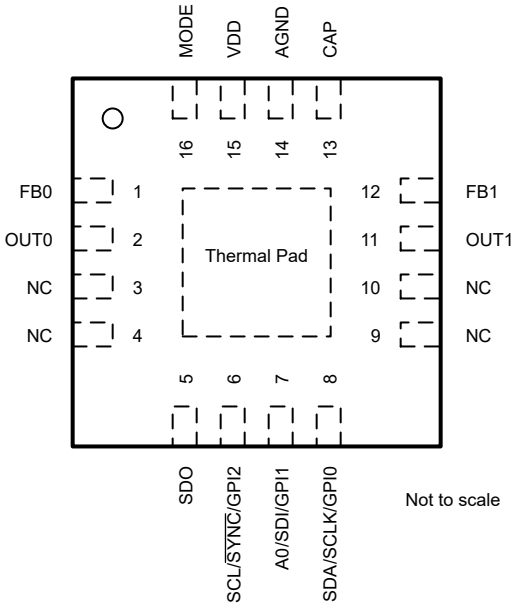

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- All the pin FMA analysis are described based on the Figure 1-1 functional block diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB0	1	OUT0 (PWM) is always high	B
OUT0	2	OUT0 is be stuck at zero if OUT0 is configured as open drain	B
		Device can be damaged over a period of time if OUT0 is configured in push-pull mode	A
NC	3	No change in functionality or performance	D
NC	4	No change in functionality or performance	D
SDO	5	Read back data is corrupted	B
SCL/$\overline{\text{SYNC}}$/GPI2	6	Loss of communication with the device	B
A0/SDI/GPI1	7	Loss of communication with the device	B
SDA/SCLK/GPI0	8	Loss of communication with the device	B
NC	9	No change in functionality or performance	D
NC	10	No change in functionality or performance	D
OUT1	11	OUT0 (PWM) is always high, resulting in incorrect PWM duty cycle	B
FB1	12	OUT0 (PWM) is always high, resulting in incorrect PWM duty cycle	B
CAP	13	Loss of functionality, device enters short circuit protection, power consumption increases	B
AGND	14	No change in functionality or performance	D
VDD	15	Complete loss of functionality, no device damage	B
MODE	16	Loss of GPI functionality	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB0	1	OUT0 (PWM) results in incorrect duty cycle	B
OUT0	2	OUT0 output value is not available	B
NC	3	No change in functionality or performance	D
NC	4	No change in functionality or performance	D
SDO	5	Read back data is not available	B
SCL/$\overline{\text{SYNC}}$/GPI2	6	Loss of communication with the device	B
A0/SDI/GPI1	7	Loss of communication with the device	B
SDA/SCLK/GPI0	8	Loss of communication with the device	B
NC	9	No change in functionality or performance	D
NC	10	No change in functionality or performance	D
OUT1	11	OUT0 (PWM) will result in incorrect duty cycle	B
FB1	12	OUT0 (PWM) will result in incorrect duty cycle	B
CAP	13	Open-circuited pin can cause damage to the low-voltage digital core and NVM supplied by the internal LDO	A
AGND	14	Complete loss of functionality, no device damage	B
VDD	15	Complete loss of functionality, no device damage	B
MODE	16	Loss of communication and GPI functionality	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
FB0	1	MODE	Short to corner pin is not expected	D
		OUT0	OUT0 (PWM) results in incorrect duty cycle	B
OUT0	2	FB0	OUT0 (PWM) results in incorrect duty cycle	B
		NC	No change in functionality or performance	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
NC	3	OUT0	No change in functionality or performance	D
		NC	No change in functionality or performance	D
NC	4	NC	No change in functionality or performance	D
		SDO	Short to corner pin is not expected	D
SDO	5	NC	Short to corner pin is not expected	D
		SCL/$\overline{\text{SYNC}}$/GPI2	Loss of communication,GPI and SDO functionality	B
SCL/$\overline{\text{SYNC}}$/GPI2	6	SDO	Loss of communication, GPI and SDO functionality	B
		A0/SDI/GPI1	Loss of communication and GPI functionality	B
A0/SDI/GPI1	7	SCL/$\overline{\text{SYNC}}$/GPI2	Loss of communication and GPI functionality	B
		SDA/SCLK/GPI0	Loss of communication and GPI functionality	B
SDA/SCLK/GPI0	8	A0/SDI/GPI1	Loss of communication and GPI functionality	B
		NC	Short to corner pin is not expected	D
NC	9	SDA/SCLK/GPI0	Short to corner pin is not expected	D
		NC	No change in functionality or performance	D
NC	10	NC	No change in functionality or performance	D
		OUT1	No change in functionality or performance	D
OUT1	11	NC	No change in functionality or performance	D
		FB1	This is intended connection	D
FB1	12	OUT1	This is intended connection	D
		CAP	Short to corner pin is not expected	D
CAP	13	FB1	Short to corner pin is not expected	D
		AGND	Device enters short circuit protection, power consumption increases	B
AGND	14	CAP	Device enters short circuit protection, power consumption increases	B
		VDD	Complete loss of functionality, no device damage	B
VDD	15	AGND	Complete loss of functionality, no device damage	B
		MODE	Loss of communication functionality	B
MODE	16	VDD	Loss of communication functionality	B
		FB0	Short to corner pin is not expected	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB0	1	OUT0 (PWM) is always low	B
OUT0	2	Device can be damaged over a period of time	A
NC	3	No change in functionality or performance	D
NC	4	No change in functionality or performance	D
SDO	5	Read back data is corrupted	B
SCL/$\overline{\text{SYNC}}$/GPI2	6	Loss of communication with the device	B
A0/SDI/GPI1	7	Loss of communication with the device	B
SDA/SCLK/GPI0	8	Loss of communication with the device	B
NC	9	No change in functionality or performance	D
NC	10	No change in functionality or performance	D
OUT1	11	OUT0 (PWM) is always low	B
FB1	12	OUT0 (PWM) is always low	B
CAP	13	Open-circuited pin can cause damage to the low-voltage digital core and NVM supplied by the internal LDO	A
AGND	14	Complete loss of functionality, no device damage	B
VDD	15	No change in functionality or performance	D
MODE	16	Loss of communication functionality	B

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