Functional Safety Information

TPSI2072-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for TPSI2072-Q1 (DWQ package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the functional block diagram of TPSI2072-Q1 for reference.

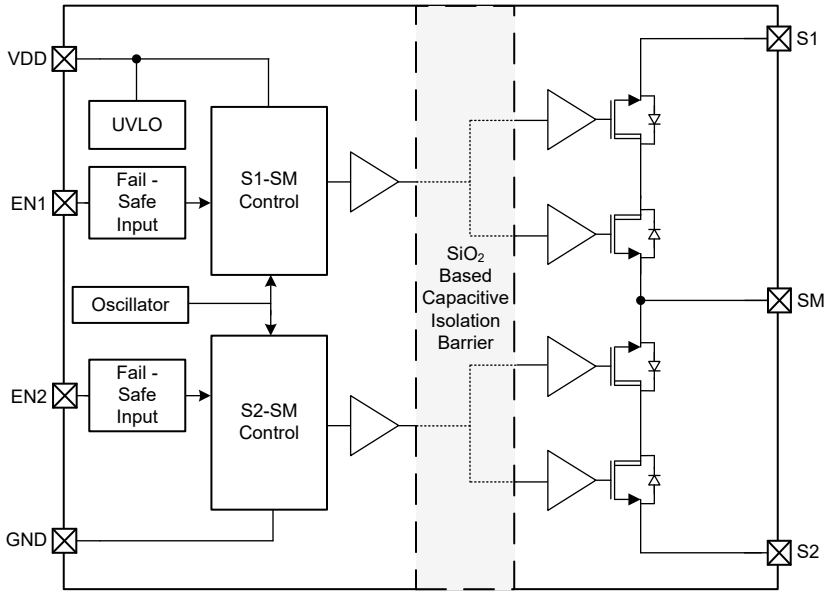

Figure 1-1. TPSI2072-Q1 Functional Block Diagram

TPSI2072-Q1 was developed using a quality-managed development process, but was not developed in accordance with IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the TPSI2072-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	22
Die FIT Rate	4
Package FIT Rate	18

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 200 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	30 FIT	75°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPSI2072-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
One switch stuck OFF	45
Both switches stuck OFF	10
Switch OFF current higher than specification	35
Primary side ON current higher than specification	10

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPSI2072-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to Adjacent Pin (see Table 4-4)

Table 4-2 through Table 4-4 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1. Note that when pin short to ground case is discussed, only primary side ground shorts are considered.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Below is the TPSI2072-Q1 pin diagram package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPSI2072-Q1 data sheet.

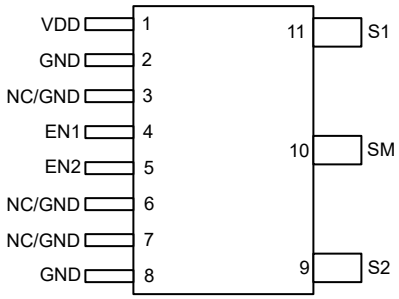

Figure 4-1. TPSI2072-Q1 Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	Device in OFF state (UVLO), secondary side switch in OFF state	B
GND	2	No effect	D
NC/GND	3	No effect	D
EN1	4	Secondary side switch from S1-SM in OFF state	B
EN2	5	Secondary side switch from SM-S2 in OFF state	B
NC/GND	6	No effect	D
NC/GND	7	No effect	D
GND	8	No effect	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	Device in OFF state (UVLO), secondary side switch in OFF state	B
GND	2	No effect	D
NC/GND	3	No effect	D
EN1	4	Secondary side switch from S1-SM in OFF state	B
EN2	5	Secondary side switch from SM-S2 in OFF state	B
NC/GND	6	No effect	D
NC/GND	7	No effect	D
GND	8	No effect	D
S2	9	No effect	D
SM	10	No effect	D
S1	11	No effect	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	2	Device in OFF state (UVLO), secondary side switch in OFF state	B
GND	2	3	No effect	B
NC/GND	3	4	No effect if pin 3 is NC, if pin 3 is GND the secondary side switch between S1-SM will be in OFF state	D or B
EN1	4	5	The states of the secondary sides switches between S1-SM and SM-S2 will always be both ON or both OFF depending on pin voltage.	B
EN2	5	6	No effect if pin 6 is NC, if pin 6 is GND the secondary side switch between SM-S2 will be in OFF state	D or B
NC/GND	6	7	No effect	D
NC/GND	7	8	No effect	D
S2	9	10	The secondary side switch between SM-S2 is shorted out by the external connection.	C
SM	10	11	The secondary side switch between S1-SM is shorted out by the external connection.	C

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