Functional Safety Information

TLVx365-Q1 Functional Safety FIT Rate and Pin FMA

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1 Overview

This document contains information for TLVx365-Q1 (SOT-23 and SOIC packages) to aid in a functional safety system design. The SOT-23 package is the TLV365-Q1 and the SOIC package is the TLV2365-Q1. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

TLVx365-Q1 shows the device functional block diagram for reference.

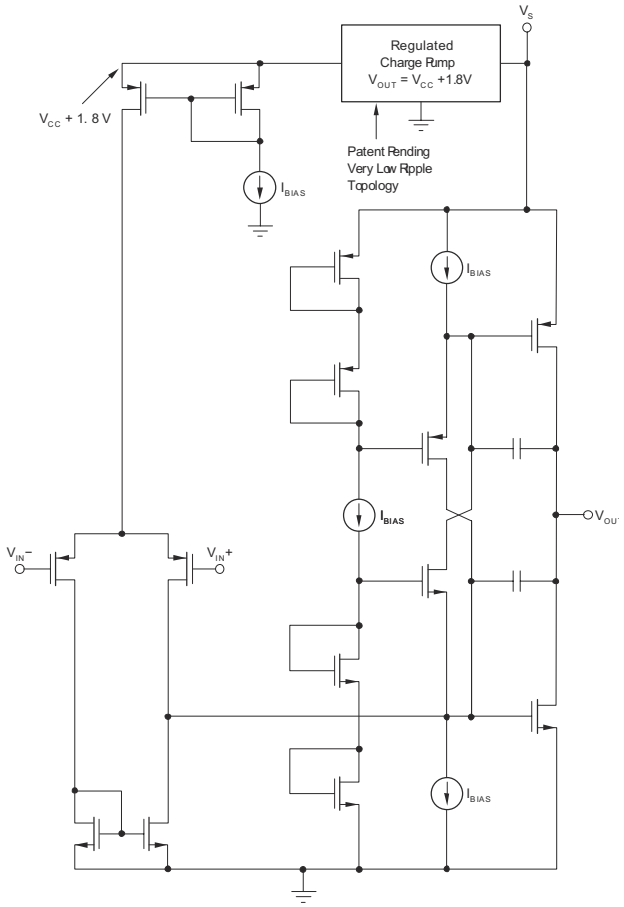

Figure 1-1. Functional Block Diagram

TLVx365-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOT-23 Package

This section provides functional safety failure in time (FIT) rates for the SOT-23 package of the TLVx365-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	4
Die FIT Rate	2
Package FIT Rate	2

The failure rate and mission profile information in comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 24.25 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op Amp, Comparators, Voltage Monitors	4 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 SOIC Package

This section provides functional safety failure in time (FIT) rates for the SOIC package of the TLVx365-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	10
Die FIT rate	3
Package FIT rate	7

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 48.5 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	BICMOS Op Amp, Comparators, Voltage Monitors	4 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TLVx365-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output is floating, open	20
Output is stuck, high	20
Output is stuck, low	20
Output functional, not in specification	40

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TLVx365-Q1 (SOT-23 and SOIC packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to V+ (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Total supply voltage of 5V with V+ connected to 5V and V- connected to ground.
- Input and output pins biased to 2.5V reference point.
- Device is configured with feedback network in gain greater than or equal to 1V/V.

4.1 SOT-23 Package

Figure 4-1 shows the TLVx365-Q1 pin diagram for the SOT-23 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLVx365-Q1 data sheet.

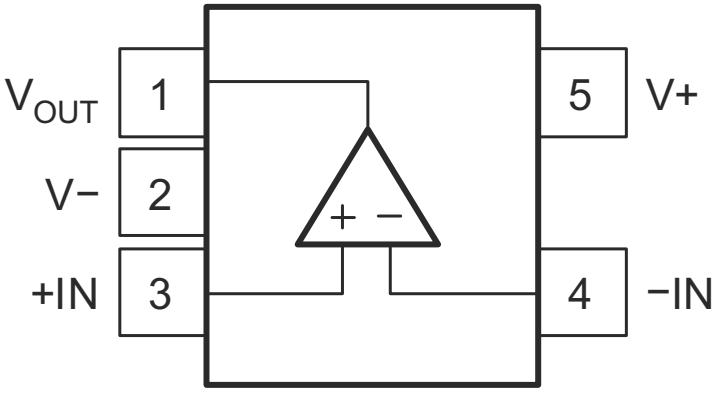

Figure 4-1. Pin Diagram (SOT-23) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VOUT	1	Short to GND may cause device to overheat.	B
V-	2	Normal operation, unless dual supply voltage was intended.	D
+IN	3	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
-IN	4	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
V+	5	Diodes from input to V+ may turn on due to input signal and cause electrical overstress (EOS).	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VOUT	1	Output can be left open. There is no effect on the device, but the output will not be measured.	C
V-	2	Lowest voltage output pin will try to power the V- pin of the device.	B
+IN	3	Floating input, circuit will likely not function as expected.	C
-IN	4	Floating input, circuit will likely not function as expected.	C
V+	5	Highest voltage output pin will try to power the V+ pin of the device.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VOUT	1	V-	Short to V- may cause device to overheat.	B
V-	2	+IN	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
+IN	3	-IN	No damage to device. Application circuit will not work. Pins are not adjacent to each other.	C
-IN	4	V+	Input at V+ is a valid input, however, desired application result is unlikely. Pins are not as near to each other, due to package type.	B
V+	5	VOUT	Short to VS+ may cause device to overheat. Pins are not adjacent to each other.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to V+

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VOUT	1	Short to V+ may cause device to overheat.	B
V-	2	Diodes from input to V- may turn on due to input signal and cause electrical overstress (EOS).	A
+IN	3	Input at V+ is a valid input, however, desired application result is unlikely.	C
-IN	4	Input at V+ is a valid input, however, desired application result is unlikely.	C
V+	5	Normal Operation.	D

4.2 SOIC Package

Figure 4-2 shows the TLVx365-Q1 pin diagram for the SOIC package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLVx365-Q1 data sheet.

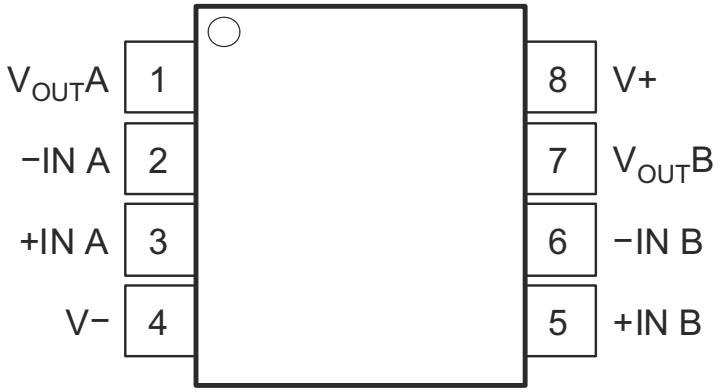

Figure 4-2. Pin Diagram (SOIC Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VOUTA	1	Short to GND may cause device to overheat.	B
-IN A	2	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
+IN A	3	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
V-	4	Normal operation, unless dual supply voltage was intended.	D
+IN B	5	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
-IN B	6	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
VOUTB	7	Short to GND may cause device to overheat.	B
V+	8	Diodes from input to V+ may turn on due to input signal and cause electrical overstress (EOS).	A

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VOUTA	1	Output can be left open. There is no effect on the device, but the output will not be measured.	C
-IN A	2	Floating input, circuit will likely not function as expected.	C
+IN A	3	Floating input, circuit will likely not function as expected.	C
V-	4	Lowest voltage pin will try to power the V- pin of the device.	B
+IN B	5	Floating input, circuit will likely not function as expected.	C
-IN B	6	Floating input, circuit will likely not function as expected.	C
VOUTB	7	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
V+	8	Highest voltage output pin will try to power the V+ pin of the device.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VOUTA	1	-IN A	Channel 1 configured in unity gain	C
-IN A	2	+IN A	No damage to device. Application circuit will not work.	C
+IN A	3	V-	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
V-	4	+IN B	Input at V- (GND) is valid input, however, desired application result is unlikely. Pins are not adjacent to each other.	C
+IN B	5	-IN B	No damage to device. Application circuit will not work	C
-IN B	6	VOUTB	Channel 2 configured in unity gain	C
VOUTB	7	V+	Short to V+ may cause device to overheat.	B
V+	8	VOUTA	Short to V+ may cause device to overheat. Pins are not adjacent to each other.	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to V+

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VOUTA	1	Short to VS+ may cause device to overheat.	B
-IN A	2	Input at V+ is valid input, however, desired application result is unlikely.	C
+IN A	3	Input at V+ is a valid input, however, desired application result is unlikely.	C
V-	4	Diodes from input to V- may turn on due to input signal and cause electrical overstress (EOS).	A
+IN B	5	Input at V+ is a valid input, however, desired application result is unlikely.	C
-IN B	6	Input at V+ is a valid input, however, desired application result is unlikely.	C
VOUTB	7	Short to VS+ may cause device to overheat.	B
V+	8	Normal Operation.	D

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