Functional Safety Information

TPS1214-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS1214-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

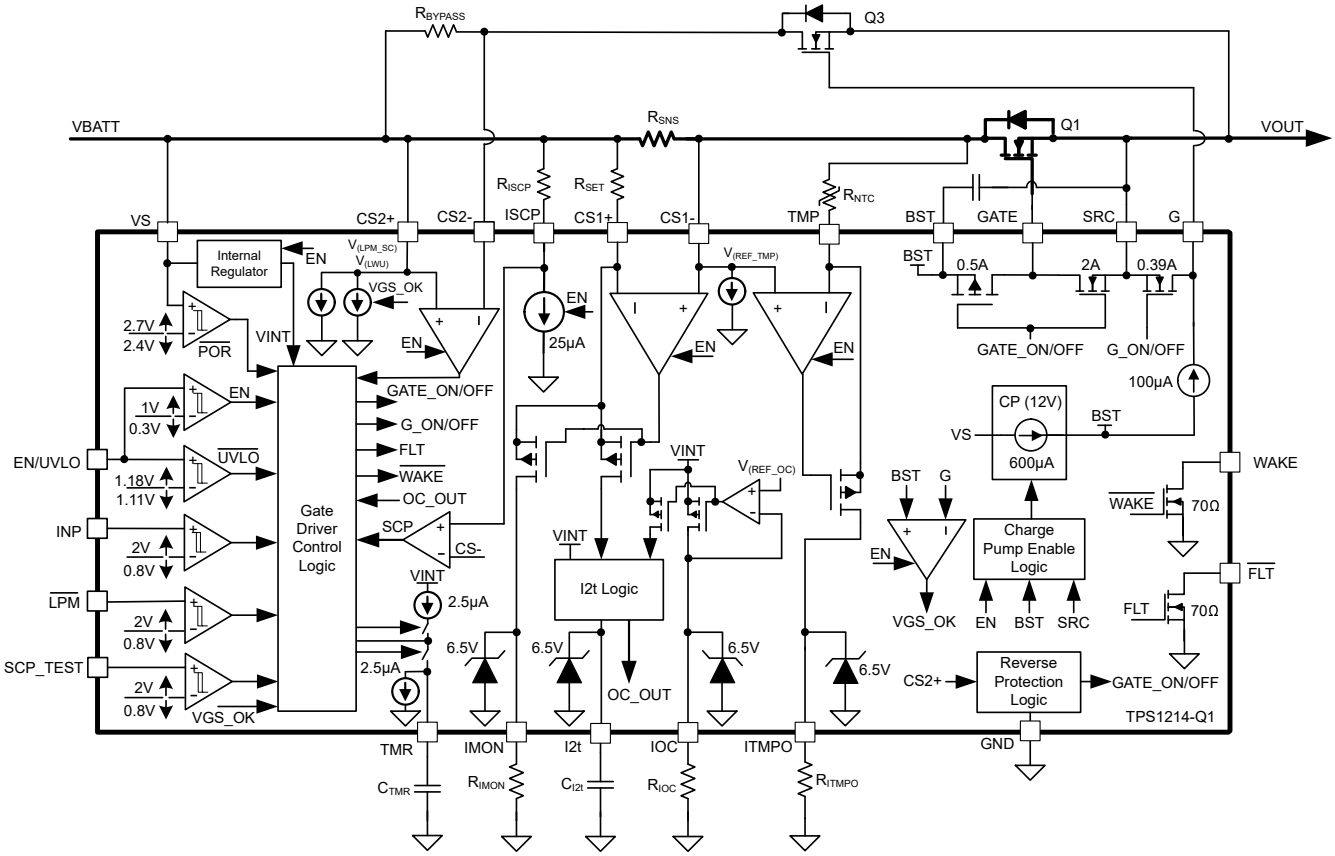

Figure 1-1. Functional Block Diagram

TPS1214-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS1214-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	12
Die FIT Rate	3
Package FIT Rate	6

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 12mW
- Climate type: World-wide Table 8 IEC TR 62380
- Package factor (lambda 3): Table 17b IEC TR 62380
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	30 FIT	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS1214-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Gate output stuck high	19%
Gate output stuck low	34%
Gate output functional, not in specification voltage or timing	27%
Short circuit protection fails to trip or false trip	2%
i2t protection fails to trip or false trip	6%
IMON not in specification	3%
ITMPO not in specification	4%
Pin to Pin short any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS1214-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-2)
- Pin short-circuited to an adjacent pin (see Table 4-2)
- Pin short-circuited to supply (see Table 4-2)

Table 4-2 through Table 4-2 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS1214-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS1214-Q1 data sheet.

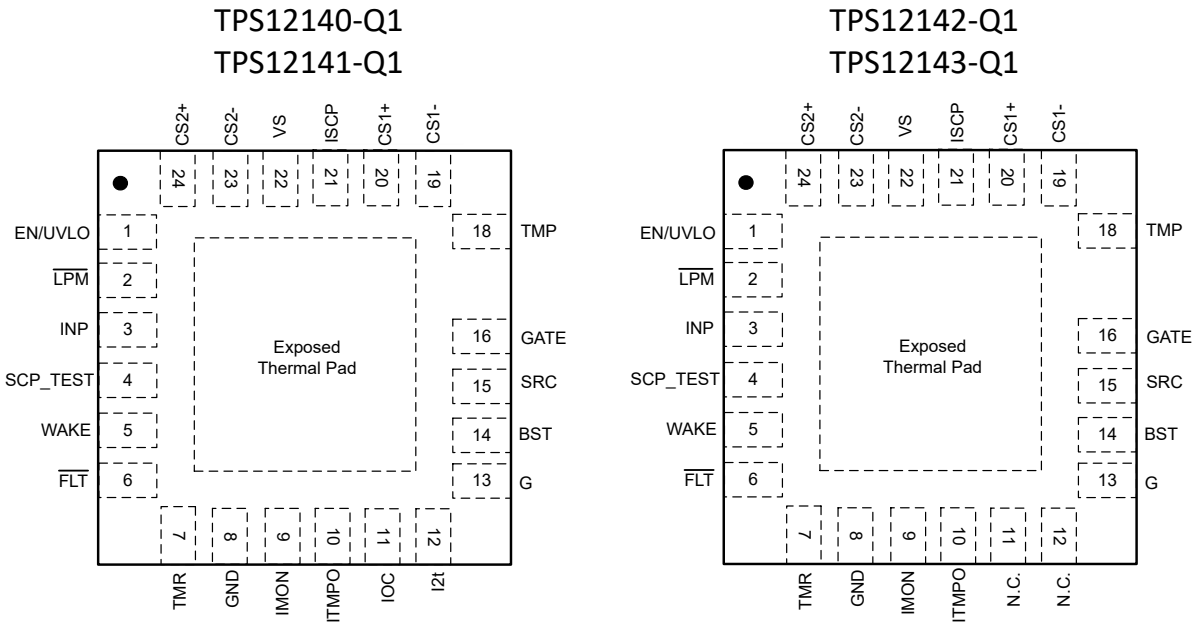

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Follow data sheet recommendation for operating conditions, external component selection and PCB layout

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	Normal operation. The device is disabled.	B
$\overline{\text{LPM}}$	2	Device remains in low power mode (LPM) and bypass path (G) overcurrent protection is active.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
INP	3	If $\overline{\text{LPM}}$ = High then, Main path (GATE) does not turn ON. $\overline{\text{LPM}}$ = Low: No concern.	B
SCP_TEST	4	Normal operation. SCP_TEST Diagnosis is not available.	B
WAKE	5	Pin is pulled to GND through internal pull down. No concerns. In LPM, current is limited by external pull-up resistor on WAKE pin. WAKE functionality is not be available.	B
$\overline{\text{FLT}}$	6	I2t based Overcurrent, short-circuit, Charge pump UVLO fault diagnostic can not be reported.	B
TMR	7	Device is in Latch off mode.	B
GND	8	Normal operation.	D
IMON	9	IMON information is not available.	B
ITMPO	10	ITMPO information is not available.	B
IOC	11	I2t based overcurrent protection is not be available.	B
I2t	12	I2t based overcurrent protection is disabled.	B
G	13	With G grounded, if the pin voltage between SRC and G exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
BST	14	Gate driver supply does not come up. Gate drives (GATE and G) remain OFF.	B
SRC	15	Output short to GND protection kicks in.	B
GATE	16	With GATE grounded, if the pin voltage between SRC and GATE exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
TMP	18	With TMP grounded, if the pin voltage between TMP and SRC exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
CS1-	19	With CS1- grounded, if the pin voltage between CS1+ and CS1– exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
CS1+	20	With CS1+ grounded, if the pin voltage between CS1+ and CS1– exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
ISCP	21	With ISCP grounded, if the pin voltage between ISCP and CS1– exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
VS	22	With VS grounded, if the pin voltage between VS and SRC exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
CS2-	23	False loadwakeup triggers.	B
CS2+	24	With CS2+ grounded, if the pin voltage between CS2+ and SRC exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	Internal pulldown brings EN/UVLO to low disabling the device.	B
$\overline{\text{LPM}}$	2	Internal pulldown brings $\overline{\text{LPM}}$ to low, pulling G output high. Device can not transition to Active mode.	B
INP	3	Internal pulldown brings INP to low, pulling GATE output low.	B
SCP_TEST	4	Internal pulldown brings SCP_TEST to low. Normal operation. SCP_TEST Diagnosis is not available.	B
WAKE	5	WAKE is pulled to GND in active mode through internal switch. WAKE indication is not available.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
$\overline{FLT}$	6	I2t based Overcurrent, short-circuit, Charge pump UVLO fault diagnostic can not be reported.	B
TMR	7	Device goes to auto-retry mode after overcurrent fault with minimum auto-retry time based on parasitic capacitor on TMR pin.	B
GND	8	Device does not power up and is disabled.	B
IMON	9	I2t based overcurrent protection is disabled.	B
ITMPO	10	Normal operation.	D
IOC	11	Minimum I2t start threshold OCP threshold is set. I2t based overcurrent protection is incorrect. Device powers up but main path (GATE) turns OFF based on C_{I2t}.	B
I2t	12	I2t based overcurrent protection is incorrect.	B
G	13	G output is not controlled. Bypass path remains OFF.	B
BST	14	External FET is turned ON and OFF repetitively due to no capacitor connection at BST pin.	B
SRC	15	The external FET does not turn OFF as the FET source got disconnected from the internal pulldown driver.	B
GATE	16	The external FET does not turn OFF as the FET GATE disconnects from the internal pulldown driver.	B
TMP	18	ITMPO is unavailable.	B
CS1-	19	CS1– is internally clamped to CS1+ minus 2 diode drops. Device detects false short-circuit fault. IMON and I2t protection are unavailable.	B
CS1+	20	Device detects false short-circuit fault. IMON and I2t protection are unavailable.	B
ISCP	21	Short-circuit protection feature is disabled.	B
VS	22	Device is not powered up and is disabled.	B
CS2-	23	Device detects false loadwakeup event.	B
CS2+	24	Device is damaged.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	2 ($\overline{LPM}$)	When EN/UVLO is driven high then device turns ON in Active mode	B
$\overline{LPM}$	2	3 (INP)	When INP is Low: Device remains in LPM. High current protection in Bypass path (G) active. When INP is High: Device powers up in active mode.	B
INP	3	4 (SCP_TEST)	If SCP_TEST = Low and $\overline{LPM}$ = High then, Main path (GATE) is not turn ON. INP voltage goes to 0V. $\overline{LPM}$ = Low: No concern. If SCP_TEST = High and $\overline{LPM}$ = High: Main path (GATE) is always be OFF and $\overline{FLT}$ asserts low. $\overline{LPM}$ Low: No concern.	B
SCP_TEST	4	5 (WAKE)	Device can damage if SCP_TEST is connected to a strong supply with current higher than 5mA and WAKE goes low during active mode. Preventive action is to connect diode and at least 1kΩ resistor in series with SCP_TEST	B
WAKE	5	6 ($\overline{FLT}$)	WAKE and $\overline{FLT}$ indication not available.	B
TMR	7	8 (GND)	Device is set to latch-off mode if overcurrent fault is detected.	B
GND	8	9 (IMON)	IMON output is not reported.	B
IMON	9	10 (ITMPO)	IMON and ITMPO output is not reported.	B
ITMPO	10	11 (IOC)	Device can detect false I2t based overcurrent and ITMPO output is not reported.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IOC	11	12 (I2t)	Device can detect false I2t based overcurrent.	B
G	13	14 (BST)	BST cap can discharge through the pull down on G pin. Bypass path (G) is not be able to turn ON if $V_{GS(th)}$ of bypass FET is > 2V.	B
BST	14	15 (SRC)	Gate drive supply is shorted and external FETs do not turn ON.	B
SRC	15	16 (GATE)	Shorting of the pulldown switch (between GATE and SRC) of the internal gate driver. External FET remains OFF.	B
CS1-	19	18 (CS1+)	Bypasses the external current sense resistor. IMON, overcurrent and short-circuit protection features get disabled.	B
CS1+	20	19 (ISCP)	IMON information is not available. False SCP can trigger.	B
ISCP	21	20 (VS)	Short-circuit protection is set to minimum setting (2mV).	C
VS	22	23 (CS2-)	Loadwakeup functionality is unavailable.	B
CS2-	23	24 (CS2+)	Loadwakeup functionality is unavailable.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	Device remains enabled. If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
$\overline{\text{LPM}}$	2	Device turns ON in active mode. If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
INP	3	Main path (GATE) remains ON in active mode. If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
SCP_TEST	4	If $\overline{\text{LPM}}$ = High then, Main path (GATE) remains OFF in active mode. If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
WAKE	5	If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
$\overline{\text{FLT}}$	6	If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
TMR	7	If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
GND	8	If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
IMON	9	If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
ITMPO	10	If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
IOC	11	If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
I2t	12	If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
G	13	If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
BST	14	If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
SRC	15	Output stuck on to supply	B
GATE	16	If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
TMP	18	If pin voltage exceeds the pin data sheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
CS1-	19	In the application, the external sense resistor is bypassed and IMON, I2t based over current and short circuit protection is not work.	B
CS1+	20	IMON and I2t outputs are saturated. External FET (GATE) turns OFF due to false overcurrent event.	B
ISCP	21	Short-circuit protection is set to minimum setting of 2mV.	C
VS	22	Normal operation.	D
CS2-	23	Loadwakeup functionality is disabled.	B
CS2+	24	Normal operation.	D

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