Functional Safety Information

LM5190-Q1 and LM25190-Q1 Functional Safety FIT Rate, FMD, and Pin FMA

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Trademarks

1 Overview

This document contains information for LM5190-Q1 and LM25190-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

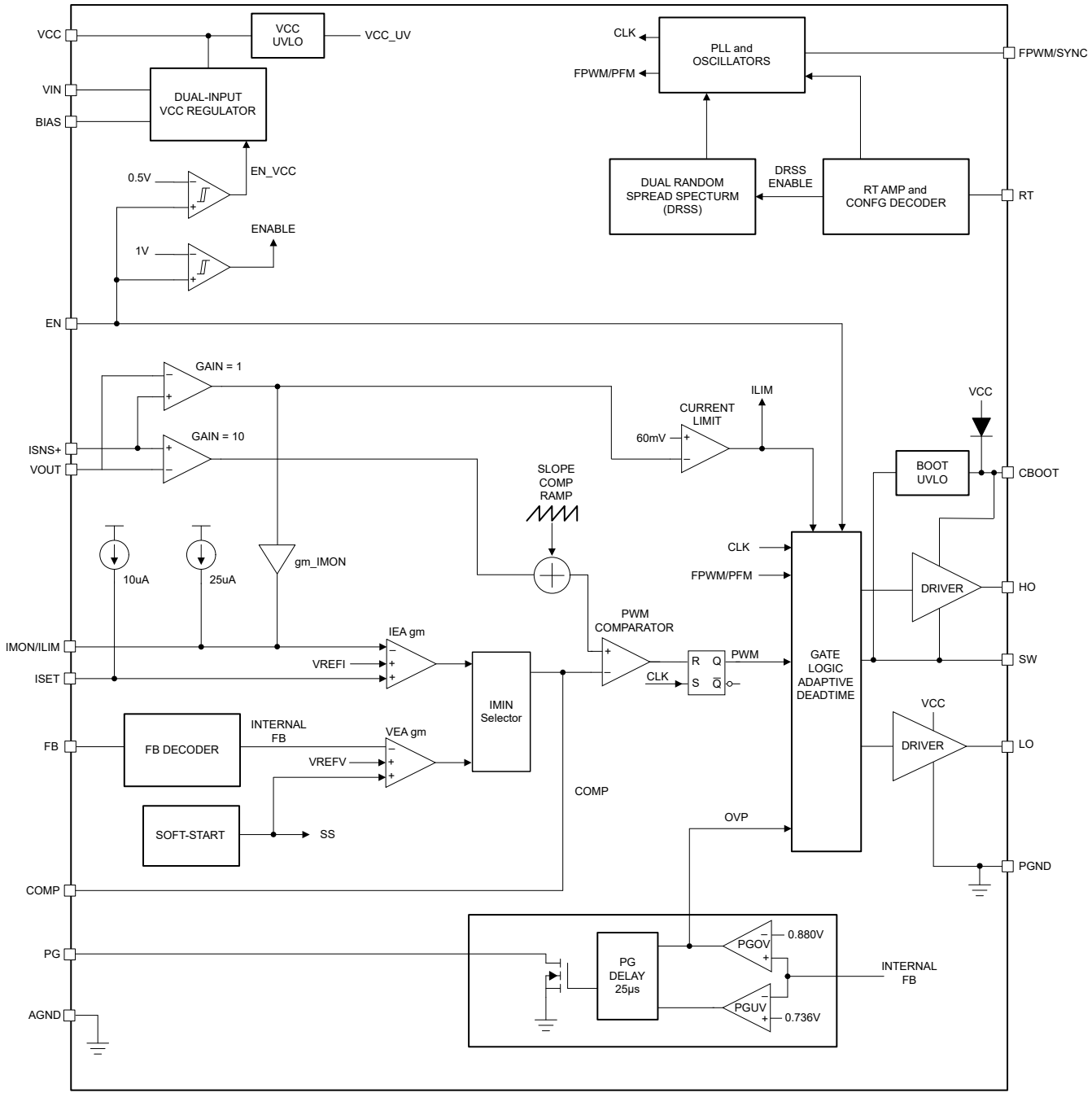

Figure 1-1. Functional Block Diagram

LM5190-Q1 and LM25190-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for LM5190-Q1 and LM25190-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	16
Die FIT rate	7
Package FIT rate	9

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 750mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed HV > 50V supply	30 FIT	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM5190-Q1 and LM25190-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No Output Voltage	40
Output not in specification – voltage or timing	25
Gate driver stuck on	5
Constant – current limit not in specification	20
Power good – false trip or fails to trip	5
Short circuit any two pins	5

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM5190-Q1 and LM25190-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM5190-Q1 and LM25190-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM5190-Q1 and LM25190-Q1 datasheets.

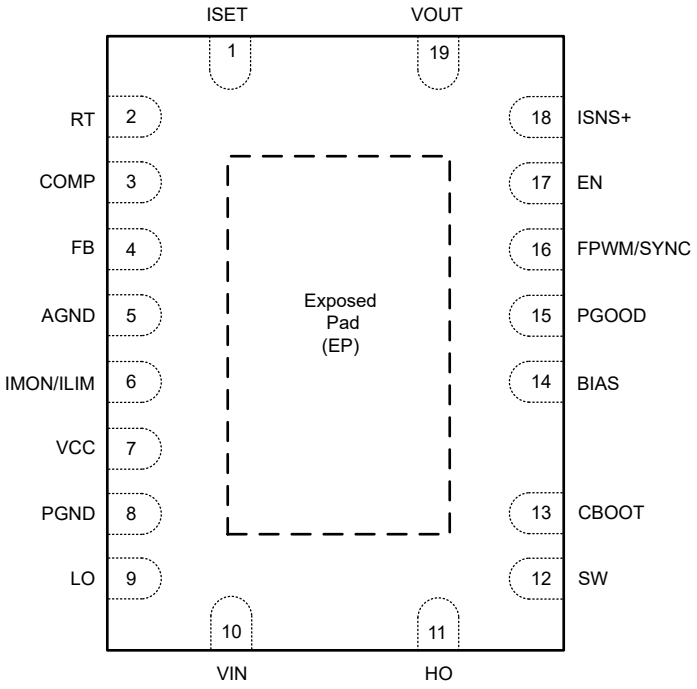

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ISET	1	VOUT = 0V. The ISET pin is not functional.	B
RT	2	The output voltage attempts to regulate at maximum FSW, causing maximum power dissipation.	C
COMP	3	VOUT = 0V.	B
FB	4	The target of the output voltage is set to 5V.	B
AGND	5	The AGND pin is GND. VOUT = VOUT is as expected.	D
IMON/ILIM	6	VOUT = VOUT is as expected. The current monitor and CC limit are not functional.	B
VCC	7	VOUT = 0V, the device does not switch, the output of the VCC pin is loaded.	B
PGND	8	The PGND pin is GND. VOUT = VOUT is as expected.	D
LO	9	VOUT = 0V, the internal VCC regulator is loaded to current limit.	B
VIN	10	VOUT = 0V.	B
HO	11	VOUT = 0V, the internal VCC regulator is loaded to current limit.	B
SW	12	VOUT = 0V. The high-side FET is shorted from the VIN pin to GND.	A
CBOOT	13	VOUT = 0V. The high-side FET is shorted from the VIN pin to GND.	B
BIAS	14	VOUT = VOUT is as expected. The internal VCC regulator provides bias voltage.	C
PGOOD	15	VOUT = VOUT is as expected. The PGOOD pin is not functional.	C
FPWM/SYNC	16	VOUT = VOUT is as expected. There is no synchronization available and the device is always in PFM mode.	C
EN	17	VOUT = 0V. The **device** is always in shutdown.	B
ISNS+	18	VOUT = 0V.	A
VOUT	19	VOUT = 0V.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ISET	1	VOUT = VOUT is as expected. The ISET pin is not functional.	C
RT	2	The RT pin regulates to 1V, but the internal oscillator does not function.	B
COMP	3	The output voltage oscillates.	A
FB	4	VOUT = VIN.	A
AGND	5	The output voltage is indeterminate.	B
IMON/ILIM	6	VOUT = 0V. The current monitor and CC limit are not functional.	B
VCC	7	VOUT = 0V.	B
PGND	8	VOUT = 0V.	B
LO	9	VOUT = VOUT is as expected but with reduced efficiency.	C
VIN	10	VOUT = 0V.	B
HO	11	If the HO pin is opened while the HO pin has voltage to the SW pin, the high-side FET never turns off. VOUT = VIN.	A
SW	12	The output voltage is indeterminate. The floating rail of the CBOOT pin has no reference to the actual node of the SW pin. VOUT = VIN.	A
CBOOT	13	VOUT = 0V.	B
BIAS	14	VOUT = VOUT is as expected. The internal VCC regulator provides bias voltage.	C
PGOOD	15	VOUT = VOUT is as expected. The PGOOD pin is not functional.	C
FPWM/SYNC	16	VOUT = VOUT is as expected. There is no synchronization available and **the device** is always in FPWM mode.	C
EN	17	VOUT = 0V.	B
ISNS+	18	The open ISNS+ pin blocks current limit and causes the output voltage to oscillate.	A
VOUT	19	VOUT = 0V, if the internal feedback is used.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
ISET	1	RT	If the resistor of the RT pin is tied to the VCC pin, the ISET pin can be damaged. If the resistor of the RT pin is tied to the AGND pin, VOUT = VOUT is as expected. The switching frequency is lower. The CC operation is affected.	A
RT	2	COMP	If the resistor of the RT pin is tied to the VCC pin, the COMP pin can be damaged. If the resistor of the RT pin is tied to the AGND pin, VOUT = 0V.	A
COMP	3	FB	External FB mode: The COMP pin regulates to 0.8V and the output is unregulated. VOUT = indeterminate.	B
			Internal FB mode FB = VCC, there is damage to the device.	A
			Internal FB mode FB = GND, VOUT = 0V.	B
FB	4	AGND	The target of the output voltage is set to 5V.	B
AGND	5	IMON/ILIM	VOUT = VOUT is as expected. The current monitor and CC limit are not functional.	C
IMON/ILIM	6	VCC	There is damage to the device.	A
VCC	7	PGND	The VCC pin is grounded. VOUT = 0V.	B
PGND	8	LO	VOUT = 0V. The VCC pin is loaded by the LO driver.	B
LO	9	VIN	VOUT = 0V. The driver is damaged if VIN > 8V.	A
VIN	10	HO	For VIN > 8V, the **pin** exceeds the maximum ratings and the HO pin is damaged. For VIN < 8V, VOUT = dropout is lower than the VIN pin voltage, no switching, and there is excess current from the VIN pin.	A
HO	11	SW	VOUT = 0V.	B
SW	12	CBOOT	VOUT = 0V.	B
CBOOT	13	BIAS	There is damage to the device if CBOOT > 30V.	A
BIAS	14	PGOOD	The pulldown of the PG pin can be damaged. VOUT = VOUT is as expected.	A
PGOOD	15	FPWM/SYNC	VOUT = VOUT is as expected. If the FPWM pin is tied to the VCC pin, the pulldown of the PG pin can be damaged.	A
FPWM/SYNC	16	EN	VOUT = VOUT is as expected.	A
EN	17	ISNS+	The EN pin is high-voltage rated. VOUT = VOUT is as expected if VOUT > 1V. If VOUT < 1V, **the device** is disabled.	B
ISNS+	18	VOUT	The current limit is disabled since the current limit resistor is shorted. The output voltage cannot regulate since current-mode feedback is shorted.	A
VOUT	19	ISET	VOUT = 0V. If prebias VOUT > 5.5V, the ISET pin is damaged.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ISET	1	There is damage to the device if VIN > 5.5V.	A
RT	2	There is damage to the device if VIN > 8V.	A
COMP	3	There is damage to the device if VIN > 5.5V If VIN < 5.5V, the output voltage is out of regulation.	A
FB	4	There is damage to the device if VIN > 8V. If VIN < 8V, VOUT = VIN is as expected.	A
AGND	5	VOUT = 0V.	B
IMON/ILIM	6	There is damage to the device if VIN > 5.5V.	A
VCC	7	There is damage to the device if VIN > 8V. If VIN < 8V, VOUT = VOUT is as expected.	A
PGND	8	VOUT = 0V.	B
LO	9	VOUT = 0V. The driver is damaged if VIN > 8V.	A
VIN	10	N/A	D
HO	11	For VIN > 8V, **the pin** exceeds the maximum ratings and the HO pin is damaged. For VIN < 8V, VOUT = dropout is lower than the VIN pin, there is no switching, and there is excess current from the VIN pin.	A
SW	12	VOUT = VIN, there is excess current from the VIN pin. The LO pin turns on and shorts against the VIN pin.	B
CBOOT	13	There is damage to the device if VIN > 8V. If VIN < 8V, VOUT < the output voltage target.	A
BIAS	14	There is damage to the device if VIN > 30V.	A
PGOOD	15	There is damage to the device.	A
FPWM/SYNC	16	There is damage to the device if VIN > 8V. If VIN < 8V, VOUT = VOUT is as expected, but **the device** is always in FPWM mode.	A
EN	17	**The device** is always on. VOUT = VOUT is as expected.	C
ISNS+	18	There is damage to the device.	A
VOUT	19	VOUT = VIN.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2025	*	Initial Release

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