Functional Safety Information

DRV81004-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the DRV81004-Q1 (14-pin HTSSOP (PWP) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

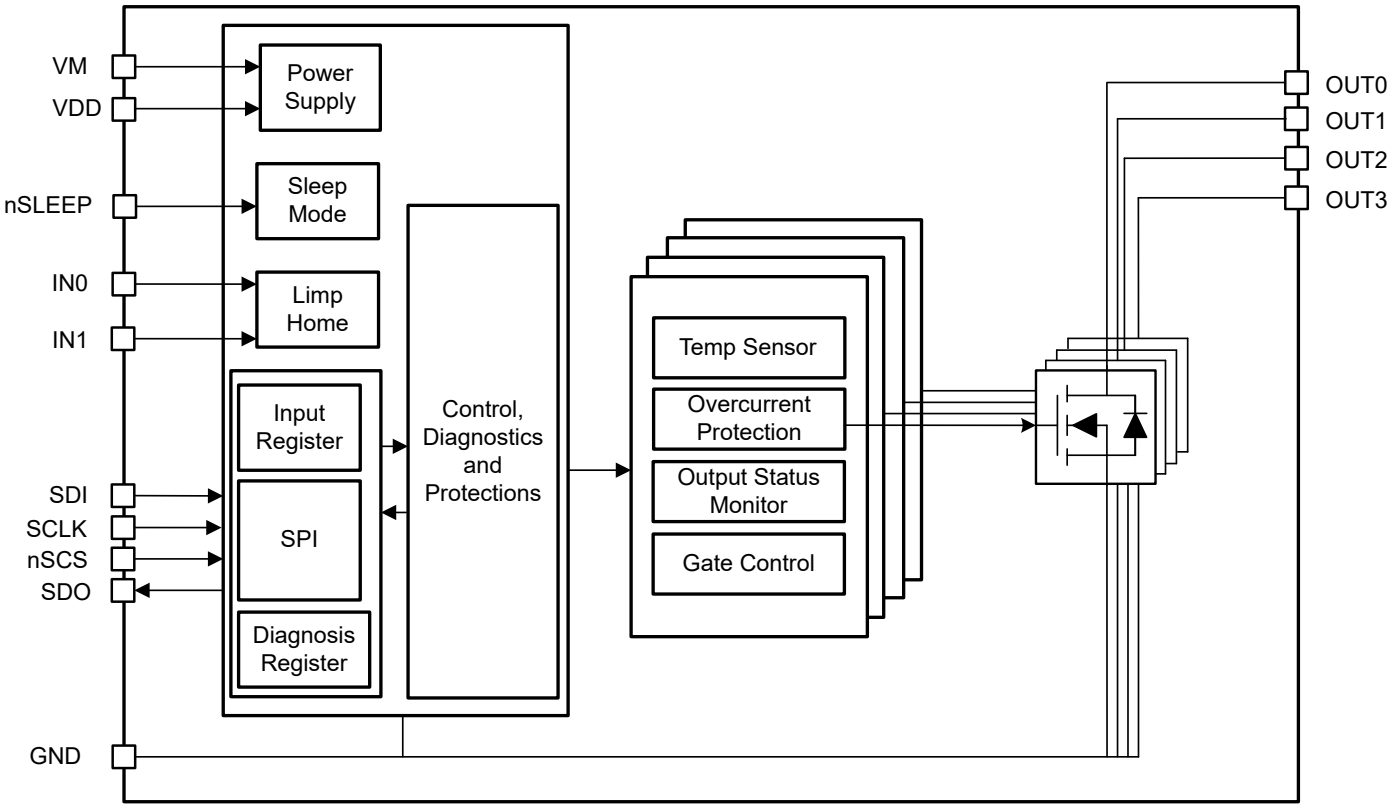

Figure 1-1. Functional Block Diagram

The DRV81004-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the DRV81004-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	18
Die FIT rate	9
Package FIT rate	9

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1W
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the DRV81004-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT is stuck LOW when commanded OFF	10
OUT is stuck OFF when commanded LOW	10
OUT ON resistance too high when commanded LOW	10
OUT slew rate too fast or too slow	10
OUT is stuck HIGH when commanded OFF	10
OUT is stuck OFF when commanded HIGH	10
OUT ON resistance too high when commanded HIGH	9
Incorrect fault indication	25
Incorrect operation of clamp circuit	6

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the DRV81004-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the DRV81004-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the DRV81004-Q1 data sheet.

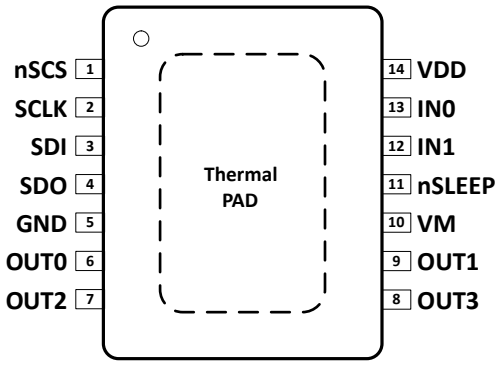

Figure 4-1. Pin Diagram

Following is the assumption of use and the device configuration assumed for the pin FMA in this section:

- The device is used with external components consistent with the values described in the external component table of the data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
nSCS	1	SPI communication is nonfunctional.	B
SCLK	2	SPI communication is nonfunctional.	B
SDI	3	SPI communication is nonfunctional.	B
SDO	4	SPI communication is nonfunctional.	B
GND	5	Intended operation.	D
OUT0	6	Loss of load control.	B
OUT2	7	Loss of load control.	B
OUT3	8	Loss of load control.	B
OUT1	9	Loss of load control.	B
VM	10	VM undervoltage warning.	B
nSLEEP	11	SPI communication is nonfunctional.	B
IN1	12	Loss of load control.	B
IN0	13	Loss of load control.	B
VDD	14	SPI communication is nonfunctional.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
nSCS	1	SPI communication is nonfunctional.	B
SCLK	2	SPI communication is nonfunctional.	B
SDI	3	SPI communication is nonfunctional.	B
SDO	4	SPI communication is nonfunctional.	B
GND	5	Loss of load control.	B
OUT0	6	False faults are potentially detected.	B
OUT2	7	False faults are potentially detected	B
OUT3	8	False faults are potentially detected	B
OUT1	9	False faults are potentially detected	B
VM	10	VM undervoltage warning.	B
nSLEEP	11	SPI communication is nonfunctional.	B
IN1	12	Loss of load control.	B
IN0	13	Loss of load control.	B
VDD	14	SPI communication is nonfunctional.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to Pin No.	Description of Potential Failure Effects	Failure Effect Class
nSCS	1	2	SPI communication is nonfunctional.	B
SCLK	2	3	SPI communication is nonfunctional.	B
SDI	3	4	SPI communication is nonfunctional.	B
SDO	4	5	SPI communication is nonfunctional.	B
GND	5	6	Loss of load control.	B
OUT0	6	7	Loss of load control, false faults are potentially detected.	B
OUT2	7	8	Loss of load control, false faults are potentially detected.	B
OUT3	8	9	Loss of load control, false faults are potentially detected.	B
OUT1	9	10	Loss of load control, false faults are potentially detected.	B
VM	10	11	False faults are potentially detected.	B
nSLEEP	11	12	Loss of load control.	B
IN1	12	13	Loss of load control.	B
IN0	13	14	Loss of load control.	B
VDD	14	1	SPI communication is nonfunctional.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
nSCS	1	Low voltage pin maximum voltage is violated.	A
SCLK	2	Low voltage pin maximum voltage is violated.	A
SDI	3	Low voltage pin maximum voltage is violated.	A
SDO	4	Low voltage pin maximum voltage is violated.	A
GND	5	VM undervoltage warning.	B
OUT0	6	Loss of load control, false faults are potentially detected.	B
OUT2	7	Loss of load control, false faults are potentially detected.	B
OUT3	8	Loss of load control, false faults are potentially detected.	B
OUT1	9	Loss of load control, false faults are potentially detected.	B
VM	10	Intended operation.	D
nSLEEP	11	No impact to functionality.	D
IN1	12	Low voltage pin maximum voltage is violated.	A
IN0	13	Low voltage pin maximum voltage is violated.	A
VDD	14	Low voltage pin maximum voltage is violated.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2025	*	Initial Release

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