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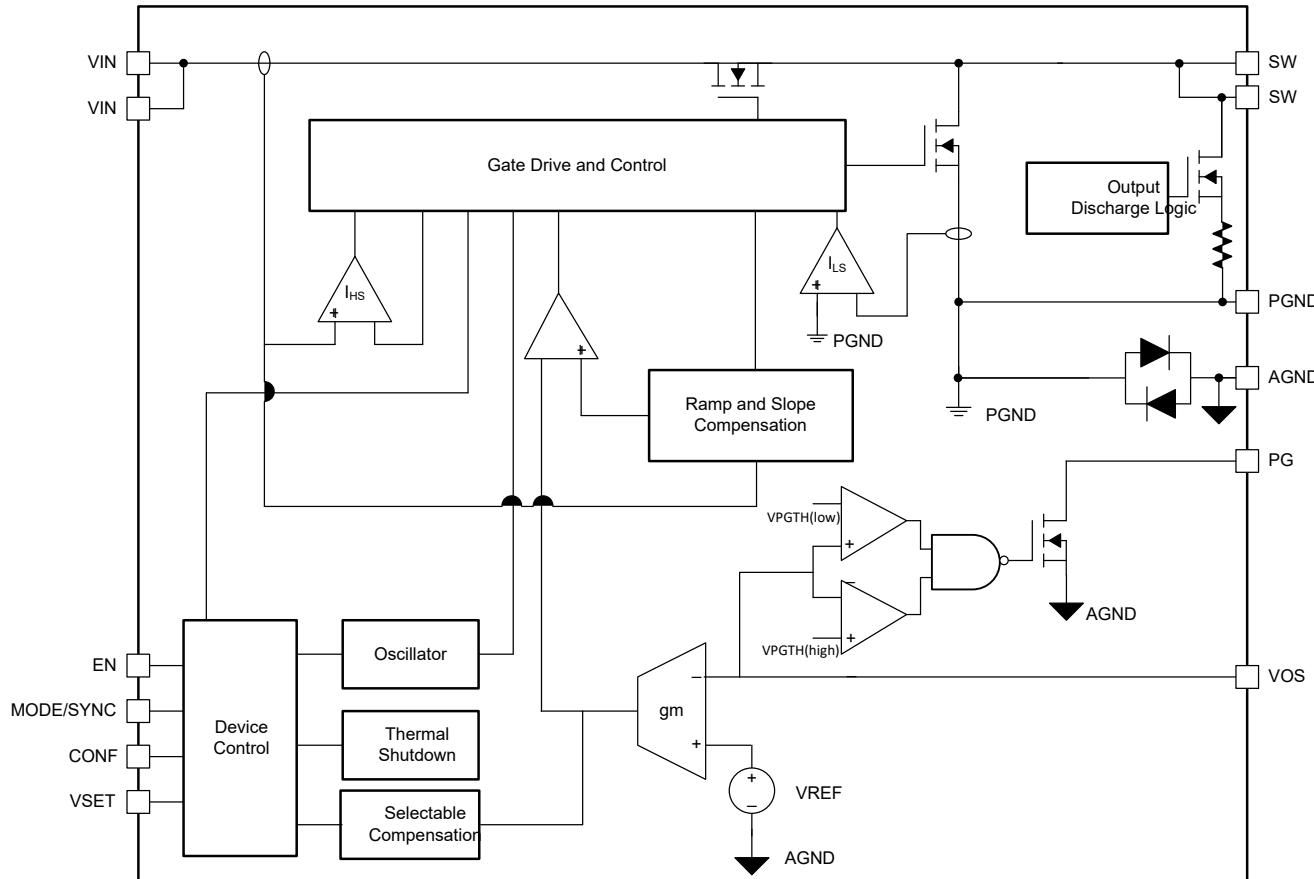
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## 1 Overview

This document contains information for TPS62A204-Q1 (RZX (WQFN-FCRLF, 13) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.



**Figure 1-1. Functional Block Diagram**

TPS62A204-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS62A204-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11.
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2.

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total component FIT rate	8
Die FIT rate	4
Package FIT rate	4

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Automotive control or figure 16
- Power dissipation: 338mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2T**

Table	Category	Reference FIT Rate	Reference Virtual T <sub>j</sub>
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T<sub>j</sub> (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

### 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS62A204-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

Die Failure Modes	Failure Mode Distribution (%)
SW no output	35
SW output not in specification – voltage or timing	45
SW power high-side or low-side FET stuck on	10
PG false trip or fails to trip	5
Short circuit any two pins	5

## 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS62A204-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

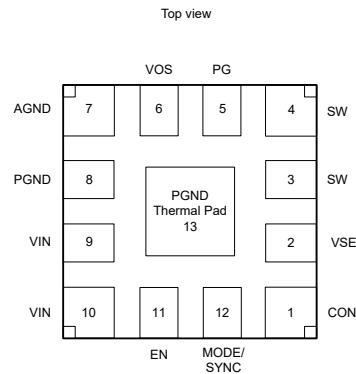
- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to VIN (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

**Table 4-1. TI Classification of Failure Effects**

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-1](#) shows the TPS62A204-Q1 pin diagram. For a detailed description of the device pins, please refer to the *Pin Configuration and Functions* section in the TPS62A204-Q1 data sheet.



**Figure 4-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is operating in the typical application. Please refer to the *Simplified Schematics* in the TPS62A204-Q1 datasheet.

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
CONF	1	There is a loss of functionality. There is the potential for wrong compensation, frequency, and SSC settings.	B
VSET	2	The device powers up with the wrong output voltage.	B
SW	3	The device is potentially damaged.	A
	4		
PG	5	There is no damage to the device, but loss of functionality occurs.	B
VOS	6	There is no damage to the device, but loss of functionality occurs.	B
AGND	7	There device functions as intended.	D
PGND	8	There device functions as intended.	D
	13		

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	9	The device does not power up.	B
	10		
EN	11	The device does not power up.	B
MODE/SYNC	12	The device always operates in automatic (auto) mode (PFM/PWM); rather than adjusting the mode to the correct setting.	B

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
CONF	1	There is a loss of functionality. There is the potential for wrong compensation, frequency, and SSC settings.	B
VSET	2	The device powers up with the wrong output voltage.	B
SW	3	The device powers up and operates if either the 3 or 4 pin is still connected. The performance parameters are potentially degraded.	C
	4		
PG	5	There is no damage to the device, but loss of functionality occurs.	B
VOS	6	There is no damage to the device, but the output voltage can be out of regulation.	B
AGND	7	The device powers up.	C
PGND	8	The device powers up and operates if either the 8 or 13 pin is still connected. The performance parameters are potentially degraded.	C
	13		
VIN	9	The device powers up and operates if either the 9 or 10 pin is still connected. The performance parameters are potentially degraded.	C
	10		
EN	11	If the device is not intended to be disabled, the device does not power up.	B
MODE/SYNC	12	The device powers and operates either in FPWM or PFM mode.	B

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
CONF	1	VSET	There is a loss of functionality. There is the potential for wrong compensation, frequency, and SSC settings.	B
VSET	2	SW	The device powers up but potentially regulates to the wrong output voltage.	B
SW	3	PG	The device is potentially damaged.	A
	4			
PG	5	VOS	There is a loss of PG functionality.	B
VOS	6	AGND	There is no damage to the device, but the output voltage can be out of regulation.	B
AGND	7	PGND	The device powers up and performance parameters are potentially degraded.	C
PGND	8	VIN	The device does not power up.	B
	13			
VIN	9	EN	The device is always enabled.	B
	10			
EN	11	MODE/SYNC	The device always runs in FPWM mode.	B
MODE/SYNC	12	CONF	The device powers up and operates in either Auto or FPWM mode. There is the potential for wrong compensation, frequency, and SSC settings.	B

**Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class FSET
CONF	1	There is a loss of functionality. There is the potential for wrong compensation, frequency, and SSC settings.	B
VSET	2	The device powers up but potentially regulates to the wrong output voltage.	B
SW	3	The device is potentially damaged.	A
	4		
PG	5	The device is potentially damaged.	A
VOS	6	The output voltage can be out of regulation; the device is potentially damaged.	A
AGND	7	The device does not power up.	B
PGND	8	The device does not power up.	B
	13		
VIN	9	The device functions as intended.	D
	10		
EN	11	The device is always enabled, but there is a loss of functionality.	B
MODE/SYNC	12	The device always operates in automatic (auto) mode (PFM/PWM); rather than adjusting the mode to the correct setting.	B

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from November 4, 2025 to November 12, 2025 (from Revision \* (November 2025) to Revision A (November 2025))**

• Changed software to SW in the <i>Die Failure Modes and Distribution</i> table.....	<b>4</b>
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