Functional Safety Information

TCAN843-Q1 Functional Safety FIT Rate, FMD, and Pin FMA

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1 Overview

This document contains information for the TCAN843-Q1 to aid in a functional safety system design. This is a controller area network (CAN) transceiver in the D (SOIC, 14), DMT (VSON, 14), and DYY (SOT, 14) packages to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (FMA) for the device pins of TCAN843-Q1

Figure 1-1 shows the device functional block diagram for reference.

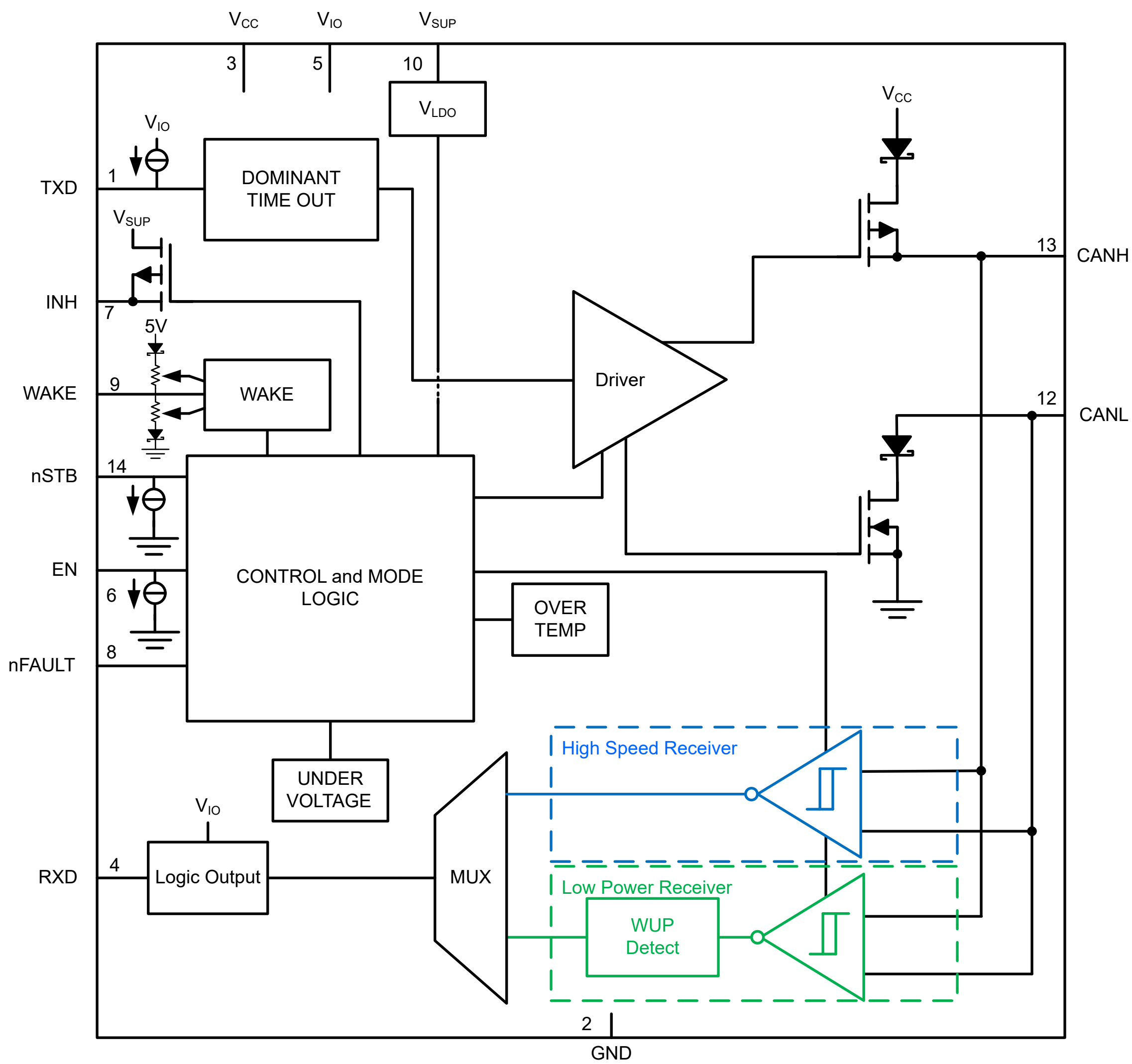

Figure 1-1. TCAN843-Q1 Functional Block Diagram

TCAN843-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TCAN843-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) 14-pin SOIC (D)	FIT (Failures Per 10^9 Hours) 14-pin VSON (DMT)	FIT (Failures Per 10^9 Hours) 14-pin SOT (DYY)
Total component FIT rate	19	9	8
Die FIT rate	4	3	4
Package FIT rate	15	6	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 151mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed ≤ 50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TCAN843-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Receiver fail	35
Transmitter fail	35
System stuck in sleep mode	15
Control and mode logic failure	10
CANL or CANH driver stuck dominant	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TCAN843-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to V_{CC} (see Table 4-5)
- Pin short-circuited to V_{SUP} (see Table 4-6)
- Pin short-circuited to V_{IO} (Table 4-7)

Table 4-2 through Table 4-7 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the D (SOIC, 14) pin diagram. Figure 4-2 shows the DMT (VSON, 14) pin diagram. Figure 4-3 shows the DYY (SOT, 14) pin diagram.

For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TCAN843-Q1 datasheet.

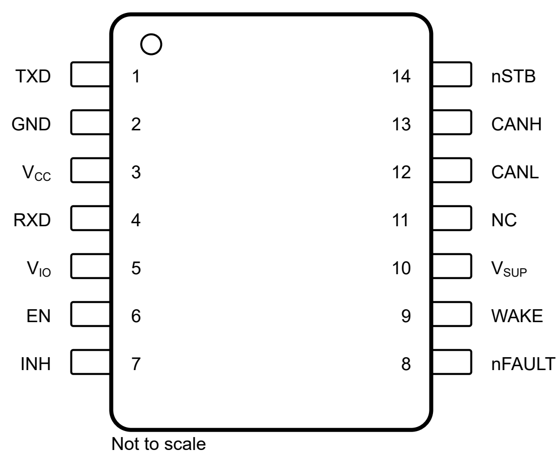

Figure 4-1. D (SOIC, 14) Pin Diagram

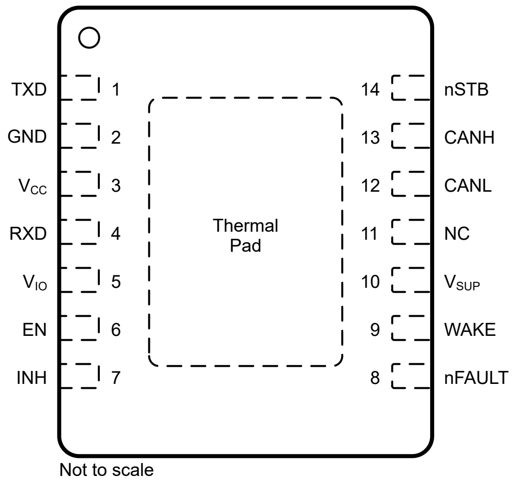

Figure 4-2. DMT (VSON, 14) Pin Diagram

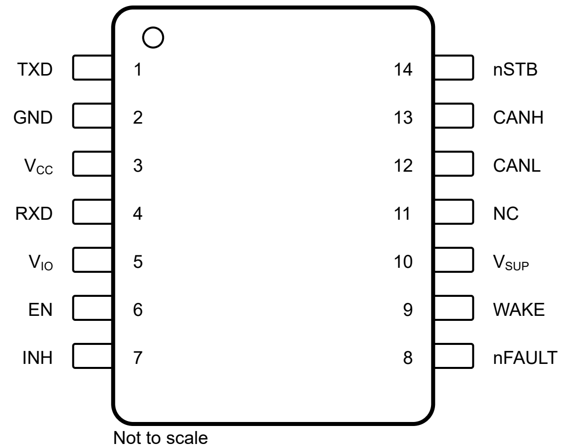

Figure 4-3. DYY (SOT, 14) Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- V_{CC} = 4.5V to 5.5V
- V_{SUP} = 4.5V to 28V
- V_{IO} = 2.9V to 5.5V

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	The TXD pin becomes biased dominant indefinitely. The device enters dominant time-out mode and is unable to transmit data.	B
GND	2	None.	D
V_{CC}	3	The CAN transmitter is not powered and the device enters sleep mode. There is a high current draw from the external regulator supplying to the V_{CC} pin.	B
RXD	4	The RXD output is biased recessive indefinitely. The host is unable to receive data from the bus.	B
V_{IO}	5	The device enters sleep mode. The transceiver is passive on the bus. There is a high current draw from the external regulator that supplies to V_{IO}.	B
EN	6	The EN pin becomes biased low. The device is not able to enter normal mode and is unable to communicate.	B
INH	7	High I_{SUP} current can occur. The INH pin can be damaged and indication from sleep mode transition is not available.	A
nFAULT	8	The nFAULT pin is biased low indefinitely, which indicates a fault indefinitely to the MCU.	B
WAKE	9	The WAKE pin is biased low indefinitely, and the device is not able to utilize the local wake-up function.	B
V_{SUP}	10	The device becomes unpowered. There is high current flowing from the source supplying to the V_{SUP} pin (battery) to ground.	B
NC	11	None.	D
CANL	12	The $V_{O(REC)}$ specification is violated, and EMC performance potentially degrades.	C
CANH	13	The device cannot drive the dominant bit to the bus, so communication is not possible.	B
nSTB	14	The nSTB pin becomes biased low indefinitely. The transceiver is unable to enter normal mode and is unable to communicate.	B
Thermal Pad	-	None.	D

Note

The VSON package includes a thermal pad.

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	The TXD pin defaults to a recessive bias. The driver is always recessive and the system is unable to transmit data.	B
GND	2	The device becomes unpowered.	B
V_{CC}	3	The CAN transmitter is not powered and the device enters sleep mode. There is a high current draw from the external regulator supplying to the V_{CC} pin.	B
RXD	4	The MCU is unable to receive data from the transceiver.	B
V_{IO}	5	The device enters protected mode.	B
EN	6	The EN pin defaults to a logic-low bias. The device is not able to enter normal mode and is unable to communicate.	B
INH	7	The system power control is potentially affected.	C
nFAULT	8	The MCU becomes unable to monitor faults in the system.	B
WAKE	9	The local wake-up function is not able to be used.	B
V_{SUP}	10	The device becomes unpowered.	B
NC	11	None.	D
CANL	12	The device cannot drive dominant on the bus and is unable to communicate.	B
CANH	13	The device cannot drive dominant on the bus and is unable to communicate.	B
nSTB	14	The nSTB defaults to a logic-low bias. The device is not able to enter normal mode and is unable to communicate.	B
Thermal Pad	-	None.	D

Note

The VSON package includes a thermal pad.

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
TXD	1	GND	The TXD pin is biased dominant indefinitely. The device enters dominant time-out mode and is unable to transmit data.	B
GND	2	V_{CC}	The CAN transmitter is not powered and the device enters sleep mode. There is a high current draw from the external regulator supplying to the V_{CC} pin.	B
V_{CC}	3	RXD	The RXD output becomes biased recessive indefinitely. The controller is unable to receive data from CAN bus.	B
RXD	4	V_{IO}	The RXD output becomes biased recessive indefinitely. The controller is unable to receive data from CAN bus.	B
V_{IO}	5	EN	The EN pin becomes biased high indefinitely. The device is unable to enter standby and silent mode.	B
EN	6	INH	There is an absolute maximum violation on the EN pin, except in sleep mode. The transceiver can be damaged.	A
nFAULT	8	WAKE	There is a potential absolute maximum violation on the nFAULT pin if WAKE is biased high. The transceiver can be damaged.	A
WAKE	9	V_{SUP}	The WAKE pin becomes biased high indefinitely. The local wake-up function is not able to be used.	B
V_{SUP}	10	NC	None.	D
NC	11	CANL	None.	D
CANL	12	CANH	The CAN bus becomes stuck recessive. Communication is not possible. I_{OS} current can be reached on the CANH or CANL pins.	B
CANH	13	nSTB	The driver and receiver turn off when the CAN bus is recessive. The device potentially does not enter normal mode.	B

Note

The VSON package includes a thermal pad. All device pins are adjacent to the thermal pad. The behavior of the device, when pins are shorted to the thermal pad, depends on the net that is connected to the thermal pad.

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{CC}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	The TXD pin becomes biased recessive indefinitely. The device is unable to transmit data.	B
GND	2	The CAN transmitter is not powered and the device enters sleep mode. There is a high current draw from the external regulator supplying to the V_{CC} pin.	B
V_{CC}	3	None.	D
RXD	4	The RXD output becomes biased recessive indefinitely. The controller is unable to receive data from CAN bus.	B
V_{IO}	5	The I/O pins operate as 5V inputs and outputs. The microcontroller can be damaged if $V_{CC} > V_{IO}$.	C
EN	6	The EN pin becomes biased high indefinitely. The device is unable to enter standby and silent mode.	B
INH	7	The INH pin is biased at V_{CC} voltage. The system potentially does not wake up. High current draw from the INH pin is possible.	B
nFAULT	8	The nFAULT pin becomes biased high indefinitely. The transceiver is unable to report faults.	B
WAKE	9	The local wake-up function is not able to be used.	B
V_{SUP}	10	The power rails of the system are short-circuited. Damage to the transceiver potentially occurs depending on the stronger power source if the absolute maximum rating of V_{CC} is exceeded.	A
NC	11	None.	D
CANL	12	I_{OS} current can be reached. The CAN bus can potentially become stuck recessive, and the device is unable to drive a dominant signal onto the bus.	B
CANH	13	The $V_{O(REC)}$ specification is violated, and EMC performance potentially degrades.	C
nSTB	14	The nSTB pin becomes biased high indefinitely. The transceiver is unable to enter standby and sleep mode.	B

Table 4-6. Pin FMA for Device Pins Short-Circuited to V_{SUP}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	An absolute maximum violation occurs and the transceiver can be damaged.	A
GND	2	The device becomes unpowered, and high I_{SUP} current potentially occurs.	B
V_{CC}	3	An absolute maximum violation occurs and the transceiver can be damaged.	A
RXD	4	An absolute maximum violation occurs and the transceiver can be damaged.	A
V_{IO}	5	An absolute maximum violation occurs and the transceiver can be damaged.	A
EN	6	An absolute maximum violation occurs and the transceiver can be damaged.	A
INH	7	The INH pin becomes stuck at the V_{SUP} level. The external regulator potentially does not enter low-power mode once the transceiver transitions to sleep mode.	D
nFAULT	8	An absolute maximum violation occurs and the transceiver can be damaged.	A
WAKE	9	The WAKE pin becomes biased high. The local wake-up function is not able to be used.	B
V_{SUP}	10	None.	D
NC	11	None.	D
CANL	12	I_{OS} current can be reached. The bus becomes stuck recessive, and communication is not possible.	B
CANH	13	The $V_{O(REC)}$ specification is violated, and EMC performance potentially degrades. There is an increased likelihood of communication errors on the CAN bus.	C
nSTB	14	An absolute maximum violation occurs and the transceiver can be damaged.	A

Table 4-7. Pin FMA for Device Pins Short-Circuited to V_{IO}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	The TXD pin becomes biased recessive indefinitely. The device is unable to transmit data.	B
GND	2	The device enters low-power mode. There is a high current draw from the external regulator supplying to the V_{IO} pin.	B
V_{CC}	3	If V_{IO} < UV_{CC}, an undervoltage condition potentially occurs on V_{CC}.	C
RXD	4	The RXD output becomes biased recessive indefinitely. The controller is unable to receive data from CAN bus.	B
V_{IO}	5	None.	D
EN	6	The EN pin becomes biased high indefinitely. The device is unable to enter standby and silent mode.	B
INH	7	The INH pin is biased at V_{IO} voltage. The system potentially does not wake up. High current draw from the INH pin is possible.	A
nFAULT	8	The nFAULT pin becomes biased high indefinitely. The transceiver is unable to report faults.	B
WAKE	9	The local wake-up function is not able to be used.	B
V_{SUP}	10	The power rails of the system are short-circuited. Damage to the transceiver potentially occurs, depending on the stronger power source, if the absolute maximum rating of V_{IO} is exceeded.	A
NC	11	None.	D
CANL	12	I_{OS} current can be reached. The CAN bus potentially becomes stuck recessive, and the device is unable to drive a dominant signal onto the bus.	B
CANH	13	The $V_{O(REC)}$ specification is violated, and EMC performance potentially degrades.	C
nSTB	14	The nSTB pin becomes biased high indefinitely. The transceiver is unable to enter standby and sleep mode.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release