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Matched-Filter Ultrasonic Sensing: Theory and Implementation

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This document provides a detailed discussion on the operating theory of the matched-filter based ultrasonic sensing technology and the single-chip implementation platform using the Texas Instruments (TI) MSP430FR6047 microcontroller (MCU).

Contents

List of Figures

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1 Introduction

Ultrasonic sensing uses the propagation of acoustic energy at ultrasonic frequencies to extract information from the environment. The primary parameter to measure is the time of flight (TOF) of the received signal. In Figure 1, the sonar transmitter sends out a pulse to the target to be detected. In this case, the time of flight is the round trip way time delay of the signal reflected from the target.

In Figure 1, R is the range of the target, C is the sound propagation speed, and T is the round-trip time of flight (TOF) of the signal reflected from the target.

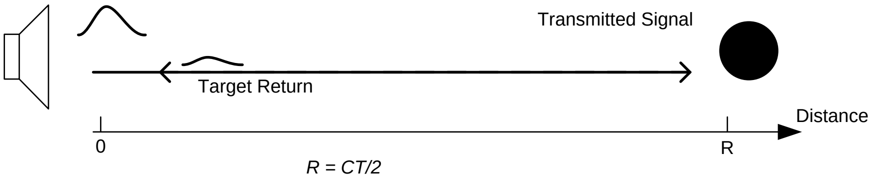

Figure 1. Sonar in Target Range Measurement

The most important parameter for the performance of an ultrasonic sensing is the accuracy of the TOF measurement. The accuracy of TOF is directly related to the signal-to-noise ratio of the received signal. Matched filtering is a digital signal processing technique developed to improve the signal-to-noise ratio of the received signal. This document provides an overview discussion of the use of matched filtering in ultrasonic sensing and the single-chip ultrasonic sensing solution using the TI MSP430FR6047 MCU.

2 Theory of Matched Filtering

In addition to the TOF accuracy requirement, many radar and sonar systems are also required to detect multiple targets separated by short distances. A fine TOF resolution requires short pulse width, which indicates high bandwidth of the transmitter and receiver. High receive signal-to-noise ratio also requires higher transmitting power. The operating bandwidth and transmitting power of sonar are often severely limited in the real world.

Pulse compression is a technique that helps overcome these limitations. In pulse compression, the transmitted pulse is modulated by a specific phase or frequency pattern during a wider pulse interval. The receiver uses a pulse-matched filter to pass reflected pulses that match the pattern of the outgoing pulse and reject noise and other signals. Because the transmitted pulse is wider, a transmitter with lower peak output power can deliver the same amount of transmitted pulse energy to maintain range accuracy performance. The compressed narrow pulse enables finer range resolution. Figure 2 shows the concept of pulse compression.

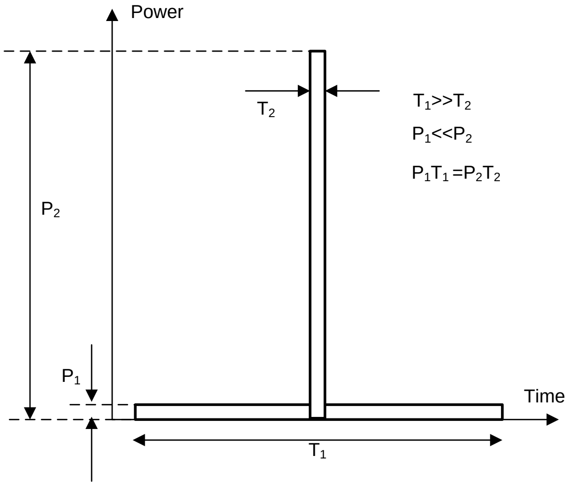

Figure 2. Concept of Pulse Compression

Assume that the transmission signal is denoted as $S_T(t)$ and the received signal as $S_R(t)$. $S_T(t)$ and $S_R(t)$ are related by Equation 1.

$$S_R(t) = H_{path} S_T(t - \tau) + n(t) \tag{1}$$

Where τ is the TOF of the received signal. H_{path} is the transfer function of the signal propagation path including amplitude attenuation. H_{path} is not a time-variant function. $n(t)$ is the noise introduced in the signal propagation path. $S_T(t)$ and $n(t)$ are not statistically correlated.

The output of the receiver filter $h_{rec}(t)$ can be expressed as Equation 2.

$$S_O(t) = h_{rec}(t) \times S_R(t) = h_{rec}(t) \times (H_{path} S_T(t - \tau) + n(t)) \tag{2}$$

If the receive filter $h_{rec}(t)$ matches the transmitted signal $S_T(t)$, then:

$$S_O(t) = h_{rec}(t) \times S_R(t) = KS_T(t) \times H_{path} S_T(t - \tau) + KS_T(t) \times n(t) \tag{3}$$

The signal component is the first item in Equation 3. It is actually the autocorrelation of the transmission signal pattern.

$$S_O(t) = h_{rec}(t) \times S_R(t) = KH_{path} CORR_{ST} + KS_T(t) \times n(t) \tag{4}$$

When the timing of the receive filter matches the received signal, the autocorrelation summarizes all the signal energy transmitted over the transmission period of time to maximize the signal to noise ratio in the output. The matched filter got its name because it uses a known signal pattern to detect the presence of the same pattern in the received signal.

Because the matched filter is the optimal linear filter for maximizing the signal-to-noise ratio in the presence of additive noise, it has been widely used in radar, sonar, and communication applications. Mathematicians have conducted extensive research to find waveforms with autocorrelation function close to a δ function, not only to maximize the signal-to-noise ratio but also to be able to detect the presence of multiple TOFs. In radar and sonar applications, this means the ability to detect targets separated by short distances.

One popular form of pulse compression modulation is the linear frequency sweep, or chirp. Figure 3 shows the waveform of a chirp pulse.

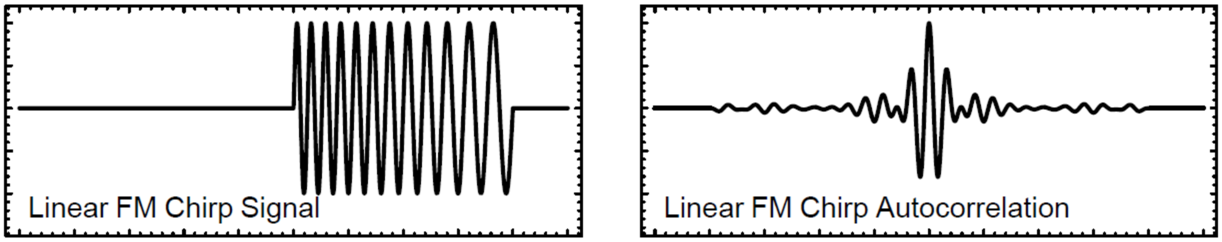

Figure 3. Time-Domain Waveform and Autocorrelation of FM Chirp

In general, the width of the autocorrelation peak is inversely proportional to the bandwidth of the transmission signal. Wide-band transmitters and receivers are required for detecting nearby TOFs.

In many ultrasonic sensing applications, such as flow meters and liquid level sensing, only one TOF measurement is needed. To use the narrow-band ceramic ultrasonic transducer, the square wave waveform in Figure 4 is often used. When driving a narrow-band ceramic ultrasonic transducer, the frequency of the driving square wave must match the resonant frequency of the ceramic transducer.

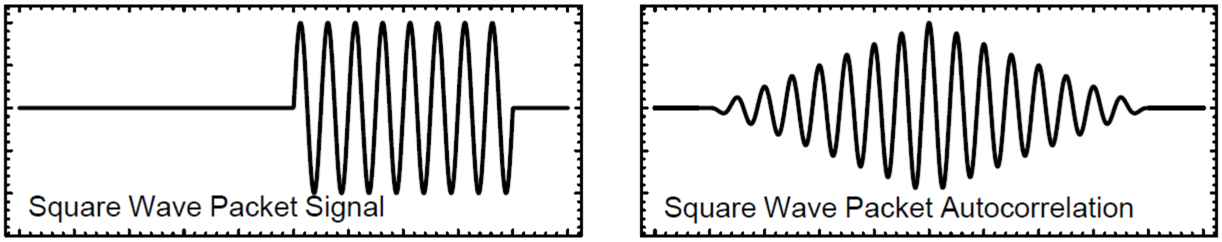

Figure 4. Time-Domain Waveform and Autocorrelation of Square-Wave Pulses

Figure 5 shows the functional block diagram of a matched-filter based system. Typically, the system designer must choose a reference signal pattern to modulate the output. The same signal pattern is also used in the matched filter for the detection of the target return. In some flow meter applications, the upstream and downstream measurement data are correlated to find the difference in TOF. The differential TOF can be used for the calculation of the flow speed of liquid or gas.

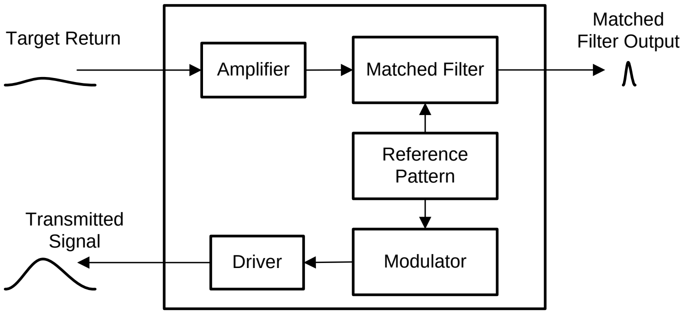

Figure 5. Block Diagram of Matched-Filter-Based Sensing System

Figure 6 shows the signal processing steps involved in a matched filter receiver.

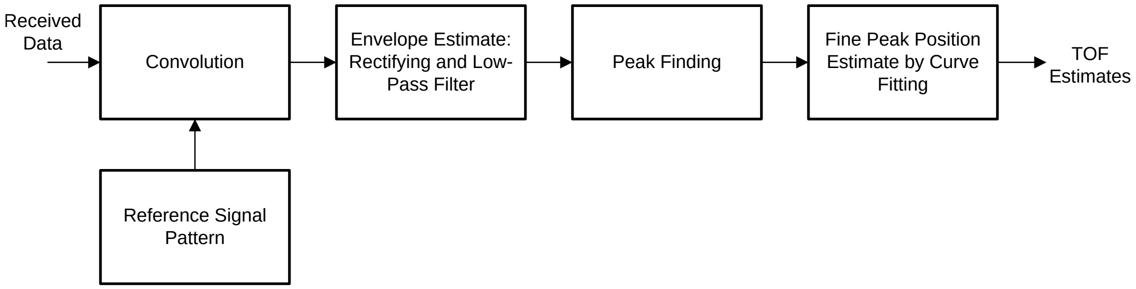

Figure 6. Signal Processing Flow of Matched-Filter Receiver

The following sections discuss how to realize the functional blocks in Figure 5 and Figure 6 on the MSP430FR6047 MCU.

3 MSP430FR6047 for Ultrasonic Sensing

Figure 7 shows the functional modules on the MSP430FR6047 MCU. The integration of the Ultrasonic Sensing Solution (USS) subsystem and the Low-Energy Accelerator (LEA) module provide necessary features to enable a single-chip solution for ultrasonic sensing.

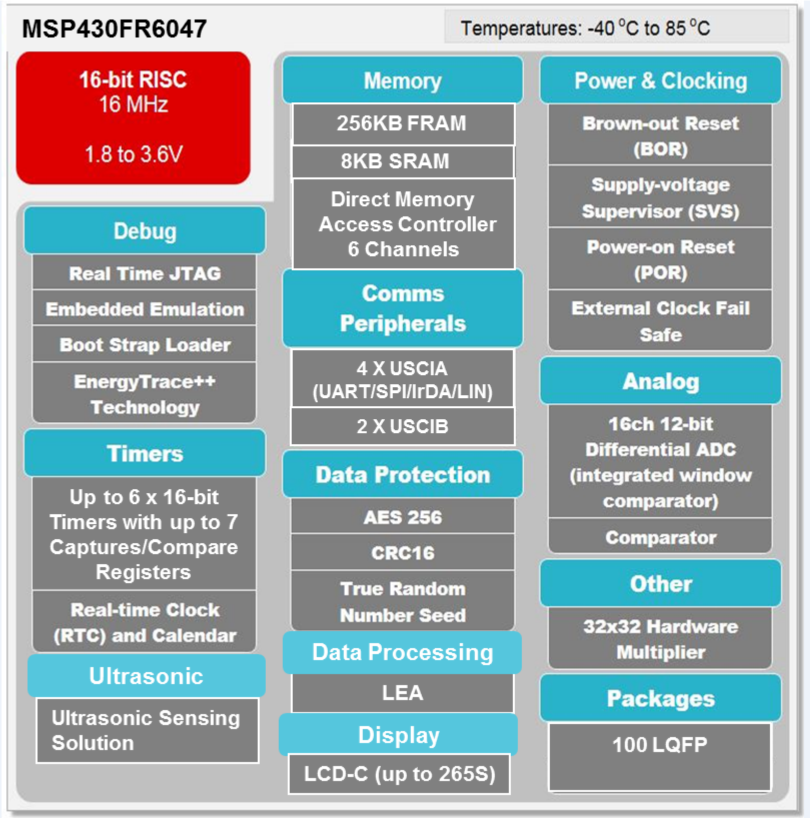

Figure 7. Functional Modules in MSP430FR6047

Figure 8 shows a functional block diagram for a MSP430FR6047-based single-chip flow meter.

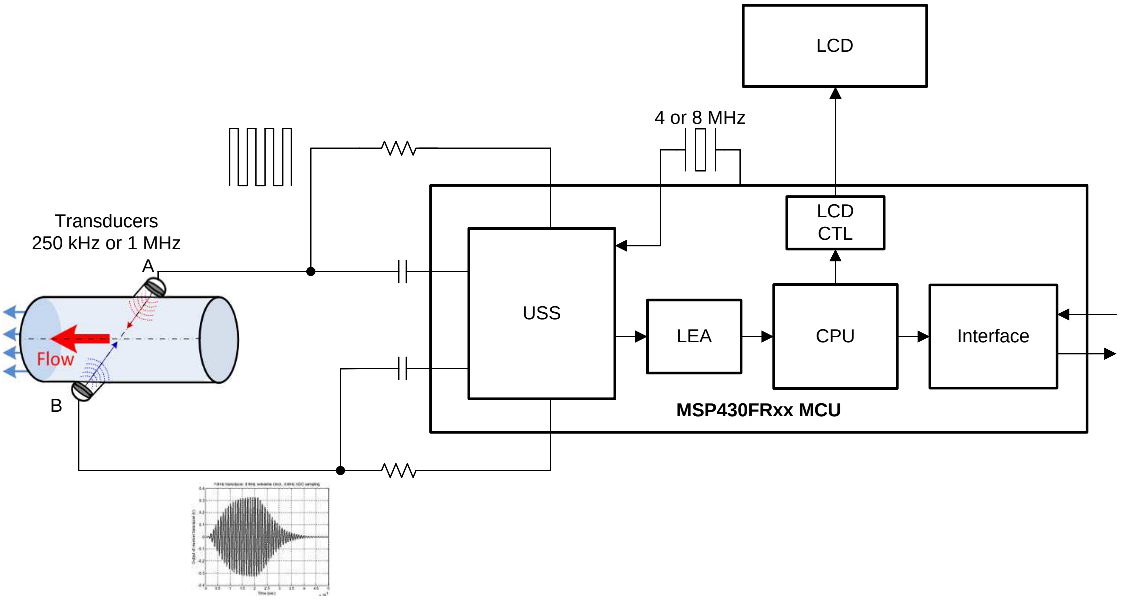

Figure 8. MSP430FR6047-Based Single-Chip Flow Meter

In Figure 8, the USS subsystem performs the following tasks:

1. Generate the excitation pulses and drive the transmitting ultrasonic transducer.
2. Amplify and filter the signal from the receiving ultrasonic transducer.
3. Convert the electrical signal to digital data stream.
4. Move the converted data into system memory for LEA.
5. Notify CPU for data readiness.

The LEA is a math coprocessor especially designed for vector type operations such as FIR filtering and FFT. The convolution calculation in matched filter is the same as FIR with the reference signal patterns as the filter coefficients. The LEA also offers functions like peak finding which can be used in TOF estimation.

More details about the functionalities provided by USS and the LEA module are in the following sections.

4 MSP430FR6047 USS Subsystem

The USS subsystem is designed to provide a high-precision ultrasonic sensing solution. Figure 9 shows the functional block diagram.

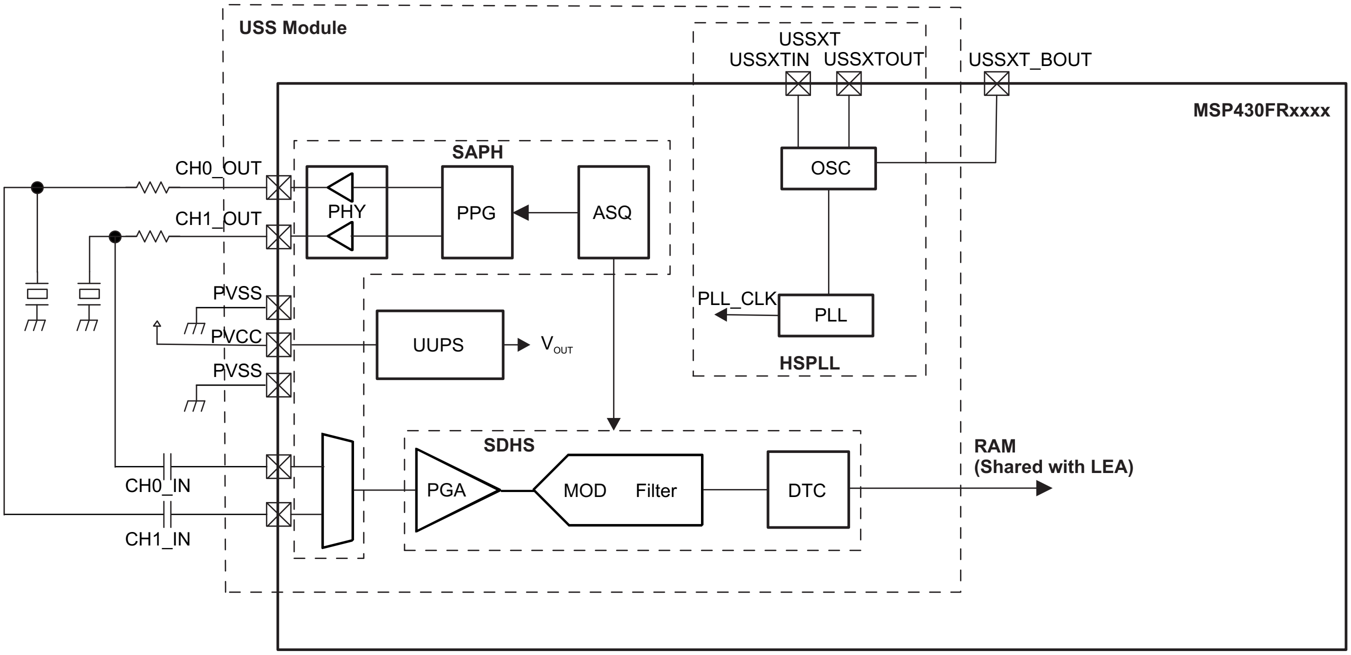

Figure 9. USS Functional Block Diagram

The USS is a sophisticated system consisting of four functional modules:

- UUPS (Universal USS Power Supply)
- HSPLL (High-Speed PLL)
- SAPH (Sequencer for Acquisition, Programmable Pulse Generator, and Physical Interface)
- SDHS (Sigma-Delta High Speed).

The UUPS module is responsible for power on and off the USS subsystem. The power sequencer (PSQ) block in UUPS can be set up to start the USS power on sequence upon the trigger from timers or CPU, and enable other USS modules when the power state is stable.

The HSPLL module generates the high-speed clock (from 68 MHz to 80 MHz) from an external crystal (4 to 8 MHz). This high-speed clock is used by the sigma-delta ADC in SDHS module and the ASQ (Acquisition Sequencer) and PPG (Programmable Pulse Generator) blocks in the SAPH module.

The SDHS module consists of a programmable gain amplifier (PGA) for the amplification of the received signal, a high speed 12 bit sigma-delta analog-to-digital converter (ADC), and a digital transfer controller (DTC) for moving ADC output data to system memory. The gain of the PGA is adjustable from –6.5 dB to 30.8 dB. The ADC can run up to 8 million samples per second (Msps). DTC is faster enough to move the high speed ADC data to LEA RAM in time. The address in LEA RAM for DTC to move data is programmable. During DTC transfer, no other bus masters can access LEA RAM.

The SAPH module consists of three blocks: Acquisition Sequencer (ASQ), Programmable Pulse Generator (PPG), and Physical Interface (PHY).

The PPG block generates excitation pulses. The frequency and length of the pulse chain is programmable. The input clock to PPG is HPLL/4. On MSP430FR6047, the frequency of the pulses cannot be dynamically changed. It only supports the square wave waveform in Section 2. The square wave is adequate for the utilization on the narrow band ceramic ultrasonic transducers. In the next generation of PPG, the period of the pulses can be changed dynamically. The new feature will enable many new ultrasonic sensing applications with wide-band transducers.

The PHY block controls output drivers to output the excitation pulses to the transmit transducer. There are two output channels. The output channels can be set to one of four modes: single ended output, differential output, high impedance, and ground. The output driver strength is also programmable. The PHY block also controls the input multiplexer for routing the correct receiving transducer to the SDHC PGA. There are two input channels. The user can program the input multiplexer to connect PGA to the desired input channel. The source of bias to PGA is also programmable.

The ASQ controls the entire measurement sequence without CPU intervention. CPU can stay in low power mode LPM0 during the measurement sequences. The timer in ASQ can be programed to produce 6 time mark events. Those time mark events trigger the measurement tasks such as the start of excitation pulses, turn on the ADC, apply the PGA bias, and start of analog-to-digital conversion. The input to the ASQ timer is the HPLL clock divided by 16.

Figure 10 shows the flow of USS measurement.

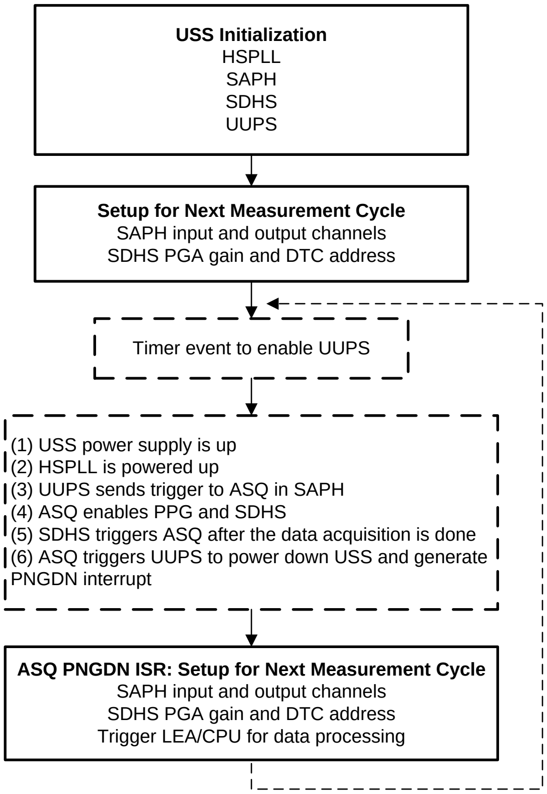

Figure 10. Flow of USS Measurement

The USS subsystem must be initialized after a system reset or waking from a low-power mode. The USS initialization includes the following tasks.

1. Set up HSPLL to output at a specified frequency.
2. Set up SAPH PPG block for the high/low time and the number of the pulses for the excitation pulses.
3. Set up SAPH bias and trimming registers for the input and output channels.
4. Set up SAPH ASQ time mark events for timings of generating excitation pulses, turning on SDHS module, applying the receive bias, and starting analog-to-digital sampling.
5. Set up SAPH ASQ to be triggered by UUPS PSQ block
6. Set up SAPH ASQ to accept analog-to-digital conversion completion signal from SDHS and generate trigger to UUPS PSQ to turn off USS power.
7. Set up SAPH ASQ to generate interrupt after receiving analog-to-digital conversion completion signal from SDHS.
8. Set up SDHS ADC to the requirement frequency and data format.
9. Set up SDHS ADC to be triggered by SAPH ASQ.
10. Set up the number of sample to be converted by SDHS ADC. SDHS will trigger ASQ after all samples are converted.
11. Set up the UUPS module to be enabled by timer or CPU
12. Set up UUPS to enable SAPH ASQ and HSPLL after the USS power supply is stabilized.

After the USS initialization, the SAPH input and output channels, the SDHA PGA gain, and the start address for DTC transfer needs to be configured for each USS measurement cycle. DTC needs to be enabled for moving analog-to-digital data from ADC to the LEA RAM used by the LEA module. User needs to make sure that no other bus masters should access this RAM when DTC transfer is in progress.

A USS measurement cycle starts after the UUPS module is triggered by a timer or CPU. Then the entire measurement cycle is controlled by the SAPH ASQ block. The tasks in the dashed block are automatically performed by USS without CPU intervention. When all the samples are moved to the RAM, ASQ generates an interrupt. In Figure 10, the parameters for next measurement cycle are configured in the interrupt routine. The user can also set up a flag in the interrupt routine and perform the processing in the main loop.

5 MSP430FR6047 Low Energy Accelerator (LEA)

The low-energy accelerator (LEA) is a TI proprietary accelerator designed to efficiently perform vector based arithmetic and signal conditioning. The LEA can perform an equivalent operation as a traditional MCU could but with much more efficiency and lower energy. LEA supports 16-bit and 32-bit fixed-point math operations. The popular algorithms supported by LEA include FFT, FIR, IIR, matrix, and vector multiply, addition, and subtraction. Table 1 compares the performance in calculating FFT between LEA and some CPU cores. An Arm® Cortex®-M4F CPU would need to run at a clock speed 3 times faster than the LEA to complete the task in the same time. Therefore, the Cortex-M4F CPU would use 3 times the energy, compared to the LEA, to complete the FFT calculation.

Table 1. FFT Performance Comparison

16-Bit Complex FFT (size)	MSP430™ With DSP Library (cycles)	MSP430 With LEA Enabled (cycles)	Cortex-M0 (cycles)	Cortex-M3 (cycles)	Cortex-M4F (cycles)
128	34960	3060	94805	22185	9377
256	80736	5750	223360	45630	17147
512	183152	11537	475920	110971	45558

The LEA operates independent of the CPU but requires the system clock. CPU can be asleep in the low-power mode 0 (LPM0) with the system clock active, or the CPU can execute concurrently while the LEA executes. The LEA uses shared SRAM (LEA RAM) and can access RAM at up to 16 MHz with 0 wait-states. The LEA consumes approximately 67 µA/MHz.

Figure 11 shows the LEA operation.

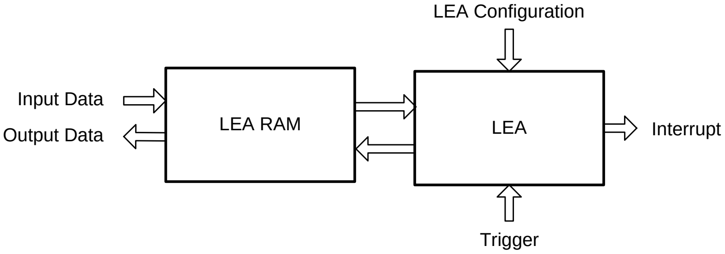

Figure 11. LEA Operation

The use of the LEA takes the following steps.

1. Configure the LEA control registers with the ID of the algorithm, the size of the data, and the addresses of the input and output data in the LEA RAM.
2. Use the DMA, CPU, or DTC to move input data to the LEA RAM.
3. Use CPU or peripheral to generate the trigger to start LEA operation.
4. The LEA generates an interrupt signal when the operation is complete. The CPU or DMA can be used to read the output data from the LEA RAM.

The user can also use the MSP DSP Library functions for LEA included in the MSPware software without detailed knowledge of the LEA.

The primary use of the LEA in ultrasonic sensing is to calculate the convolution in matched filtering. The LEA FIR function can be directly used using the reference signal pattern as the filter coefficients. When the size of the input data is large, the user may want to consider using FFT and IFFT in convolution calculation. More details about using FFT and IFFT for convolution calculation can be found in *Convolution and Deconvolution Using the FFT*. The LEA also has functions useful for constructing the envelope, finding the peak, and curve fitting to estimate fine peak location. For operation details of the USS and LEA modules, see the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide*.

6 References

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