Application Note

MSPM0 C-Series MCU Hardware Development Guide

MSP APP

ABSTRACT

The MSPM0 C-series microcontroller (MCU) portfolio offers a wide variety of low cost 32-bit MCUs with ultra-low-power and integrated analog and digital peripherals for sensing, measurement and control applications. This application note covers information needed for hardware development with MSPM0 C-series MCUs, including detailed hardware design information for power supplies, reset circuitry, clocks, debugger connections, key analog peripherals, communication interfaces, GPIOs, and board layout guidance.

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Trademarks

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1 MSPM0C Hardware Design Check List

Table 1-1 describes the main signal that needs to be checked during the MSPM0C hardware design process. The following sections provide more details.

Table 1-1. MSPM0C Hardware Design Check List

Pin (1)	Description	Requirements
VDD	Power supply positive pin	Place 10-µF and 100-nF capacitors between VDD and VSS, and keep those part close to VDD and VSS.
VSS	Power supply negative pin	
NRST	Reset pin	Connect an external 47-kΩ pullup resistor with a 10-nF pulldown capacitor.
SWCLK	Serial wire clock from debug probe	Internal pulldown to VDD, does not need any external part.
SWDIO	Bidirectional (shared) serial wire data	Internal pullup to VSS, does not need any external part.
PA0, PA1	Open-drain I/O	Pull-up resistor required for output high
PAx (exclude PA0, PA1)	General-purpose I/O	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with internal pullup or pulldown resistor.

(1) For any unused pin with a function that is shared with general-purpose I/O, follow the Section 8.5.

TI recommends connecting a combination of a 10-µF and a 0.1-nF low-ESR ceramic decoupling capacitor to the VDD and VSS pins. Higher-value capacitors can be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the decoupled pins (within a few millimeters).

The NRST reset pin is required to connect an external 47-kΩ pullup resistor with a 10-nF pulldown capacitor.

For 5-V-tolerant open drain (ODIO), a pullup resistor is required to output high, this is required for inter-integrated circuit (I2C) and universal asynchronous receiver/transmitter (UART) functions if the ODIO are used.

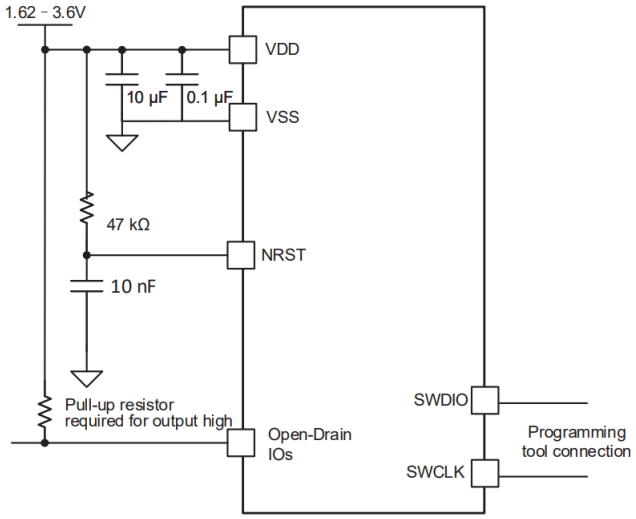

Figure 1-1. MSPM0C Typical Application Schematic

2 Power Supplies in MSPM0C Devices

Power is supplied to the device through the VDD and VSS connections. The device supports operation with a supply voltage of 1.62 V to 3.6 V and can start with a 1.62-V supply. The power management unit (PMU) generates the regulated core supplies for the device and provides supervision of the external supply. It also contains a bandgap voltage reference used by the PMU and other analog peripherals. VDD is used directly to provide the IO supply (VDDIO) and the analog supply (VDDA). VDDIO and VDDA are internally connected to VDD so that additional power supply pins are not required (see the device-specific data sheet for details).

2.1 Digital Power Supply

Core Regulator

There is an internal low-dropout linear voltage regulator to generate a 1.35-V supply rail to power the device core. The core regulator is active in all power modes except for SHUTDOWN. In all other power modes (RUN, SLEEP, STOP, and STANDBY) the drive strength of the regulator is configured automatically to support the max load current of each mode. This reduces the quiescent current of the regulator when using low power modes, improving low power performance.

2.2 Analog Power Supply

Bandgap Voltage Reference

The PMU provides a temperature and supply voltage stable bandgap voltage reference which is used by the device for internal functions, including:

- Driving the brownout reset circuit thresholds.
- Supporting the core regulator.
- Driving the on-chip VREF levels for on-chip analog peripherals.

The bandgap reference is enabled in RUN, SLEEP, and STOP modes. Bandgap voltage operates in a sampled mode in STANDBY to reduce power consumption, and is disabled in SHUTDOWN mode. SYSCTL manages the bandgap state automatically, no user configuration is required.

2.3 Built-in Power Supply and Voltage Reference

The VREF module for the MSPM0 C family is a shared voltage reference module which can be leveraged by a variety on on-board analog peripherals.

The VREF module features include:

- 1.4-V and 2.5-V user-selectable internal references.
- Sample and hold mode support VREF operation down to STANDBY operating mode.
- Internal reference supports for ADC.

2.4 Recommended Decoupling Circuit for Power Supply

A combination of a 10-µF plus a 100-nF low-ESR ceramic decoupling capacitor is recommended to connect to the DVCC pin (see Figure 2-1). Higher-value capacitors can be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the decoupled pins (within a few millimeters).

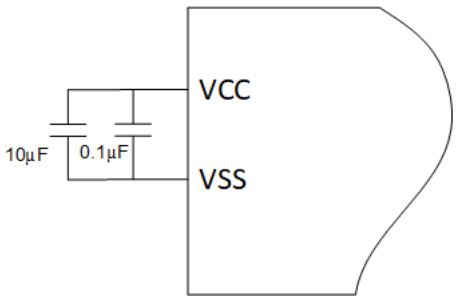

Figure 2-1. Power Supply Decoupling Circuit

3 Reset and Power Supply Supervisor

3.1 Digital Power Supply

The device has five reset levels:

- Power-on reset (POR)
- Brown-out reset (BOR)
- Boot reset (BOOTRST)
- System reset (SYSRST)
- CPU reset (CPURST)

The details of the relationships between reset levels is described in the MSPM0 C-Series 24-MHz Microcontrollers Technical Reference Manual.

After a cold start, the NRST pin is configured in NRST mode. The NRST pin must be high for the device to boot successfully. There is no internal pullup resistor on NRST. External circuitry (either a pullup resistor to DVCC or a reset control circuit) must actively pull NRST high for the device to start. A capacitor and an open button are needed for manual reset (see Figure 3-1). After the device is started, a low pulse on NRST that is <1 second in duration triggers a BOOTRST. If a low pulse on NRST is held for >1 second, a POR is triggered.

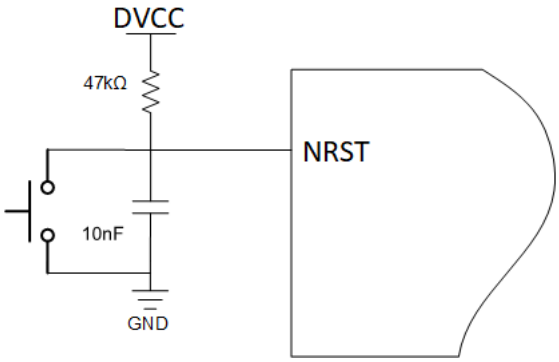

Figure 3-1. NRST Recommended Circuit

3.2 Power Supply Supervisor

3.2.1 Power-On Reset (POR) Monitor

The power-on reset (POR) monitor supervises the external supply (VDD) and asserts or de-asserts a POR violation to SYSCTL. During cold power-up, the device is held in a POR state until VDD passes the POR+. Once VDD has passed POR+, the POR state is released and the bandgap reference and BOR monitor circuit are started. If VDD drops below the POR- level, then a POR- violation is asserted and the device is again held in a POR reset state.

The POR monitor does not indicate that VDD has reached a level high enough to support correct operation of the device. Rather, it is the first step in the boot process and is used to determine if the supply voltage is sufficient to power up the bandgap reference and BOR circuit, which are then used to determine if the supply has reached a level sufficient to for the device to run correctly. The POR monitor is active in all power modes including SHUTDOWN, and cannot be disabled. (The POR triggered waveform is shown in Section 3.2.3).

3.2.2 Brownout Reset (BOR) Monitor

The brown-out reset (BOR) monitor supervises the external supply (VDD) and asserts or de-asserts a BOR violation to SYSCTL. The primary responsibility of the BOR circuit is to ensure that the external supply is maintained high enough to enable correct operation of internal circuits, including the core regulator. The BOR threshold reference is derived from the internal bandgap circuit. The threshold itself is programmable and is always higher than the POR threshold. During cold start, after VDD passes the POR+ threshold the bandgap reference and BOR circuit are started. The device is then held in a BOR state until VDD passes the BOR0+ threshold. Once VDD passes BOR0+, the BOR monitor releases the device to continue the boot process, and the PMU is started. (The BOR triggered waveform is shown in Section 3.2.3).

3.2.3 POR and BOR Behavior During Supply Changes

When the supply voltage (VDD) drops below POR-, the entire device state is cleared. Small variations in VDD which do not pass below the BOR0- threshold do not cause a BOR- violation, and the device will continue to run. Behavior for BORx thresholds other than BOR0 (for example, BOR1-BOR3) is the same as is shown for BOR0, except that the BOR circuit is configured to generate an interrupt rather than immediately triggering a BOR reset.

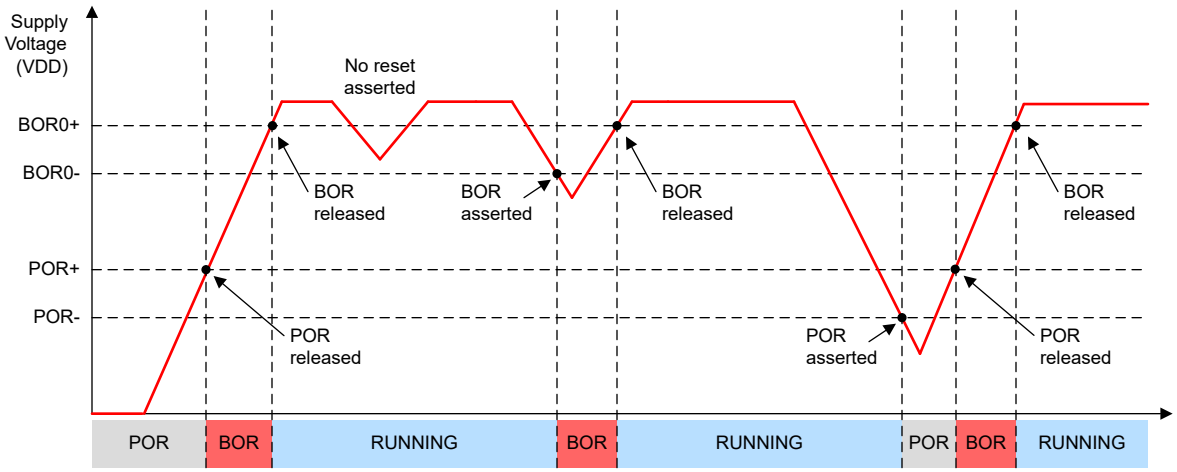

Figure 3-2. POR/BOR vs. Supply Voltage (VDD)

4 Clock System

The clock system of MSPM0C series contains the internal oscillators, the clock monitors, and the clock selection and control logic. A frequency clock counter is also provided for checking and/or calibrating the frenquency of high-speed clocks against a reference period/pluse provided on an IO pin. This section describes the clock resources on different MSPM0C family devices and their interaction with external signals or devices.

4.1 Internal Oscillators

4.1.1 Internal Low-Frequency Oscillator (LFOSC)

LFOSC is an on-chip low power oscillator that is factory trimmed to a frequency of 32.768 kHz. It provides a low-frequency clock that can be used to help the system achieve low-power. LFOSC can provide higher accuracy when used over a reduced temperature range. See the device-specific data sheet for details.

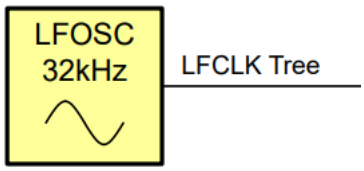

Figure 4-1. MSPM0C Series LFOSC

4.1.2 Internal System Oscillator (SYSOSC)

SYSOSC is an on-chip, accurate, and configurable oscillator with factory-trimmed frequencies of 24 MHz (base frequency). It provides a high-frequency clock that lets the CPU run at high speed for executing code and processing performance.

SYSOSC Frequency Correction Loop

The overall SYSOSC application accuracy is determined by whether the internal ROSC resistor is used and the temperature. The SYSOSC circuit error in FCL mode is ±0.49% for 25°C, ±0.86% for -40°C to 85°C, ±0.95% for -40°C to 105°C, and ±1.05% for -40°C to 125°C)

4.2 External Clock Input (xFCLK_IN)

MSPM0C series support to use external digital clock input via LFCLK_IN and HFCLK_IN Pin.

4.2.1 LFCLK_IN

To configure LFCLK to use a digital clock input, first configure the IOMUX to enable the LFCLK_IN function on the appropriate pin. When IOMUX is configured correctly and the external clock source is outputting a 32 kHz clock to LFCLK_IN, set the SETUSEEXLF bit in the EXLFCTL register in SYSCTL.

LFCLK_IN is compatible with digital square wave CMOS clock inputs and a typical duty cycle of 50% is recommanded. Check for a valid clock signal on LFCLK_IN by enabling the LFCLK monitor before setting SETUSEEXLF in the EXLFCTL register is recommanded. By default, the LFCLK monitor will check LFCLK_IN if the LFXT was not started.

Once LFCLK_IN is selected as the LFCLK source, change back to LFOSC or LFXT without going through a BOOTRST is not possible.

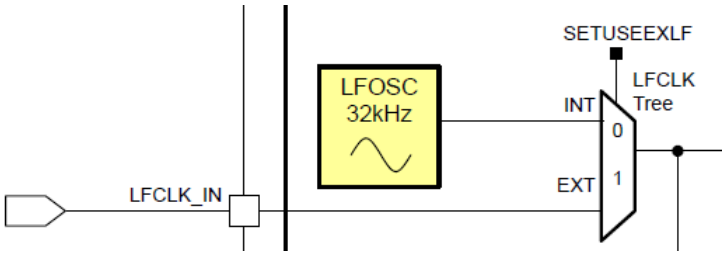

Figure 4-2. MSPM0C Series External Clock Input LFCLK_IN

4.2.2 HFCLK_IN

To configure HFCLK to use a digital clock input, first configure the IOMUX to enable the HFCLK_IN function on the appropriate pin. When IOMUX is configured correctly and the clock source is outputting a clock to HFCLK_IN, set the USEEXTHFCLK bit in the HSCLKEN register in SYSCTL.

To source MCLK from HFCLK_IN after selecting HFCLK_IN as the HFCLK source, first set the HSCLKSEL bit in the HSCLKCFG register to select HFCLK as the high-speed clock source. Then, set the USEHSCLK bit in the MCLKCFG register to select the high-speed clock source as the MCLK source. Once USEHSCLK is set, HSCLKCFG must not change and the HFCLK_IN must not be disabled until the MCLK source is switched back to SYSOSC by clearing USEHSCLK and verifying that the HSCLKMUX bit in CLKSTATUS was cleared by hardware.

HFCLK_IN is compatible with digital square wave CMOS clock inputs and a typical duty cycle of 50% is recommanded.

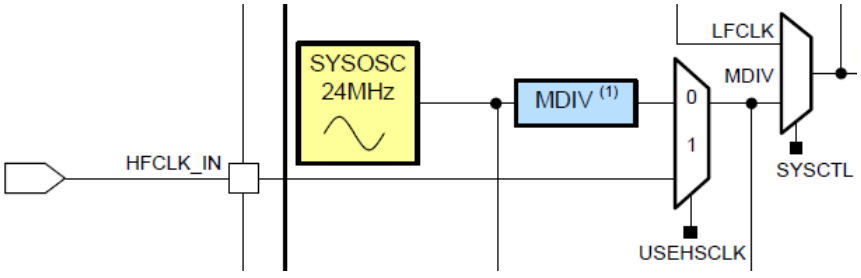

Figure 4-3. MSPM0C Series External Clock Input HFCLK_IN

4.3 External Clock Output (CLK_OUT)

A clock output unit is provided for pushing out digital clocks from the device to external circuits or to the frequency clock counter. This feature is useful for clocking external circuitry such as an external ADC that does not have its own clock source. The clock output unit has a flexible set of sources to select from and includes a programmable divider.

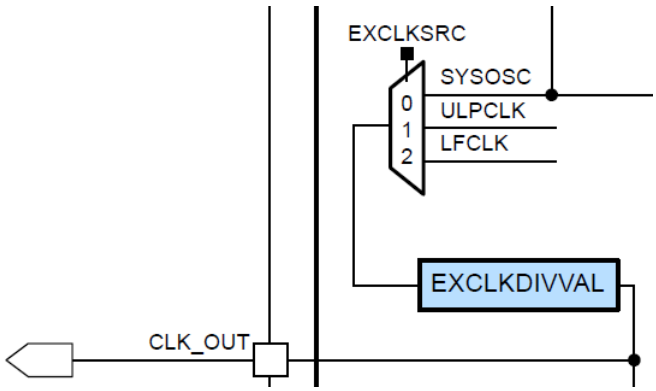

Figure 4-4. MSPM0C Series External Clock Output

Available clock sources for CLK_OUT:

- SYSOSC
- ULPCLK
- LFCLK

The selected clock source is divided by 2, 4, 6, 8, 10, 12, 14, or 16 before being output to the pin or to the frequency clock counter.

4.4 Frequency Clock Counter (FCC)

The frequency clock counter (FCC) enables flexible in-system testing and calibration of a variety of oscillators and clocks on the device. The FCC counts the number of clock periods seen on the selected source clock within a known fixed trigger period (derived from a secondary reference source) to provide an estimation of the frequency of the source clock.

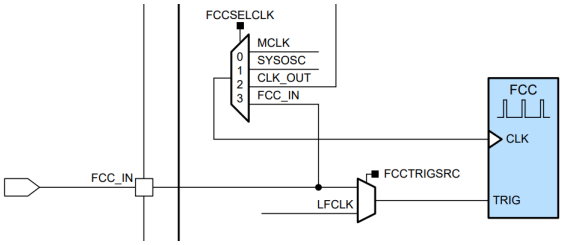

Figure 4-5. MSPM0C Series Frequency Clock Counter Block Diagram

Application software can use the FCC to measure the frequency of the following oscillators and clocks:

- MCLK
- SYSOSC
- CLK_OUT
- The external FCC input (FCC_IN)

Note

While the external FCC input (FCC_IN function) can be used as either the FCC clock source or the FCC trigger input, it cannot be used for both functions during the same FCC capture. It must be configured as either the FCC clock source or the FCC trigger.

5 Debugger

The debug sub system (DEBUGSS) interfaces the serial wire debug (SWD) two-wire physical interface to multiple debug functions within the device. MSPM0C devices support debugging of processor execution, the device state, and the power state (using EnergyTrace technology).

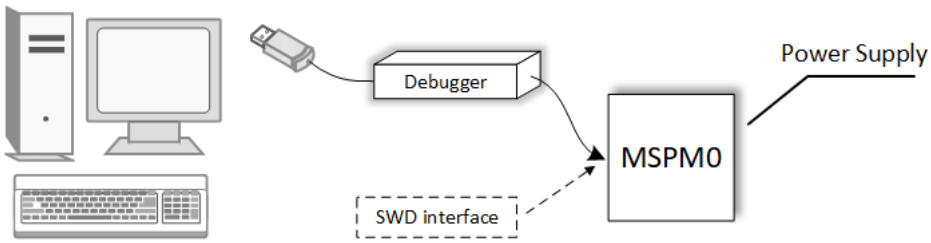

Figure 5-1. Host to Target Device Connection

5.1 Debug Port Pins and Pinout

The debug port contains SWCLK and SWDIO (see Table 5-1) which have internal pull-down and pull-up resistors (see Figure 5-2). The MSPM0L MCU family is offered in various packages with different numbers of available pins. Refer to the device-specific data sheet for details.

Table 5-1. MSPM0C Debug Ports

Device Signal	Direction	SWD Function
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

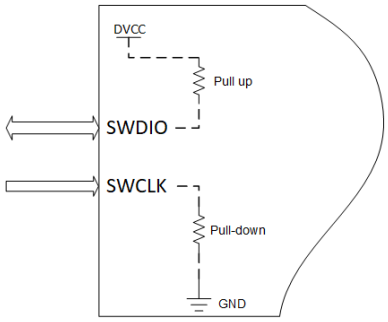

Figure 5-2. MSPM0C SWD Internal Pull

5.2 Debug Port Connection With Standard JTAG Connector

Figure 5-3 shows the connection between MSPM0C family MCU SWD debug port with the standard JTAG interface.

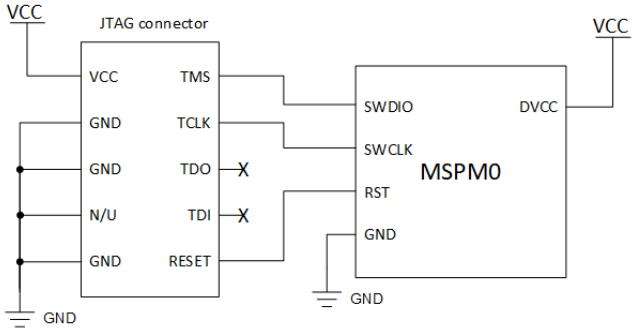

Figure 5-3. JTAG and MSPM0C Connection

For MSPM0C device, you can use XDS110 to implement debug/download function. Here list the contents of the XDS110 and provides instruction on installing the hardware.

5.2.1 Standard XDS110

You can purchase a standard XDS110 in ti.com. Figure 5-4 shows a high-level diagram of the major functional areas and interfaces of the XDS110 probe.

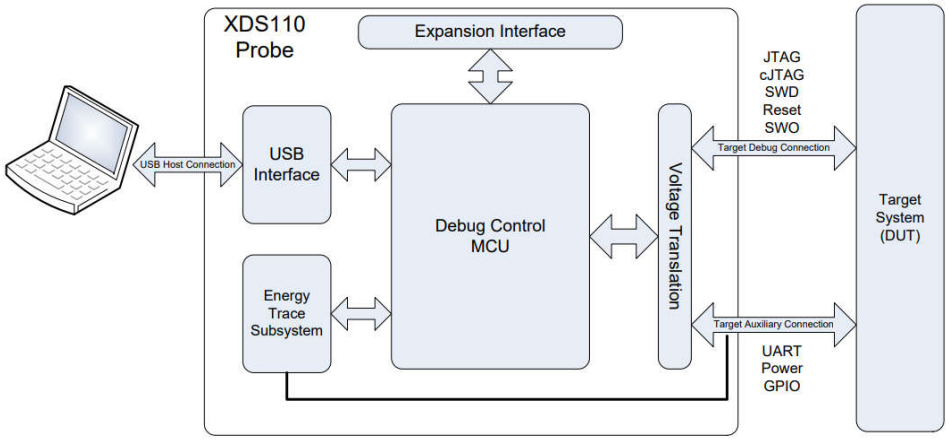

Figure 5-4. XDS110 Probe High-Level Block Diagram

More standard XDS110 information, see the *XDS110 Debug Probe User's Guide*.

5.2.2 Lite XDS110 (MSPM0 LaunchPad™ kit)

The MSPM0 LaunchPad kit include the XDS110 (Lite) circuit. You can also use this debugger to download your firmware into MSPM0 device. Figure 5-5 shows the LP-MSPM0C1104 circuit.

2.54-mm probe: This port supports the SWD protocol and includes a 5-V or 3.3-V power supply. You can connect SWDIO SWCLK 3V3 GND to the board and download firmware into the MSPM0C device.

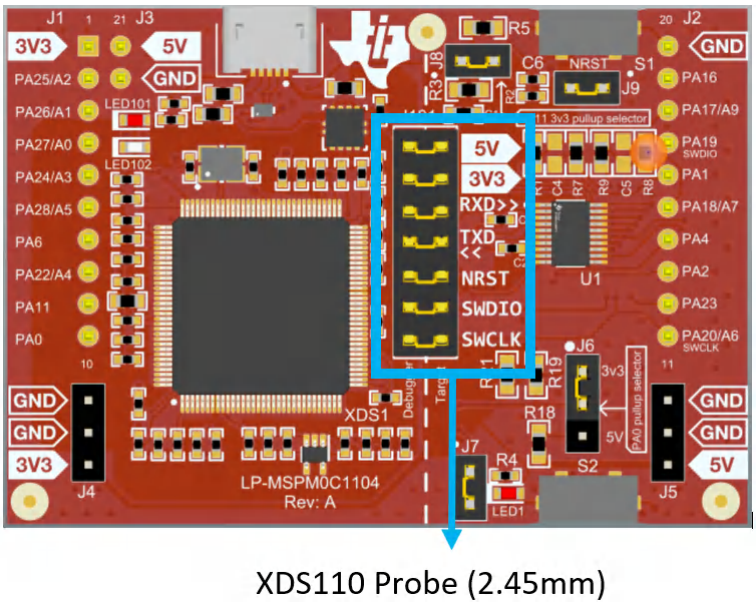

Figure 5-5. LP-MSPM0C1104

Note

- Standard XDS110 support level shift for debug ports, XDS110 just support 3.3v probe level.
- TI does not recommend using the XDS110 to power other devices except the MSPM0C MCU. The XDS110 integrates an LDO with limited current drive capability.

6 Key Analog Peripherals

The MSPM0C series MCU includes high-performance analog peripheral resources, which can provide basic analog signal conditioning functions inside the chip. To maximize the use of the MSPM0C analog peripheral performance, some considerations need to be made in the hardware design. This section discusses analog design considerations for many typical analog circuit configurations.

6.1 ADC Design Considerations

MSPM0C devices have a 12-bit, up to 1.5-Msps, analog-to-digital converter (ADC). The ADC supports fast 12-, 10-, and 8-bit analog-to-digital conversions. The ADC implements a 12-bit SAR core, sample/conversion mode control, and up to 4 independent conversion-and-control buffers.

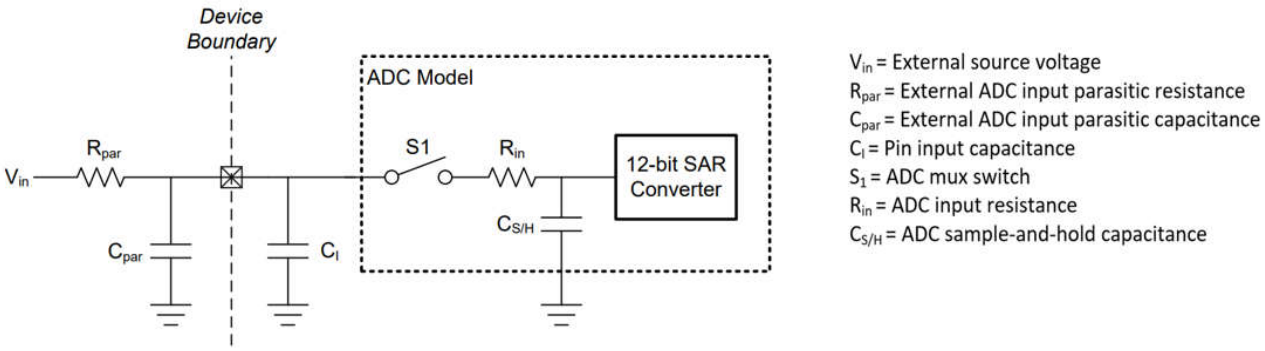

Figure 6-1. ADC Input Network

To achieve the desired conversion speed and keep high accuracy, set the proper sampling time in the hardware design. Sampling (sample-and-hold) time determines how long to sample a signal before digital conversion. During sample time, an internal switch lets the input capacitor charge. The required time to fully charge the capacitor is dependent on the external analog front-end (AFE) connected to the ADC input pin. Figure 6-1 shows a typical ADC model of an MSPM0C MCU. The R_{in} and $C_{S/H}$ values can be obtained from the device-specific data sheet. It is critical to understand the AFE drive capability and calculate the minimum sampling time required to sample the signal. The resistance of R_{par} and R_{in} affects t_{sample}. Equation 1 can be used to calculate a conservative value of the minimum sample time tsample for an n-bit and fixed settling error conversion:

$$t_{sample} \geq (\ln(2^n/\text{Settling error}) - \ln((C_{par} + C_I) / C_{S/H})) \times ((R_{par} + R_{in}) \times C_{S/H} + R_{par} \times (C_{par} + C_I)) \quad (1)$$

7 Key Digital Peripherals

The MSPM0C series MCU includes digital peripheral resources including the Timer, UART, LIN, I2C and serial peripheral interface (SPI), among others, that provide rich communication capabilities. To maximize the use of the MSPM0C digital peripherals, some considerations need to be made in the hardware design. This section discusses design considerations for many typical digital peripheral configurations.

7.1 Timer Resources and Design Considerations

Timers are one of the most basic and important modules in any MCU, and this resource is used in all applications. It can be used to process tasks regularly, delay, output PWM waveforms to drive o devices, detect the width and frequency of external pulses, simulate waveform outputs, and more.

The MSPM0C series MCU includes general-purpose timer (TIMG) and advanced control timers (TIMA). That can be used for a variety of functions, including measuring the input signal edge and period (capture mode) or generating output waveforms (compare mode output) like PWM signals. A summary of the different features and configurations of each timer is shown in the Table 7-1.

Table 7-1. TIMx Instance Configuration

Instance	Power Domain	Counter Resolution	Prescaler	Repeat Counter	CCP Channels	Phase Load	Shadow Load	Pipelined CC	Dead band	Fault Handler	QEI
TIMG0	PD0	16-bit	8-bit	-	2	-	-	-	-	-	-
TIMG1	PD0	16-bit	8-bit	-	2	-	-	-	-	-	-
TIMG2	PD0	16-bit	8-bit	-	2	-	-	-	-	-	-
TIMG3	PD0	16-bit	8-bit	-	2	-	-	-	-	-	-
TIMG4	PD0	16-bit	8-bit	-	2	-	Yes	Yes	-	-	-
TIMG5	PD0	16-bit	8-bit	-	2	-	Yes	Yes	-	-	-
TIMG6	PD1	16-bit	8-bit	-	2	-	Yes	Yes	-	-	-
TIMG7	PD1	16-bit	8-bit	-	2	-	Yes	Yes	-	-	-
TIMG8	PD0	16-bit	8-bit	-	2	-	-	-	-	-	Yes
TIMG9	PD0	16-bit	8-bit	-	2	-	-	-	-	-	Yes
TIMG10	PD1	16-bit	8-bit	-	2	-	-	-	-	-	Yes
TIMG11	PD1	16-bit	8-bit	-	2	-	-	-	-	-	Yes
TIMG12	PD1	32-bit	-	-	2	-	-	Yes	-	-	-
TIMG13	PD0	32-bit	-	-	2	-	-	Yes	-	-	-
TIMG14	PD1	16-bit	8-bit	-	4	-	-	-	-	-	-
TIMA0	PD1	16-bit	8-bit	Yes	4/2	Yes	Yes	Yes	Yes	Yes	-
TIMA1	PD1	16-bit	8-bit	Yes	2/2	Yes	Yes	Yes	Yes	Yes	-

- First look at the device specific data sheet to check which TIMG instances are available on the device
- Need to check what features are available for each TIMG instance in Technical Reference Manual

7.2 UART and LIN Resources and Design Considerations

The MSPM0C series MCU includes Universal Asynchronous Receiver-Transmitter (UART). As seen in Table 7-2, UART0 supports LIN, DALI, IrDA, ISO7816 Manchester Coding function.

Table 7-2. UART Features

UART Features	UART0 (Extend)
Active in Stop and Standby Mode	Yes
Separate transmit and receive FIFOs	Yes
Support hardware flow control	Yes
Support 9-bit configuration	Yes
Support LIN mode	Yes
Support DALI	Yes
Support IrDA	Yes
Support ISO7816 Smart Card	Yes
Support Manchester coding	Yes

Table 7-3. MSPM0C UART Specifications

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{UART}	UART input clock frequency				24	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)				3	MHz
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6	TODO	ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

The MSPM0C UART module can support up to 3-MHz baud date, this can support almost all UART applications.

Local Interconnect Network (LIN) is a commonly used low-speed network interface that consists of a commander node communicating with multiple remote responder nodes. Only a single wire is required for communication and is commonly included in the vehicle wiring harness.

The TLIN1021A-Q1 transmitter supports data rates up to 20 kbps. The transceiver controls the state of the LIN bus through the TXD pin and reports the state of the bus on its open-drain RXD output pin. The device has a current-limited wave-shaping driver to reduce electromagnetic emissions (EME).

The TLIN1021A-Q1 is designed to support 12-V applications with a wide input voltage operating range. The device supports low-power sleep mode, as well as wake-up from low-power mode via wake over LIN, the WAKE pin, or the EN pin. The device allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that can be present on a node through the TLIN1021A-Q1 INH output pin. Figure 7-1 shows a typical interface implemented using the TI TLIN1021A LIN transceiver.

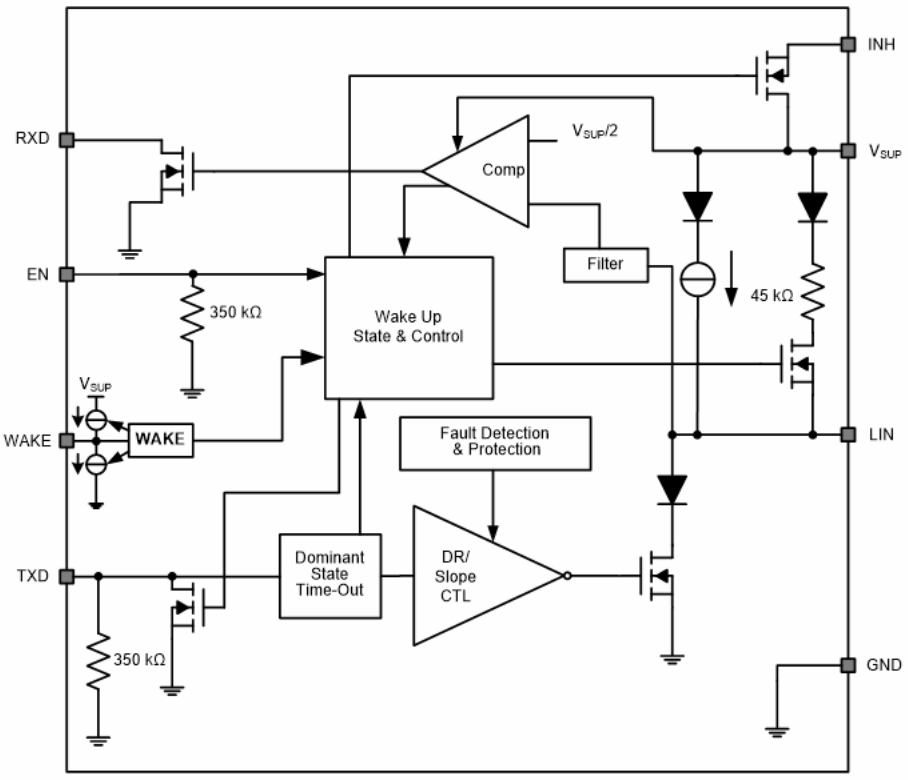

Figure 7-1. Typical LIN TLIN1021A Transceiver

Only a single wire is required for communication and is commonly included in the vehicle wiring harness. Figure 7-2 and Figure 7-3 shows a typical interface implemented using the TI TLIN1021A LIN transceiver. For more details, see the device-specific TLIN1021 data sheet.

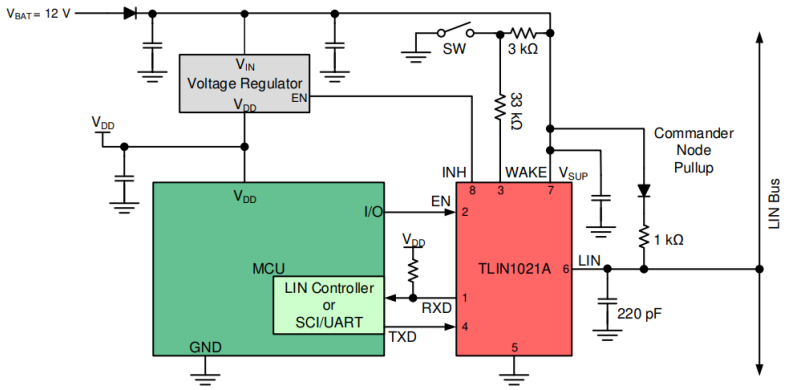

Figure 7-2. Typical LIN Application(Commander) with MSPM0C

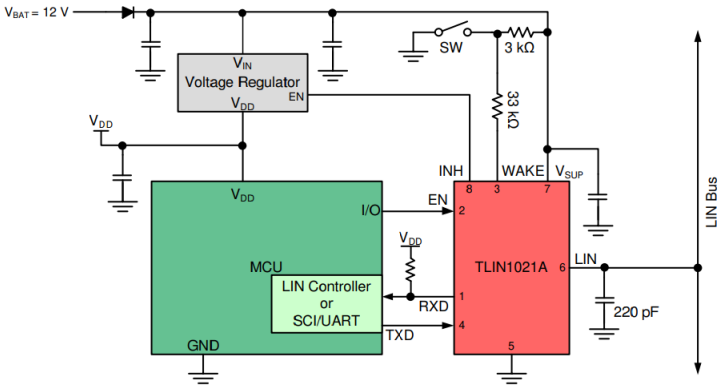

Figure 7-3. Typical LIN Application(Responder) with MSPM0C

7.3 I2C and SPI Design Considerations

SPI and I2C protocols are widely used in communication between devices or boards, such as data exchange between an MCU and a sensor. The MSPM0C series MCU includes up to 12-MHz high-speed SPI and supports 3-wire, 4-wire, chip select, and command mode. To design your system based on your requirements, see Figure 7-4.

Some SPI peripheral devices need PICO (Peripherals Input Controller Output) keep high logic. In this case, add a pullup resistor to PICO pin.

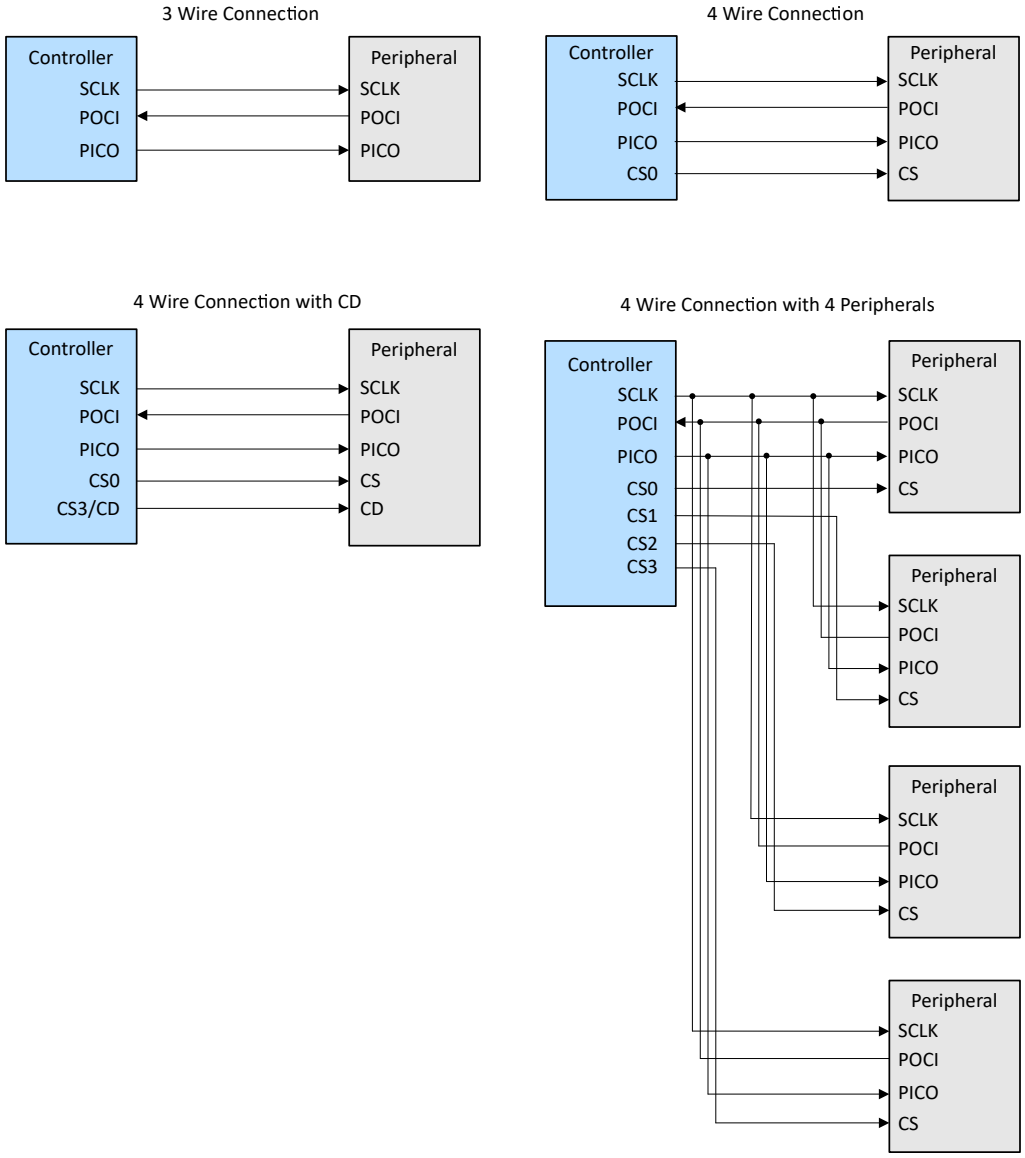

Figure 7-4. External Connections for Different SPI Configurations

For I2C bus, the MSPM0C device supports Standard, Fast and Fast plus mode, as shown in Table 7-4.

External pullup resistors are required when using I2C bus. The value of these resistors depends on the I2C speed - TI recommends 2.2k to support Fast mode+. For systems concerned with power consumption, large resistor values can be used. ODIO (see GPIOs) can be used to implement communication with a 5-V device.

Table 7-4. MSPM0C I2C Characteristics

PARAMETERS		TEST CONDITIONS	Standard Mode		Fast Mode		Fast Mode Plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{I2C}	I2C input clock frequency	I2C in Power Domain0		24		24		24	MHz
f_{SCL}	SCL clock frequency			100K		400K		1M	Hz
$t_{HD,STA}$	Hold time (repeated) START		4		0.6		0.26		us
t_{LOW}	Low period of the SCL clock		4.7		1.3		0.5		us
t_{HIGH}	High period of the SCL clock		4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START		4.7		0.6		0.26		us
$t_{HD,DAT}$	Data hold time		0		0		0		us
$t_{SU,DAT}$	Data setup time		250		100		50		us
$t_{SU,STO}$	Setup time for STOP		4		0.6		0.26		us
t_{BUF}	Bus free time between a STOP and START condition		4.7		1.3		0.5		us
$t_{VD;DAT}$	Data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	Data valid acknowledge time			3.45		0.9		0.45	us

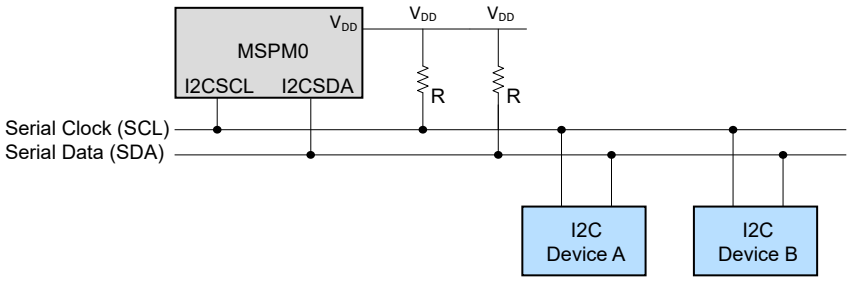

Figure 7-5. Typical I2C Bus Connection

8 GPIOs

MSPM0C series MCUs include Standard-Drive I/O (SDIO) and 5 V tolerant Open-Drain I/O (ODIO). Users can flexibly choose the appropriate I/O type based on actual requirements. And the following characteristics need to be considered in hardware design.

8.1 GPIO Output Switching Speed and Load Capacitance

When using the GPIO as I/O, design considerations must be made to ensure correct operation. As load capacitance becomes larger, the rise/fall time of the I/O pin increases. This capacitance includes pin parasitic capacitance (Ci = 5pF (Typical)) and the effects of the board traces. I/O characteristics are available in the device data sheet. Table 8-1 list the I/O output frequency characteristics of the MSPM0C device.

Table 8-1. MSPM0C GPIO Switching Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Port output frequency	SDIO	VDD ≥ 1.71 V, C_L = 20 pF			24	MHz
		ODIO	VDD ≥ 1.71 V, FM+, C_L= 20 pF to 100 pF			1	
t_r,t_f	Output rise or fall time	All output ports except ODIO	VDD ≥ 1.71 V			0.3 * f_{max}	s
t_f	Output fall time	ODIO	VDD ≥ 1.71 V, FM+, C_L= 20 pF to 100 pF	20 × VDD / 5.5		120	ns

Note

- The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.
- The output rise time of open-drain I/Os is determined by the pullup resistance and load capacitance.

8.2 GPIO Current Sink and Source

Table 8-2. MSPM0C GPIO Absolute Maximum Ratings

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	1.62		3.6	V
C_{VDD}	Capacitor placed between VDD and VSS		10		µF
I_{VDD}	Current of VDD pin			80	mA
I_{IO}	Current for SDIO pin			6	mA
	Current for ODIO pin			20	mA
T_A	Ambient temperature, S version	–40		125	°C
T_J	Max junction temperature, S version			125	°C
f_{MCLK}	MCLK, CPUCLK, ULPCLK frequency with 0 flash wait states			24	MHz

Note

- The total current of I/O must be less than the maximum value of I_{VDD}.
- ODIO are patched in a fixed pin; refer to the device data sheet.

SDIO can sink or source a maximum current of 6 mA (typical), which is sufficient to drive a typical LED. The total combined current must be less than I_{VDD} (80 mA typical).

8.3 Open-Drain GPIOs Enable 5-V Communication Without a Level Shifter

ODIO are tolerant to 5-V input. Because they are open drain, an external pullup resistor is needed for the pin to be able to output high. This I/O can used for UART or I2C interface with different voltage levels. To limit the current, a series resistor must be placed between the pin and the pullup resistor, and the RSERIES must be no less than 250 Ω. As shown in Figure 8-1, TI recommends 270 Ω. The value of the pullup resistor depends on the output frequency (see I2C and SPI Design Considerations).

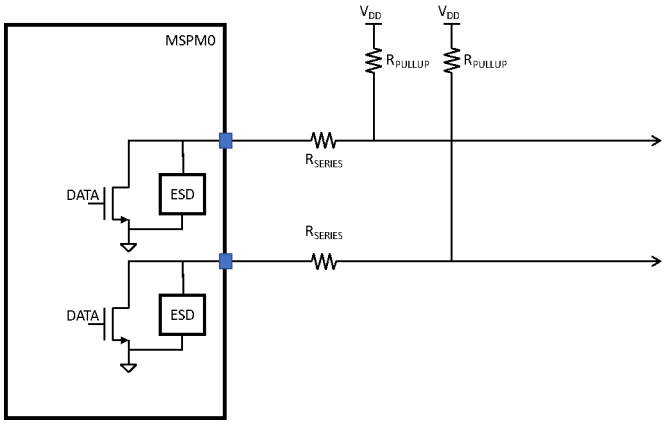

Figure 8-1. Suggested ODIO Circuit

8.4 Communicate With 1.8-V Devices Without a Level Shifter

The MSPM0C series devices use a 3.3-V logic level (excluding ODIO). To communicate with 1.8-V devices without an external level shifter device, Figure 8-2 shows a suggested circuit for interfacing with a 1.8-V device.

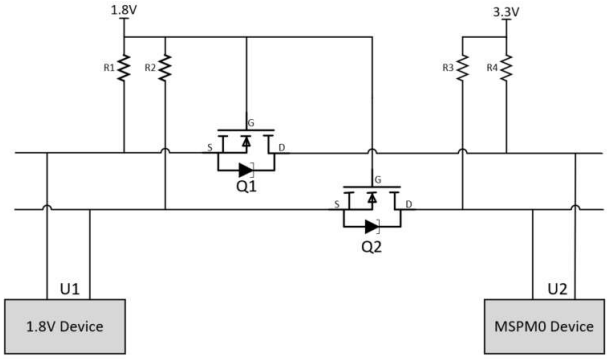

Figure 8-2. Suggested Communication Circuit With 1.8-V Device

Two MOSFET are used in this circuit - check the VGS to ensure this MOSFET be able to fully turn on with a low RDS(on): for a 1.8-V device, use less than 1.8-V VGS MOSFET. However, do not use a too low VGS MOSFET, as this causes the MOSFET to turn on at a very small voltage (MCU logic judges it as 0), resulting in communication logic error.

U1 output and U2 input

1. U1 output "1.8 V high", Q1 VGS around 0, thus Q1 turn off, U2 reads "3.3 V high" with R4.
2. U1 output "low", Q1 VGS near 1.8 V, thus Q1 turn on, U2 reads "low".

U1 input and U2 output

1. U2 output "3.3 V high", U1 keeps 1.8 V with R1, and Q1 turns off, thus U1 reads "1.8 V high".
2. U2 output "low", U1 keeps 1.8 V with R1 at first, but the diode in the MOSFET pulls down U1 to 0.7 V (diode voltage drops), and then causes VGS to be greater than the turn-on voltage, Q1 turns on, and U1 reads "low".

8.5 Unused Pins Connection

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase EMC performance, do not leave unused clocks, counters, and I/Os free or floating; for example, set I/Os to 0 or 1 (pullup or pulldown on unused I/O pins) and disable unused features.

Table 8-3. Connection of Unused Pins

Pin	Potential	Comment
PAx	Open	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unsused pins to output low or input with internal pullup or pulldown resistor.
NRST	VDD	NRST is an active-low reset signal; it must be pulled high to VCC or the device will not start.

Note

- To reduce leakage, it is advisable to configure the I/O as an analog input or to push-pull and to set it to “0”.
- BSL invoke pin must be pulled down in order to avoid entering BSL mode after reset.

9 Layout Guides

9.1 Power Supply Layout

Figure 9-1 shows the typical parts placement and routing for the power supply layout; you must modify this appropriately for your MSPM0C part. You can optionally connect a filter inductor in series with the VCC and MCU VDD pins. This inductor is used to filter the switching noise frequency of DCDC. For the value, refer to the data sheet of DCDC vendor. C1, C2, and C3 values and layout in the MSPM0C device data sheets.

Note

- Keep the smallest capacitance, closest to the MCU VDD pin (C1 < C2 < C3).
- All the traces should be direct without any vias.

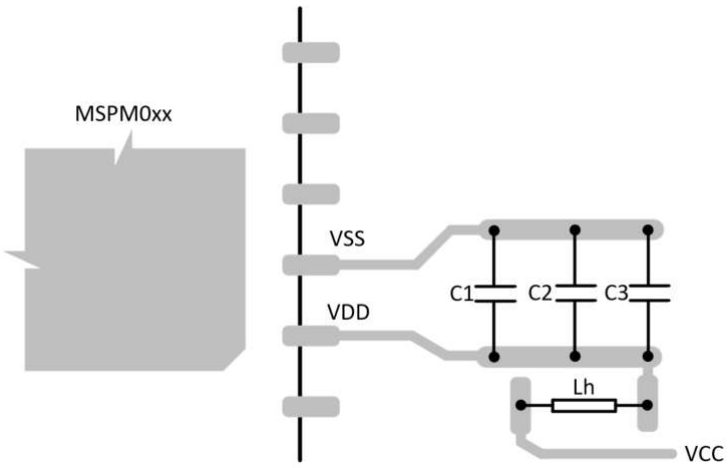

Figure 9-1. Suggested Power Supply Layout

9.2 Considerations for Ground Layout

System ground is the most critical area and foundation related to noise and EMI problems on the board. The most practical way to minimize these problems is to have a separate ground plane.

9.2.1 What is Ground Noise?

Each signal originating from a circuit (say Driver) has a return current flow to its source via ground path. As the frequency increases, or even for simple but high-current switching like relays, there is a voltage drop due to line impedance generating interference in the grounding scheme. The return path is always via the least resistance. For DC signals, that will be the lowest resistive path and for high frequency signals it will be the lowest impedance path. This explains how a ground plane simplifies the issue and is the key to ensuring signal integrity.

It is not recommended that the digital return signals propagate inside the analog return (ground) area; therefore, split the ground plane to keep all the digital signal return loops within its ground area. This splitting should be done carefully. Many designs use a single (common) voltage regulator to generate a digital and analog supply of the same voltage level (for example, 3.3 V). Isolate the analog rail and digital supply rails and their respective grounds from each other. Be careful while isolating ground, as both grounds have to be shorted somewhere. Figure 9-2 shows how possible return paths for digital signals are not allowed to form a loop passing through the analog ground. On each design, decide the common point considering the component placements and so forth. Do not add any inductors (ferrite bead) or resistors (not even zero Ω) in the series with any ground trace. The impedance increases due to associated inductance at a high frequency, causing a voltage differential. Do not route a signal referenced to digital ground over analog ground or the other direction.

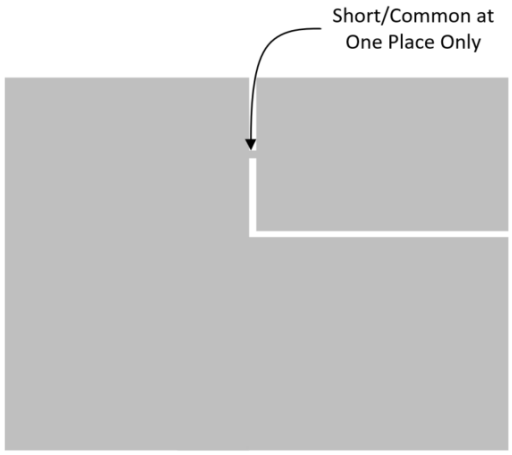

Figure 9-2. Digital and Analog Grounds and Common Area

9.3 Traces, Vias, and Other PCB Components

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner and the characteristic impedance changes. This impedance change causes reflections. Avoid right-angle bends in a trace and try to route them with at least two 45° corners. To minimize any impedance change, the best routing would be a round bend, as shown in Figure 9-3.

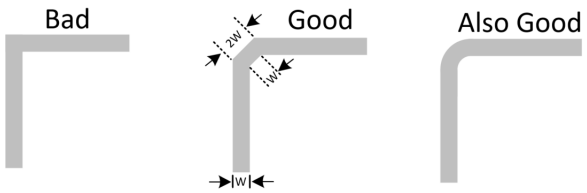

Figure 9-3. Poor and Correct Way of Bending Traces in Right Angle

To minimize crosstalk, not only between two signals on one layer but also between adjacent layers, route them 90° to each other. More complex boards need to use vias while routing; however, care must be taken when using vias as they add additional inductance and capacitance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length. When using differential signals, use vias in both traces or compensate the delay in the other trace as well.

For signal traces, pay more attention to the impact of high-frequency pulse signals, especially on relatively small analog signals (like sensor signals). Too many crossovers will couple the electromagnetic noise of the high-frequency signal to the analog signal, which will result in a low signal-to-noise ratio of the signal and affect the signal quality. Therefore, it is necessary to avoid crossing when designing. But if there is indeed an unavoidable intersection, it is recommended to intersect vertically to minimize the interference of electromagnetic noise. Figure 9-4 shows how to reduce this noise.

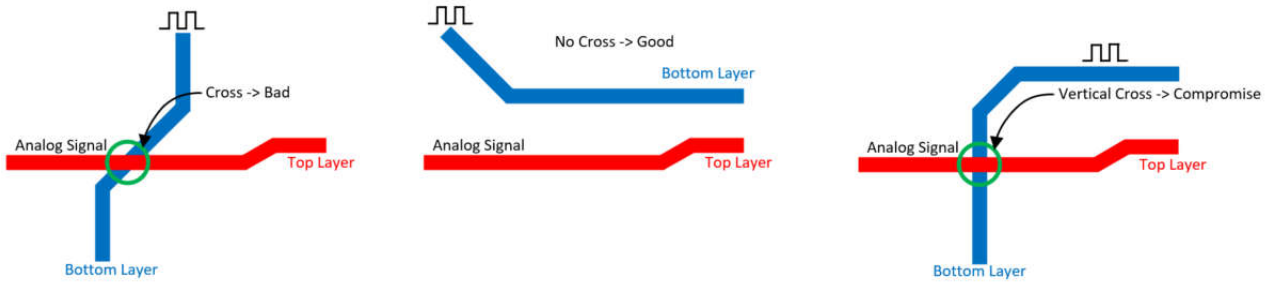

Figure 9-4. Poor and Correct Cross Traces for Analog and High-Frequency Signals

9.4 How to Select Board Layers and Recommended Stack-up

To reduce the reflections on high speed signals, it is necessary to match the impedance between the source, sink and transmission lines. The impedance of a signal trace depends on its geometry and its position with respect to any reference planes.

The trace width and spacing between differential pairs for a specific impedance requirement is dependent on the chosen PCB stack-up. As there are limitations in the minimum trace width and spacing which depend on the type of PCB technology and cost requirements, a PCB stack-up needs to be chosen which allows all the required impedances to be realized.

The minimum configuration that can be used is 2 stack-up. A 4- or 6-layer boards is required for very dense PCBs that have multiple high-speed signals.

The following stack-up (see Figure 9-5) is a 4-layer examples that can be used as a starting point for helping in a stack-up evaluation and selection. These stack-up configurations are using a GND plane adjacent to the power plane to increase the capacitance and reduce the gap between GND and power plane. So high speed signals on top layer will have a solid GND reference plane which helps to reduce EMC emissions, as going up in number of layers and having a GND reference for each PCB signal layer will improve further the radiated EMC performance.

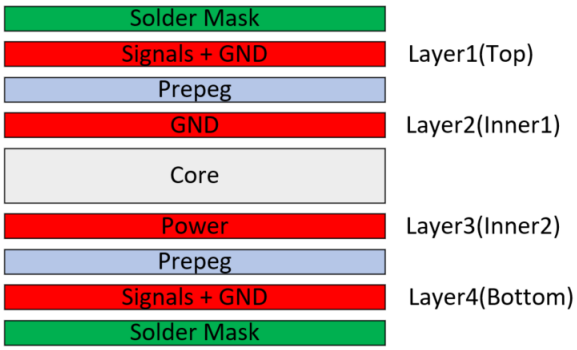

Figure 9-5. Four-Layer PCB Stack-up Example

If the system is not very complicated, there is no high-speed signal or some sensitive analog signal, then the 2 stack-up structure is sufficient.

10 References

- MSPM0C1104 Mixed-Signal Microcontrollers data sheet
- MSPM0 C-series 24-MHz Microcontrollers Technical Reference Manual
- MSPM0 L-Series MCUs Hardware Development Guide

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