TI Designs: TIPD105
AC-Coupled, Single-Supply Comparator Reference Design

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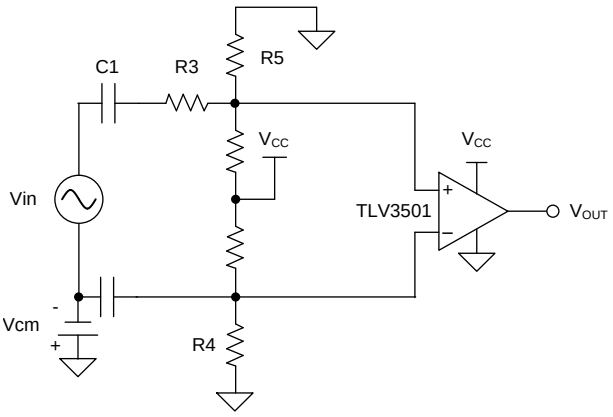
Circuit Description

A single-supply comparator is occasionally required to use AC coupling to detect sine waves or square waves. These comparators are often required because of the differences in ground potential between two different modules. Whenever AC coupling is involved in single-supply circuitry, negative voltages become a concern. Excessive negative voltages on comparators can cause the comparator to trip erroneously or to become stuck at unpredictable levels. Proper high-pass filtering and DC offsetting are required for reliable operation. This design shows how to AC couple a wide range of input signal levels and frequencies into a high-speed comparator to generate a robust and accurate clock signal.



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1 System Description

The design requirements are as follows:

- No input signal → comparator output = 0 V
- Start-up time < 1 ms
- Supply voltage: 3.3 V, +5% (3.135 V to 3.465 V)
- Input signal source supplies:
  - Vcc = 3.3 V, +5% (3.135 V to 3.465 V)
  - Vcc = 5 V, +5%, (4.75 V to 5.25 V)
  -
- Input signal levels:
  - VIL = GND + 400 mV at Isink = 2 mA
  - VIH = Vcc – 400 mV at Isource = 2 mA
  - Common-mode range: +100 mV
- Propagation delay: < 5 ns
- Duty cycle change from input to output: < 10%
- Frequency requirements: See Table 1

Table 1. Input Signal Frequency Requirements

MIN VIL	MAX VIL	MIN VIH	MAX VIH	VCM	DUTY CYCLE	t_{ON}	PERIOD
FREQUENCY 2 kHz							
0 V	400 mV	+2.7 V / +4.35 V	+3.5 V / +5.25 V	± 100 mV	40%	200 µs	500 µs
					60%	300 µs	
FREQUENCY 32 kHz							
0 V	400 mV	+2.7 V / +4.35 V	+3.5 V / +5.25 V	± 100 mV	40%	12.5 ns	31.25 ns
					60%	18.75 ns	

Table 2 shows a comparison of the design goals and simulations. Table 3 summarizes the measured performance. For each of the test cases, the duty cycle was 40%, and the comparator supply voltage was 3.135 V.

Table 2. Comparison of Design Goals and Simulations

PARAMETERS	GOAL	SIMULATED
No input signal	Vout = 0 V	Vout = 282 pV
Start-up time	< 1 ms	672 µs

Table 3. Measured Performance

WORST-CASE TEST CASE	INPUT FREQUENCY	INPUT VIL	INPUT VIH	INPUT VCM	INPUT DUTY CYCLE	SIMULATED VOUT DUTY CYCLE	MEASURED VOUT DUTY CYCLE	SIMULATED DELAY	MEASURED DELAY
1	2 kHz	0 V	5.25 V	100 mV	40%	40%	40%	3.5 ns	3.3 ns
2	2 kHz	400 mV	2.7 V	100 mV	40%	40%	40%	3.6 ns	3.75 ns
3	2 kHz	0 V	5.25 V	–100 mV	40%	40%	40%	3.5 ns	3.3 ns
4	2 kHz	400 mV	2.7 V	–100 mV	40%	40%	40%	3.6 ns	3.75 ns
5	32 MHz	0 V	5.25 V	100 mV	40%	57%	38%	3.5 ns	3.3 ns
6	32 MHz	400 mV	2.7 V	100 mV	40%	52%	39%	3.6 ns	3.75 ns
7	32 MHz	0 V	5.25 V	–100 mV	40%	57%	39%	3.5 ns	3.3 ns
8	32 MHz	400 mV	2.7 V	–100 mV	40%	51%	38%	3.6 ns	3.75 ns

Figure 1 shows the measured transient response of the design.

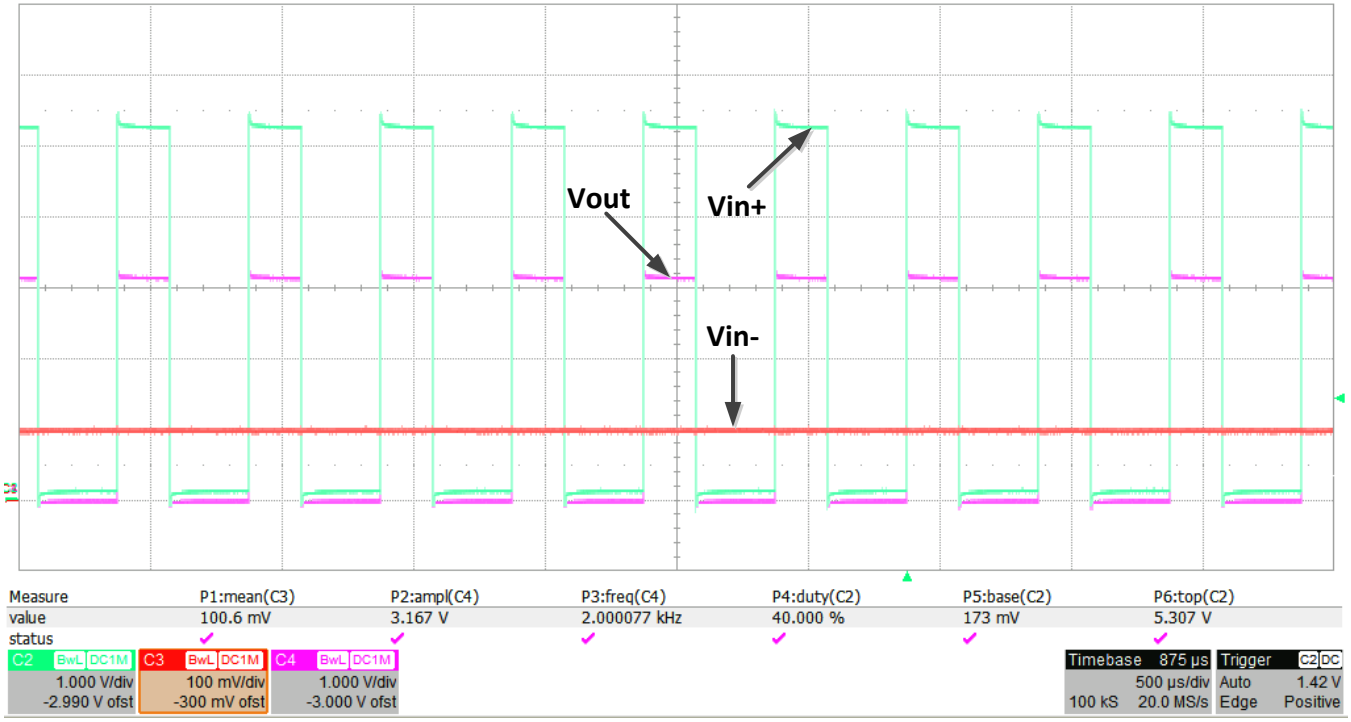
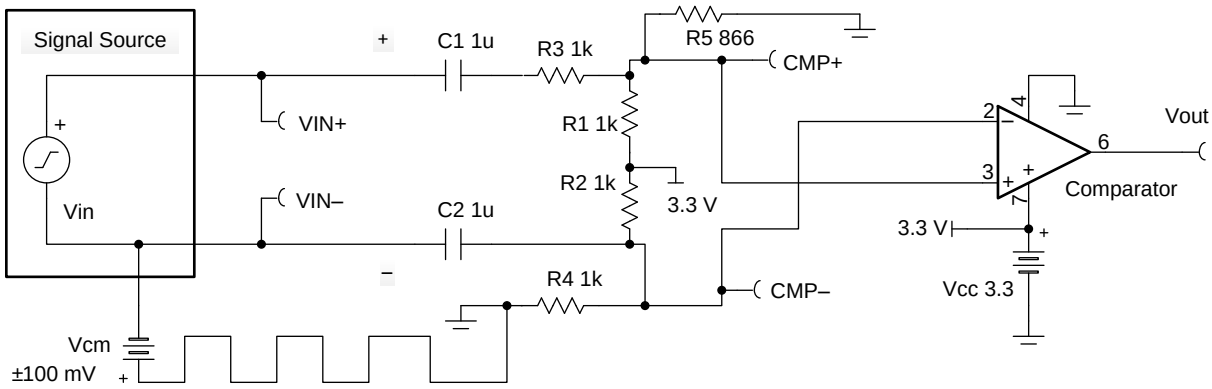


Figure 1. Transient Response of Measured Test Case 1

2 Theory of Operation

The AC-coupled, single-supply comparator circuit design provides a way to ignore ground differences between modules and to accommodate a wide range of both frequencies and amplitudes into a high-speed comparator, which results in a robust and accurate clock signal (see Figure 2). C1 and C2 provide the AC coupling of the input signal Vin. R2 and R4 provide a DC offset of mid-supply for CMP–. R1 and R5 provide a DC offset of approximately 100 mV less than mid-supply into CMP+. The differences in DC offset between CMP– and CMP+ ensure that, for no input signal, Vout is to be at the comparator-output low voltage (near 0 V). The DC offset on each input is necessary to counteract the negative voltages that occur on these inputs due to the AC coupling of Vin. R3 provides a way to divide the AC-coupled input signal down in amplitude to be less than the common-mode voltage of the comparator used. The input-scaling resistors, combined with the comparator input capacitance, form a low-pass input filter and attenuate the AC-coupled signal into the comparator. For this reason, maintaining the resistor values as low as practical is desired. The high-pass cutoff frequency of the input signal conditioning can be viewed as a simple C-R high pass with C = C1 || C2 and R = 1.964 k, which is the equivalent input resistance seen across the ends of C1 and C2 connected to CMP+ and CMP– through scaling resistors R1, R2, R3, R4, and R5.



Ground Mismatch in Signal Source
vs Conditioning Circuit

Design Analysis:
1) Use lowest value resistors possible for 32-MHz inputs.
Resistors interact with comparator parasitic input capacitance.
2) Set Vin– to mid-supply bias point.
3) Set Vin+ < mid-supply + Vos to ensure Vout = 0 V at no signal.
4) In addition, the signal must be divided down with R3 to prevent negative voltages for 0- to 5-V inputs.

Design Analysis:
5) AC couple, high- pass frequency:
Large capacitors require longer startup time from power-on.
Use 1 µF to get high pass of about 162 Hz.
For high-pass equivalent Cin = 0.5 µF, Rin = 1.964 k.

Figure 2. Complete Circuit Schematic

3 Component Selection

3.1 Comparator Selection

The preceding shows that the minimum t_{ON} of 12.5 ns is at 32 MHz and a 40% duty cycle. If the comparator has a propagation delay any longer than 12.5 ns a 32-MHz, 40% duty cycle cannot be detected. The table in Figure 3 highlights the key comparator specifications, which consist of a single supply (2.5 V to 3.5 V), rail-to-rail input, and propagation delay less than or equal to 12.5 ns based on the maximum input frequency of 32 MHz with a 40% duty cycle. The TLV3501 device meets all of these criteria.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = −40°C to +125°C.**

At T_A = +25°C and V_S = +2.7V to +5.5V, unless otherwise noted.

PARAMETER		CONDITION	TLV3501, TLV3502 MIN	TLV3501, TLV3502 TYP	TLV3501, TLV3502 MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage(1)	V_{OS}	V_{CM} = 0V, I_O = 0mA		±1	±6.5	mV
vs Temperature	**dV_{OS}/dT**	**T_A = −40°C to +125°C**		**±5**		**µV/°C**
vs Power Supply	PSRR	V_S = 2.7V to 5.5V		100	400	µV/V
Input Hysteresis				6		mV
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_{CM} = V_{CC}/2		±2	±10	pA
Input Offset Current(2)	I_{OS}	V_{CM} = V_{CC}/2		±2	±10	pA
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V−) − 0.2V		(V+) + 0.2V	V
Common-Mode Rejection	CMRR	V_{CM} = −0.2V to (V+) + 0.2V	57	70		dB
		V_{CM} = −0.2V to (V+) + 0.2V	**55**			**dB**
INPUT IMPEDANCE						
Common-Mode				10^{13} ||2		Ω ||pF
Differential				10^{13} ||4		Ω ||pF
SWITCHING CHARACTERISTICS						
Propagation Delay Time(3)	$T_{(pd)}$	ΔV_{IN} = 100mV, Overdrive = 20mV		4.5	6.4	ns
		ΔV_{IN} = 100mV, Overdrive = 20mV			**7**	**ns**
		ΔV_{IN} = 100mV, Overdrive = 5mV		7.5	10	ns
		ΔV_{IN} = 100mV, Overdrive = 5mV			**12**	**ns**
Propagation Delay Skew(4)	$\Delta t_{(SKEW)}$	ΔV_{IN} = 100mV, Overdrive = 20mV		0.5		ns
Maximum Toggle Frequency	f_{MAX}	Overdrive = 50mV, V_S = 5V		80		MHz
Rise Time(5)	t_R			1.5		ns
Fall Time(5)	t_F			1.5		ns
OUTPUT						
Voltage Output from Rail	V_{OH},V_{OL}	I_{OUT} = ±1mA		30	50	mV

Figure 3. Comparator Specifications

3.2 Comparator Input Capacitance and Low Pass Frequency

The schematic in Figure 4 shows the equivalent input impedance of the TLV3501 comparator. Through series and parallel combination of the input capacitances, the designer can arrive at the total equivalent differential input capacitance, Cin_eq, of 5 pF.

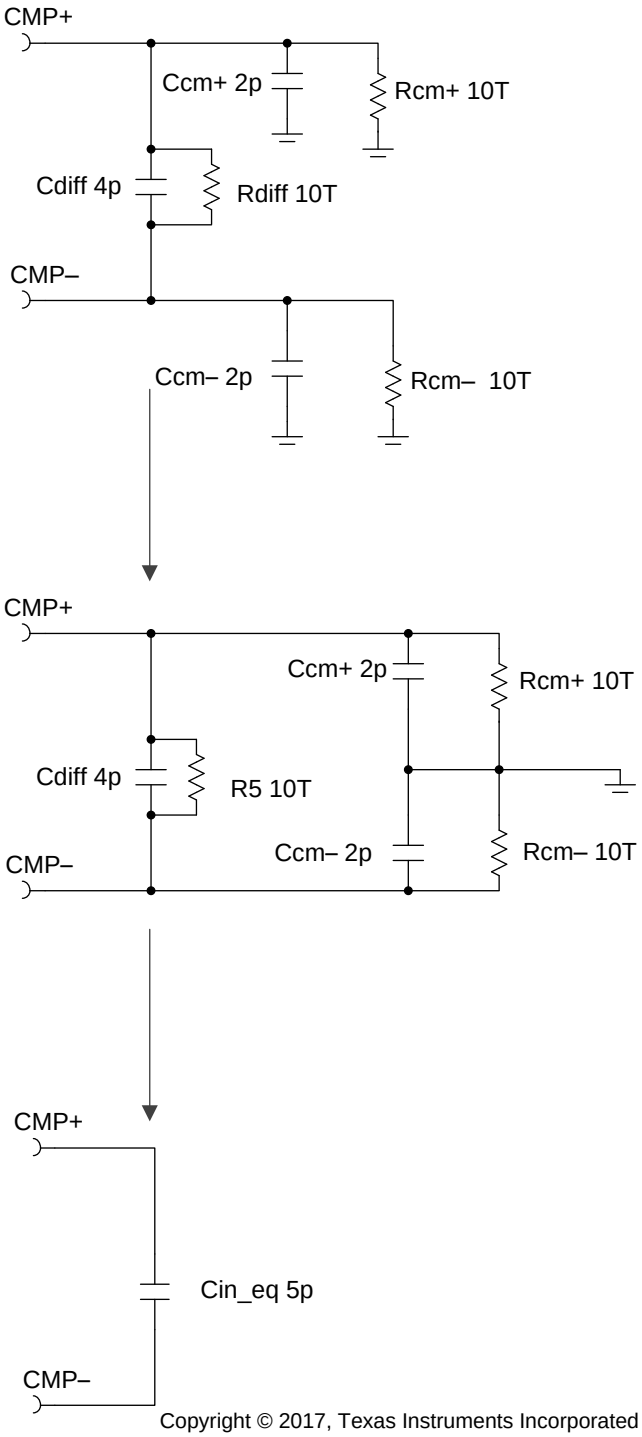


Figure 4. Comparator Input Capacitance

The total equivalent input capacitance, Ceq_in, combined with the total input resistance, Rin_eq, forms a single pole which attenuates the input signal. The next step is to choose a low-pass frequency point no lower than 32 MHz as this is the maximum input frequency. As Figure 5 shows, Rin_eq must be limited ≤ to 995 Ω.

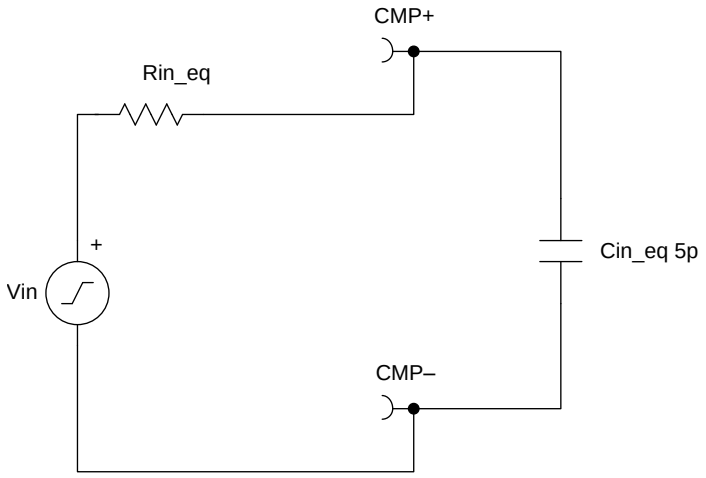


Figure 5. Low-Pass Filter Limitations

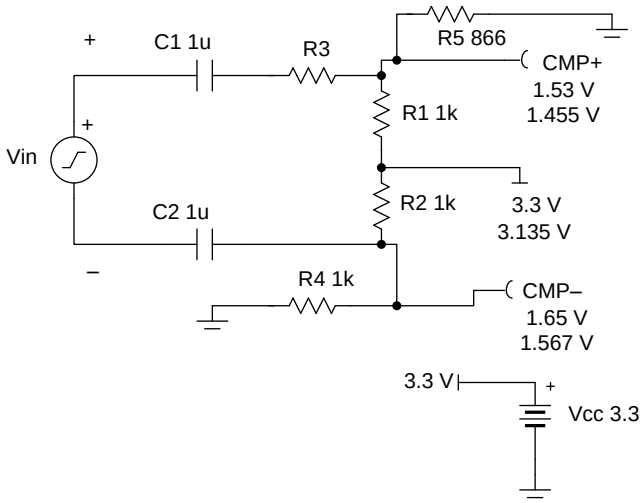
$$f\,max = 32\,MHz$$

$$f\_3dB = \frac{1}{2\pi(Cin\_eq)(Rin\_eq)}$$

$$32\,MHz = \frac{1}{2\pi(5\,pF)(Rin\_eq)} \rightarrow Rin\_eq = 995\,\Omega \quad (1)$$

3.3 Input Scaling Offset

The input-scaling offset circuit consists of R1, R2, R4, R5, and the supply voltage Vcc as shown in Figure 6. The offset has been computed for DC with no dynamic input signal. R2 and R4 divide Vcc to provide a 1.65-V offset for CMP–. R1 and R5 divide Vcc down to yield a 1.53-V offset on CMP+. Through the use of standard values, CMP+ is approximately 100 mV lower than CMP–. This specification, along with the TLV3501 input offset voltage of ±6.5 mV plus room for noise margin, ensures that the TLV3501 output is forced to zero when no signal is present, which the specifications of this design requires.

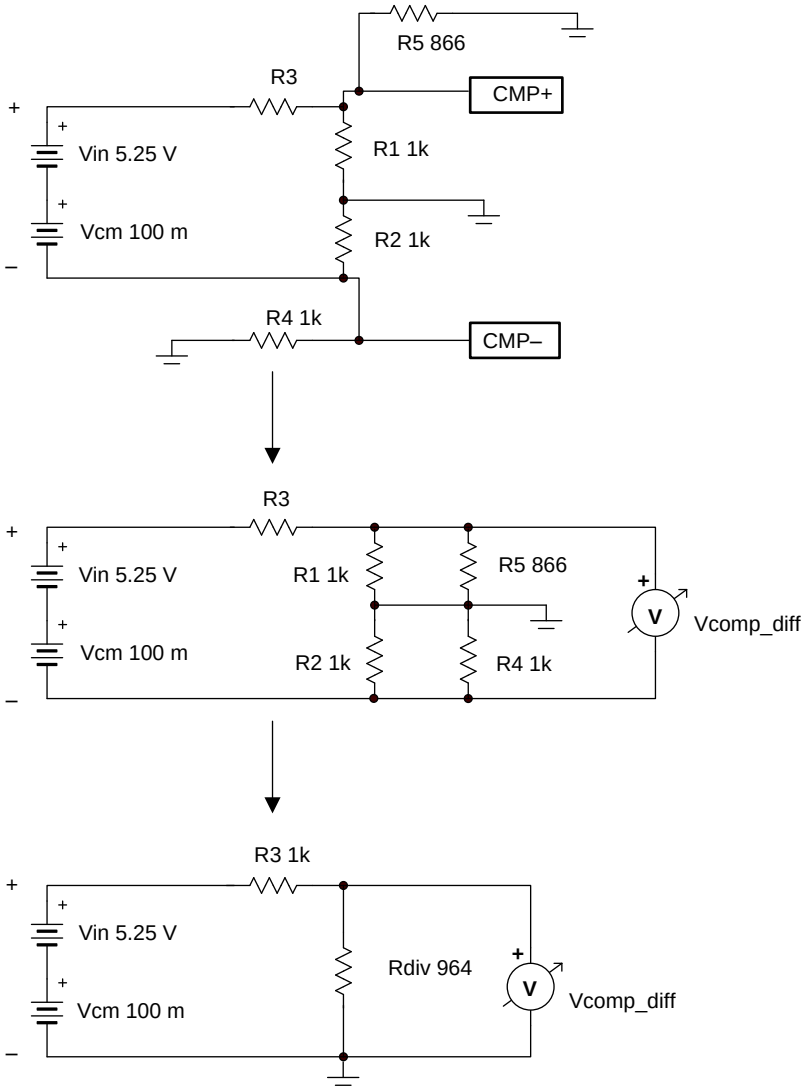


1) Offset both inputs to mid-supply so Vin negative voltages are offset to a positive value to meet TLV3501common-mode voltage range.
2) Set CMP– > (CMP+) + 100 mV to ensure that with Vin = 0 V TLV3501 Output = 0 V.
3) From Figure 4 acknowledge that Rin_eq = 995 Ω to allow Vin to pass due to TLV3501 input capacitance.
4) Start by using 1k range values to yield Rin_eq = 995 Ω.
5) On CMP– use standard values and set R2 = R4 = 1k for Vcm = Vcc / 2
6) On CMP+ use standard values and set CMP+ < (CMP–) – 100 mV.
Set R1 = 1k to keep near matched resistance from Vcc to GND. Select R5 for offset from CMP–.
7) Bottom values represent worst- case minimum values with reference variation.

Figure 6. Input Scaling Offset

3.4 Input Divider

When the Vin signal has been AC-coupled into the comparator circuit, the next step is to ensure that its amplitude is no larger than the minimum input common-mode voltage range of the TLV3501 device. Figure 7 shows a detailed analysis for choosing the last scaling resistor, R3, to adequately divide down the maximum Vin amplitude within the minimum common-mode input of the TLV3501 device.

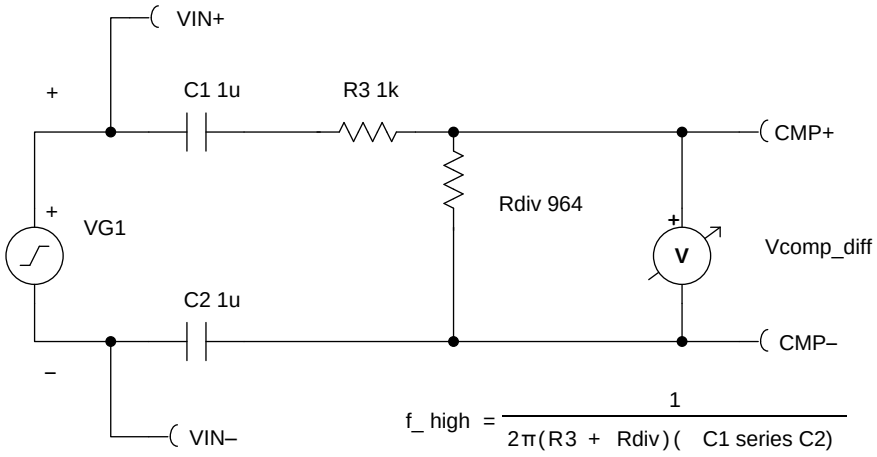


1) Vin_max = 5.25 V + 100 mV.
2) Equivalent resistor network in series with R3 is 964 Ω.
3) Minimum Vcc = 3.135 V
4) Keep Vcomp_diff < 3.335 V to meet Vcm specification of TLV3501.
5) R3_min = 582 Ω. Choose R3 = 1k for better margin and standard value already used.

Figure 7. Input Divider

3.5 Input High-Pass Filter

The AC-coupling of Vin into the comparator of this design is set by R3, Rdiv, C1, and C2, as Figure 8 shows.



1) fin_min = 2 kHz
2) Set f_high < 200 Hz; at least one decade under desired pass frequency for high-pass cut frequency.
3) For standard capacitor value, set C1 = C2 = 1 µF.
4) f_high calculates as 162 Hz.

Figure 8. Input High-Pass Filter

3.6 Recommend Component Properties

Table 4 provides the recommended component properties for the parts used in the AC-coupled comparator circuit.

Table 4. Recommended Component Properties

REF DESIGNATOR	VALUE	RECOMMENDED PROPERTIES
C1, C2	1 µF	10%, ceramic capacitor; X5R or X7R tempco
R1, R2, R3, R4	1k Ω	1/8 W, 1% film resistor, 100-ppm tempco
R5	866 Ω	1/8 W, 1% film resistor, 100-ppm tempco
U1	TLV3501	Single supply, +2.7 V to +5.5 V, Cin < 5 pF, propogation delay < 12 ns

4 Simulation

4.1 Input-Scaling Frequency Check

The circuit in Figure 9 allows the user to check the frequency response of the input-scaling network. An additional 4 pF of differential input capacitance, Cdiff, has been added to the TLV3501 device in Figure 9 to properly model the complete input capacitance of the comparator. See Section A.10 for details on this modification.

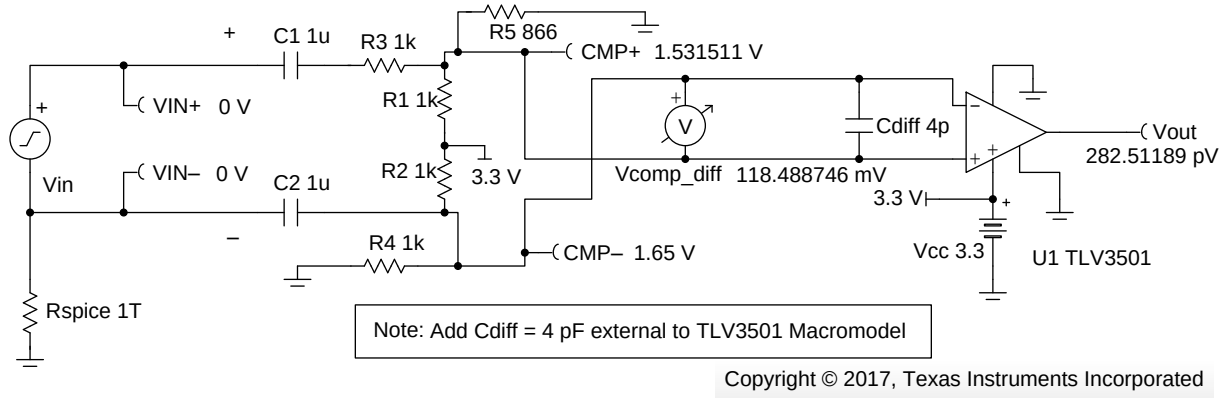


Figure 9. Input Scaling Frequency Test Circuit

As Figure 10 shows, the input-scaling network passes signals between the –3-dB high-pass point of 162 Hz to the low-pass cutoff frequency of 64 MHz. The 162 Hz is approximately one decade away from the specified, low-frequency signal range of 2 kHz. The 64-MHz low-pass is approximately two times the upper-specified operating frequency of 32 MHz.

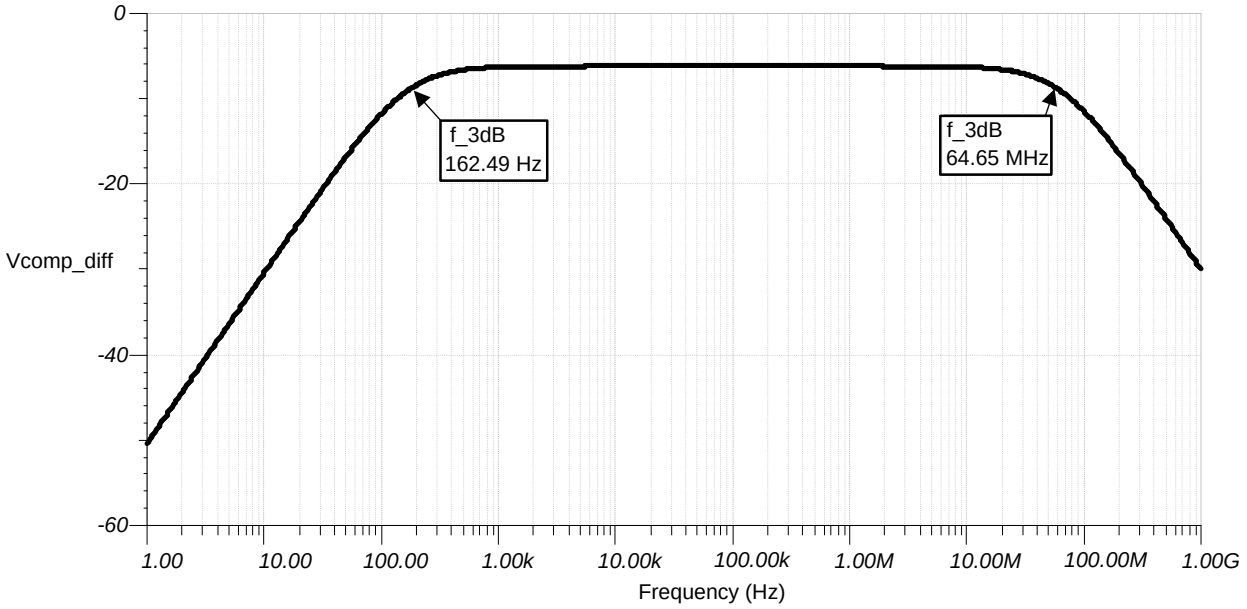


Figure 10. Input-Scaling Frequency Response

4.2 AC-Coupled Signals Yield Negative Voltages

If the DC offset of Vcc = 3.3 V were to be removed (see the test circuit in Figure 11), then the user could observe the effects of AC coupling and the magnitudes of negative voltages that would appear at the TLV3501 inputs, CMP+ and CMP–. From superposition, whatever negative voltages that appear are counteracted directly by the positive DC offsets of 1.65 V on CMP– and 1.53 V on CMP+. Figure 12 and Figure 13 confirm that the DC offsets on CMP– and CMP+ are required.

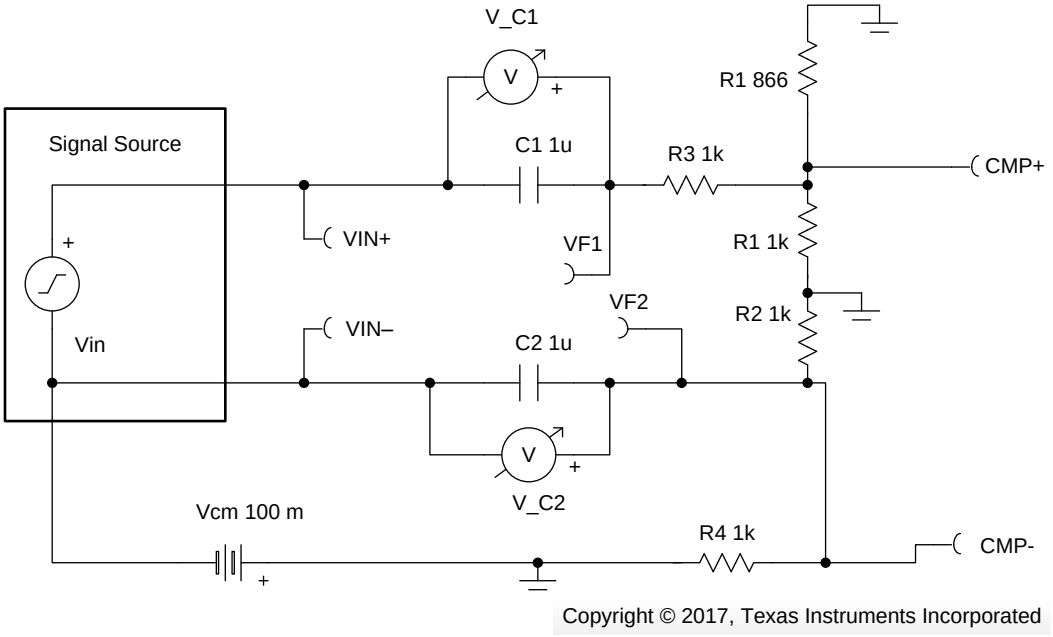


Figure 11. AC-Coupled Signals—Negative Voltage Test

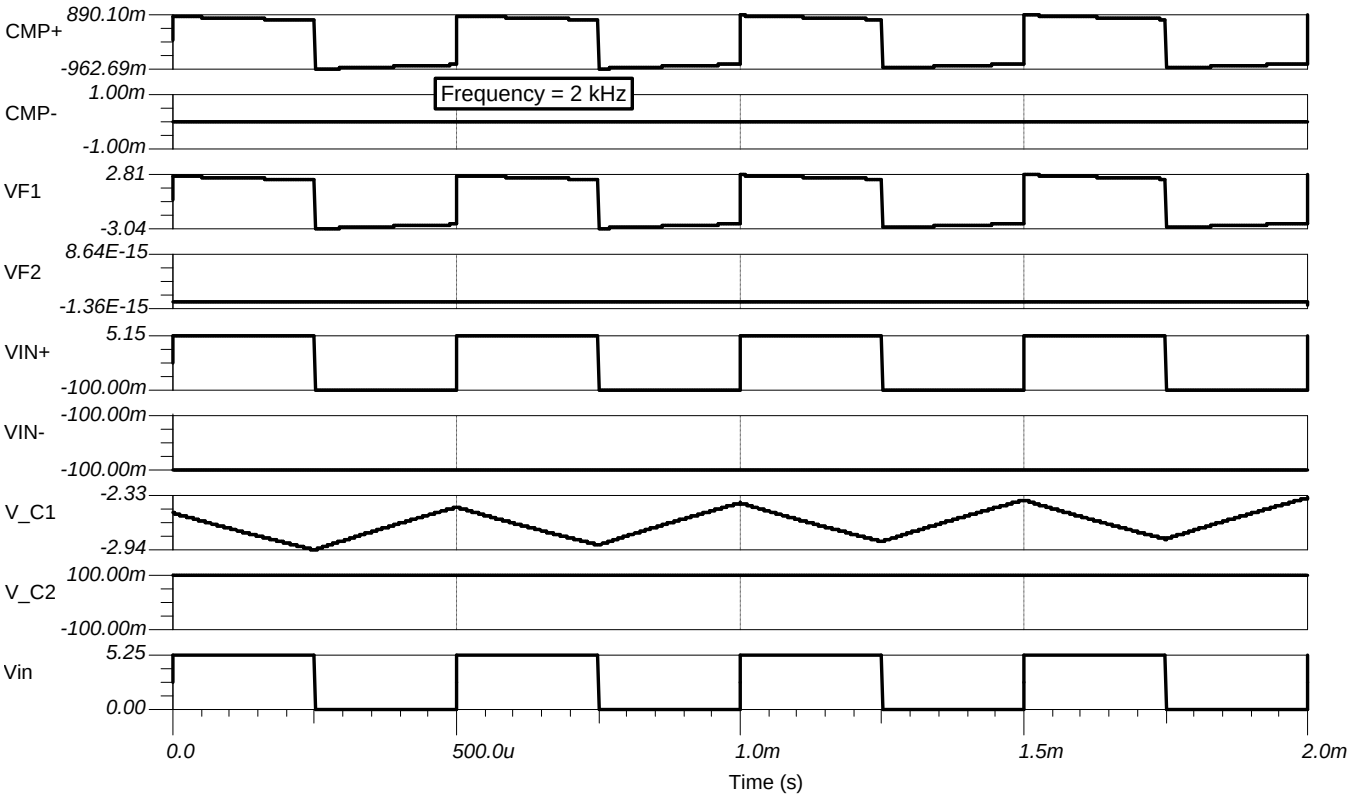


Figure 12. AC-Coupled Signals—Negative Voltage 2 kHz

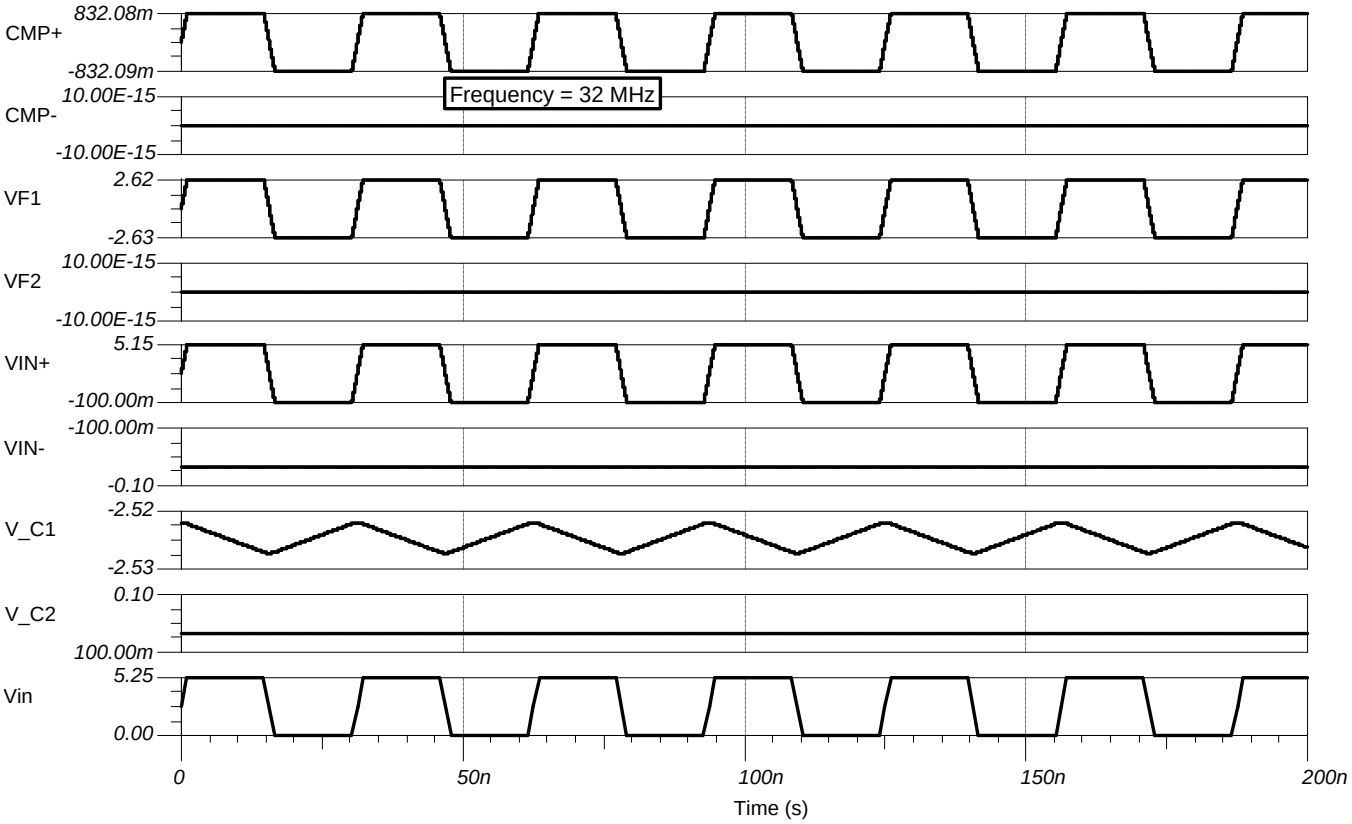


Figure 13. AC-Coupled Signals—Negative Voltage 32 MHz

4.3 Test Cases

The worst-case test cases for the TIPD105 design are detailed in Table 5. To ensure that the circuit works robustly at the extremes, the minimum- and maximum-input amplitudes are checked along with the minimum- and maximum frequencies and minimum- and maximum common-mode input voltage. Figure 14 is the test circuit for checking the final design. Figure 15 shows the initial start-up time until the reliable signals are observable from the TLV3501 device. By checking the selection for the “Zero initial values” field in the *Transient Analysis* control window, the user can discern how long it takes for the input AC-coupling capacitors to charge, resulting in the output of reliable pulses after approximately 672 µs. For Figure 16 through Figure 23, the “Calculate operating point” option in the *Transient Analysis* control window has been set to ignore the start-up time and observe the behavior of the circuit after C1 and C2 are past the initial start-up time. The key thing to look at is how far CMP+ is swinging about CMP–. The input offset voltage for the TLV3501 comparator is ±6.5 mV. This is a voltage which the designer must stay far away from in the high- and low AC-coupled input levels for reliable operation. In all test cases, the CMP+ is at least 120 mV above or below CMP– in the high levels and low levels that have been AC-coupled into the TLV3501 comparator inputs.

Table 5. Worst-Case Test Cases for AC-Coupled Comparator

TEST CASE	FREQUENCY	VIL	VIH	VCM	DUTY CYCLE	Vcc
1	2 kHz	0 V	5.25 V	+100 mV	40%	3.135 V
2	2 kHz	400 mV	2.7 V	+100 mV	40%	3.135 V
3	2 kHz	0 V	5.25 V	–100 mV	40%	3.135 V
4	2 kHz	400 mV	2.7 V	–100 mV	40%	3.135 V
5	32 MHz	0 V	5.25 V	+100 mV	40%	3.135 V
6	32 MHz	400 mV	2.7 V	+100 mV	40%	3.135 V
7	32 MHz	0 V	5.25 V	–100 mV	40%	3.135 V
8	32 MHz	400 mV	2.7 V	–100 mV	40%	3.135 V

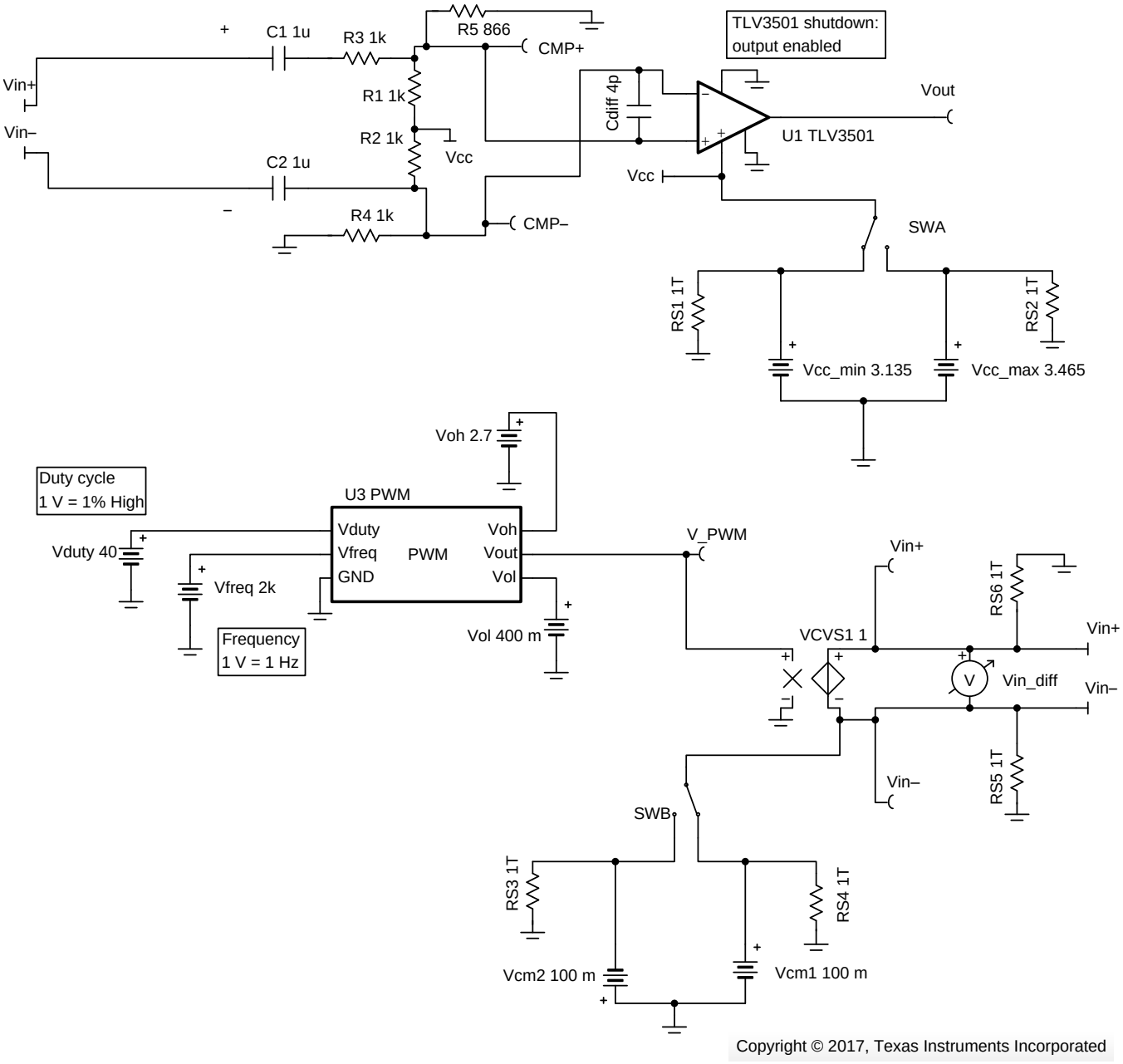


Figure 14. SPICE Test Case Circuit

To test the final design, use an easy-to-adjust pulse-width modulated (PWM) signal generator, as the preceding Figure 14 shows. This generator has an adjustable frequency, duty cycle, Voh (output high-voltage level), and Vol (output low-voltage level). These adjustable features allow the user to easily test all corner conditions of the design specifications for the compliance of the final circuit implementation. Refer to Section A.11 for design details of the PWM signal source. Two common-mode voltages, Vcm1 (+100 mV) or Vcm2 (–100 mV), are added to offset the PWM signal generator on the output of VCVS1 (voltage-controlled voltage source) per the Vin common-mode specification. A switch, SWB, functions to select the common-mode input-applied voltage. Note that both common-mode voltages have a 1-TΩ resistor in parallel alignment to avoid SPICE convergence issues. The outputs of VCVS1 are each terminated with 1-TΩ resistors for SPICE convergence when the user connects to the AC-coupled comparator inputs.

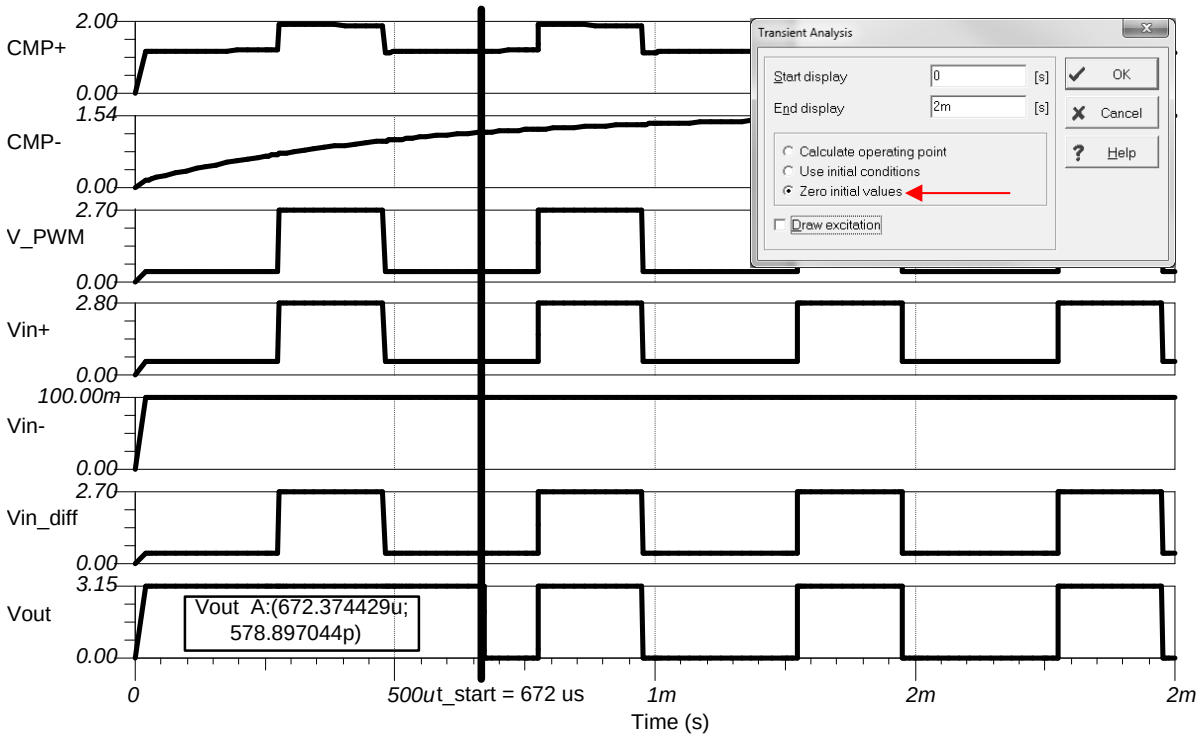


Figure 15. Initial Start Charge Time for CMP–

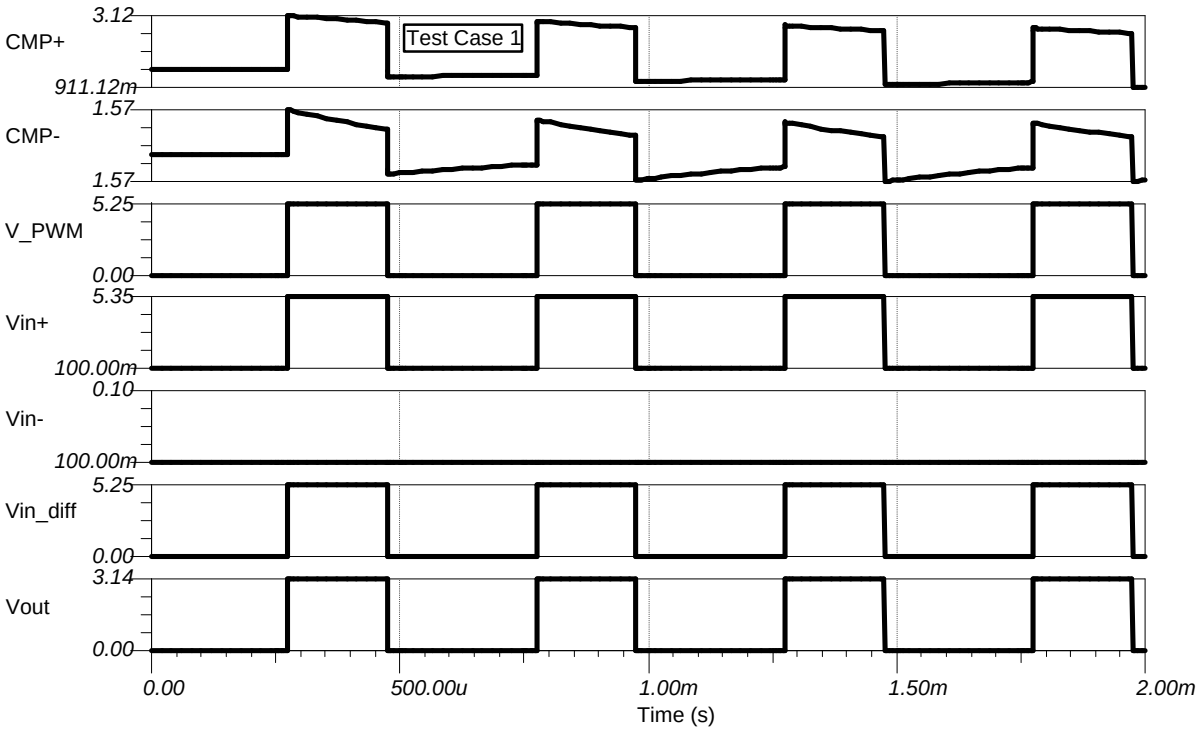


Figure 16. Test Case 1

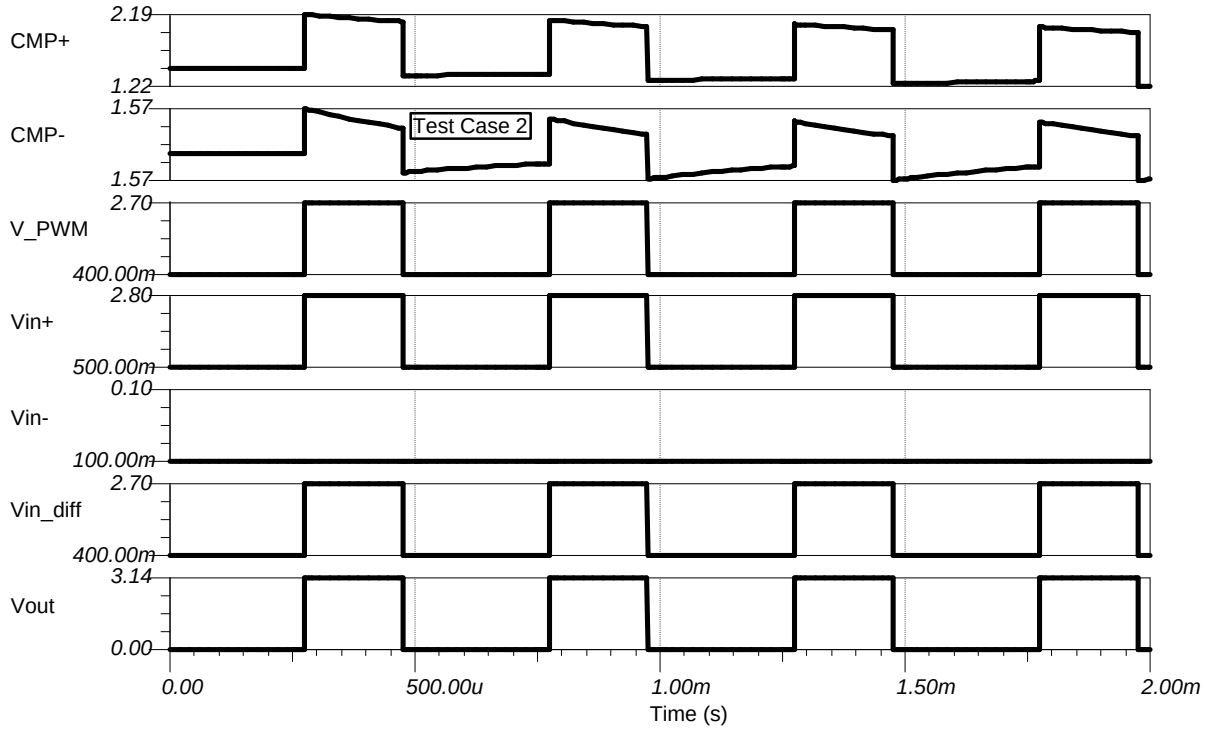


Figure 17. Test Case 2

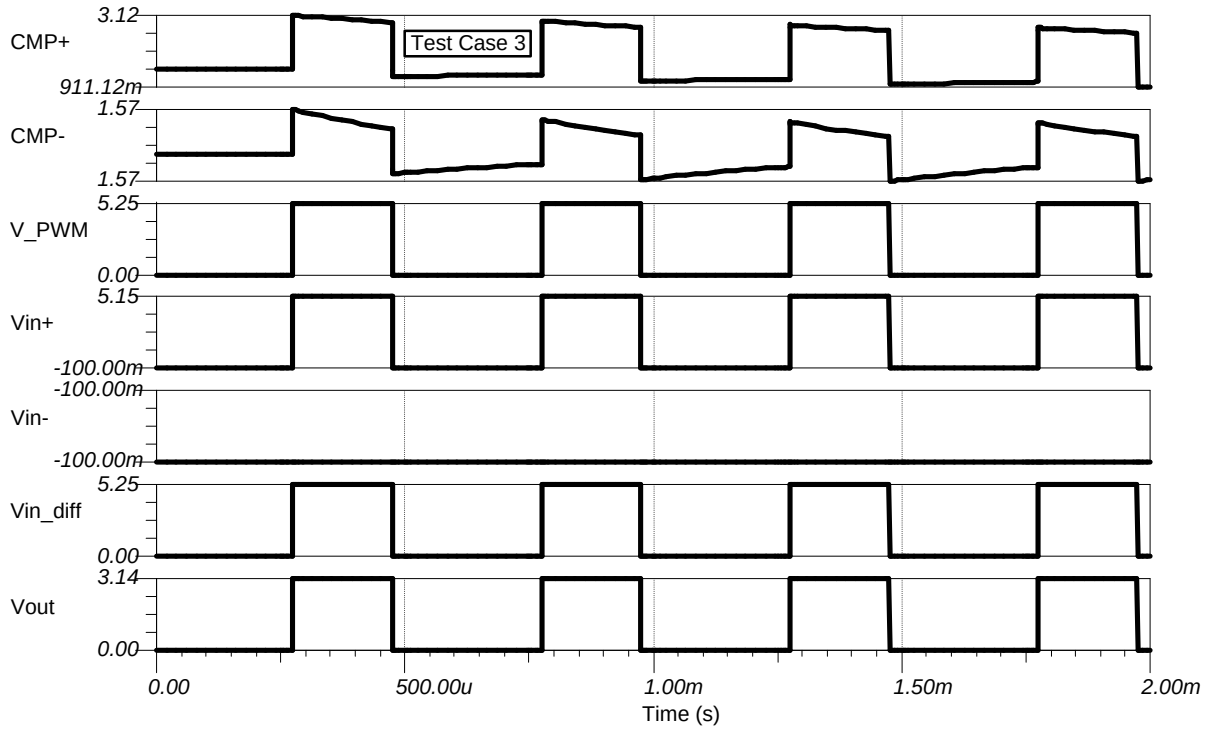


Figure 18. Test Case 3

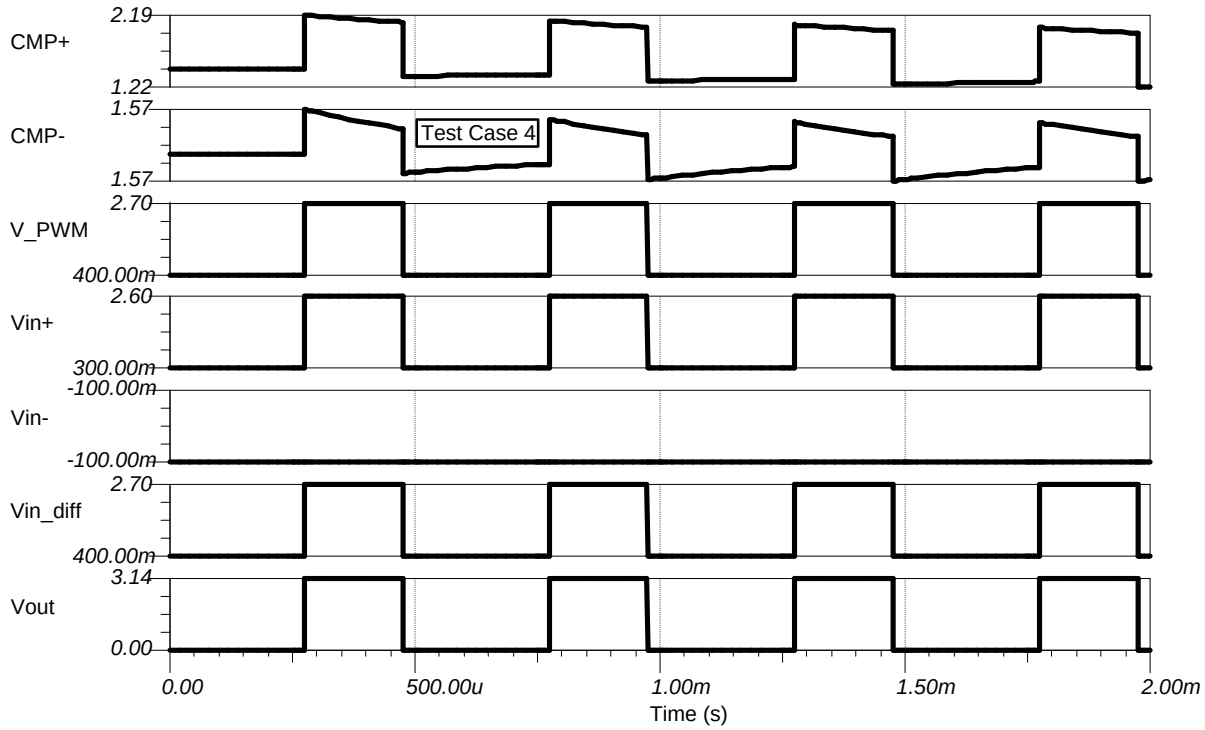


Figure 19. Test Case 4

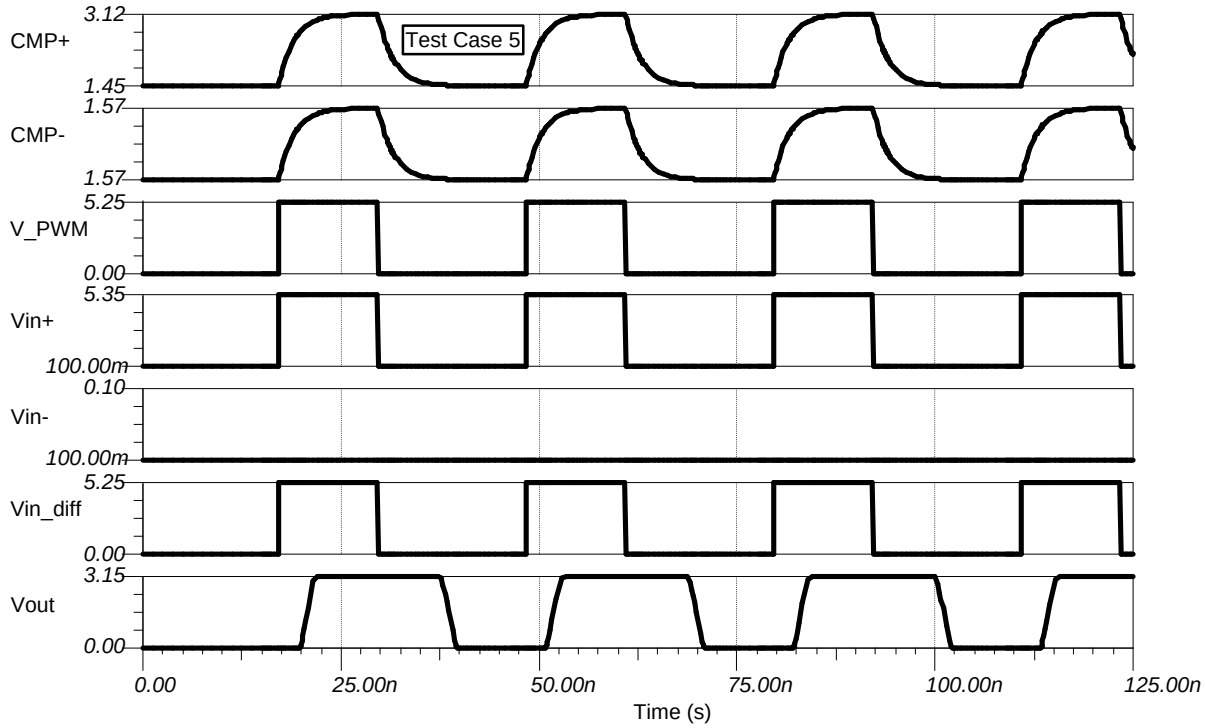


Figure 20. Test Case 5

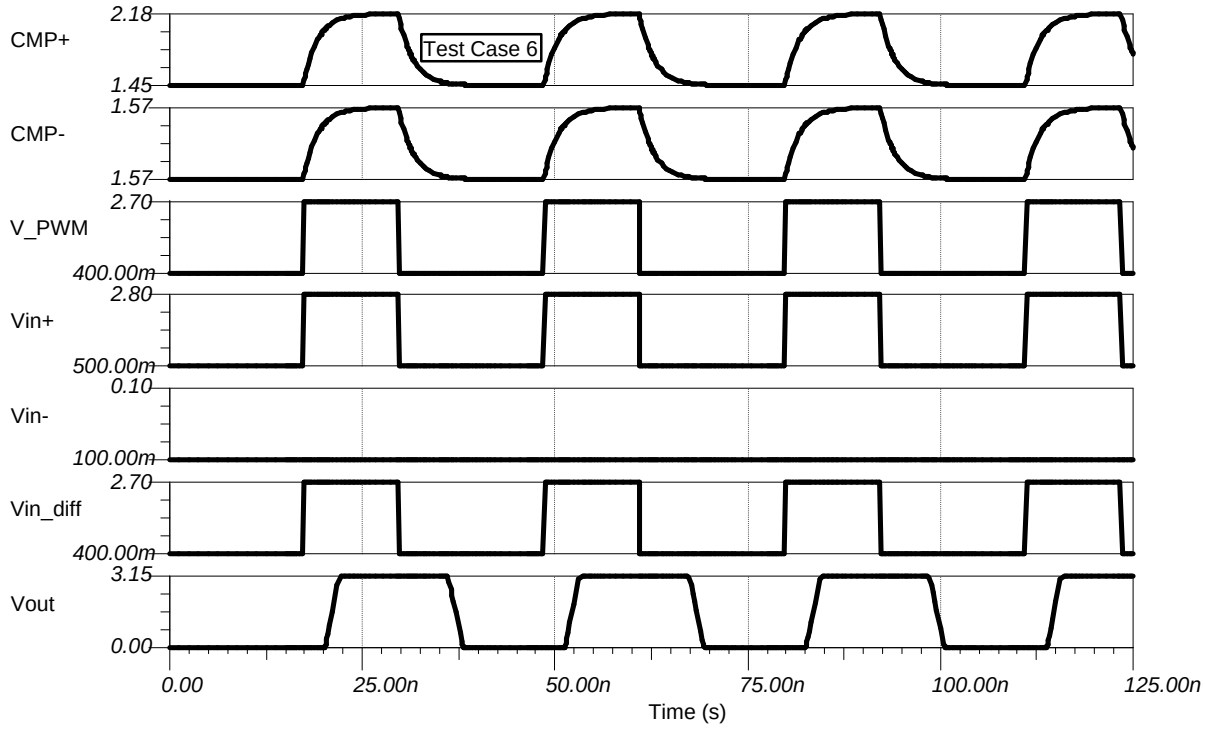


Figure 21. Test Case 6

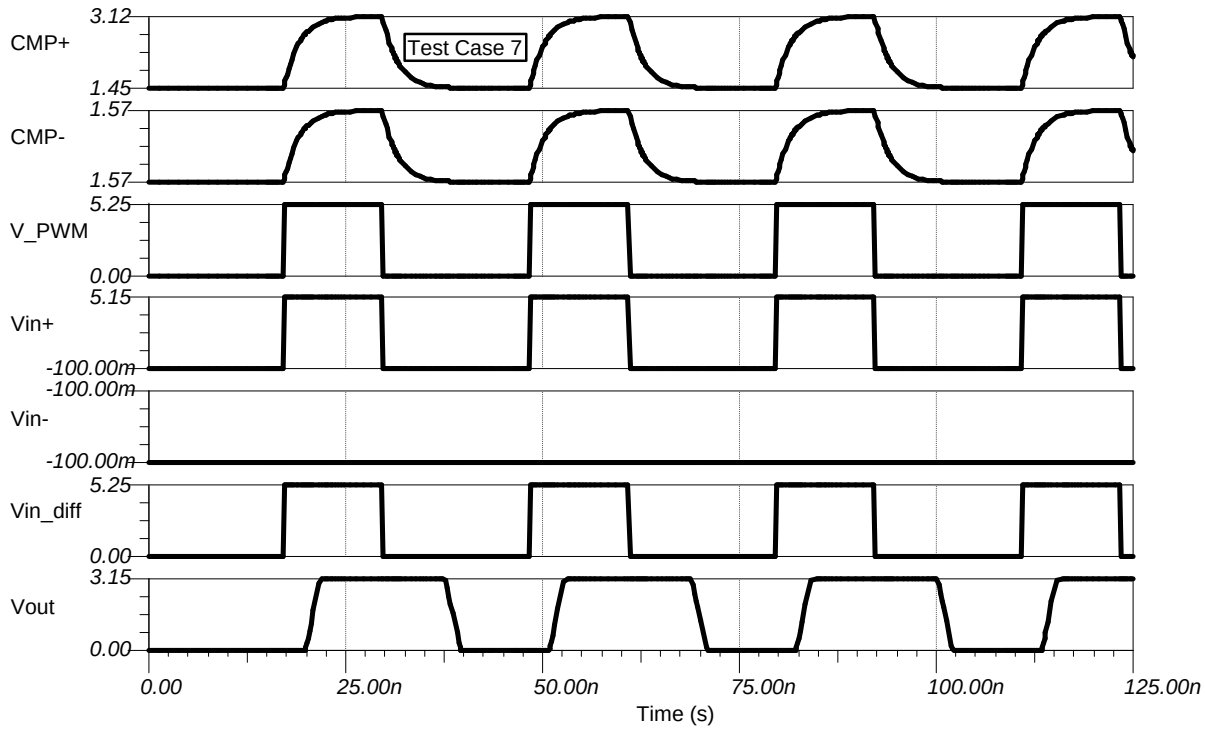


Figure 22. Test Case 7

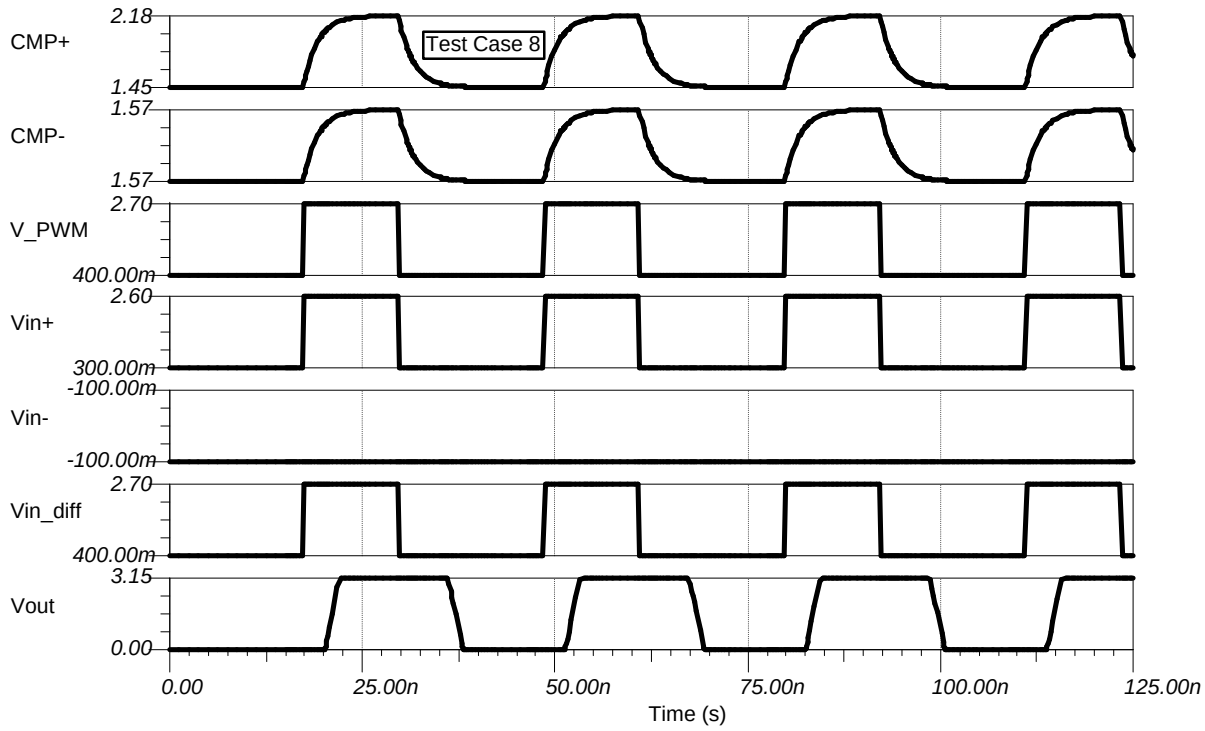


Figure 23. Test Case 8

5 Verification and Measured Performance

5.1 Transient Response

Figure 24 through Figure 31 show the measured transient response for each of the test cases listed in Table 5. The data was generated using a DG2020 device to input a square wave into Vin+ and a bench power supply to input a DC signal into Vin–. To reduce reflections between the DG2020 device and the printed circuit board (PCB), a 50-Ω resistor was placed from Vin+ to ground and the DG2020 device was configured to have an output impedance of 50 Ω. Notice that the measured transient response closely matches the simulated transient response of each test case. Also note that, at an input frequency of 32 MHz, Vin+ does not appear as a clean square wave and also Vin– appears to be varying, which is due to limitations of the measurement equipment and is not a result of the design.

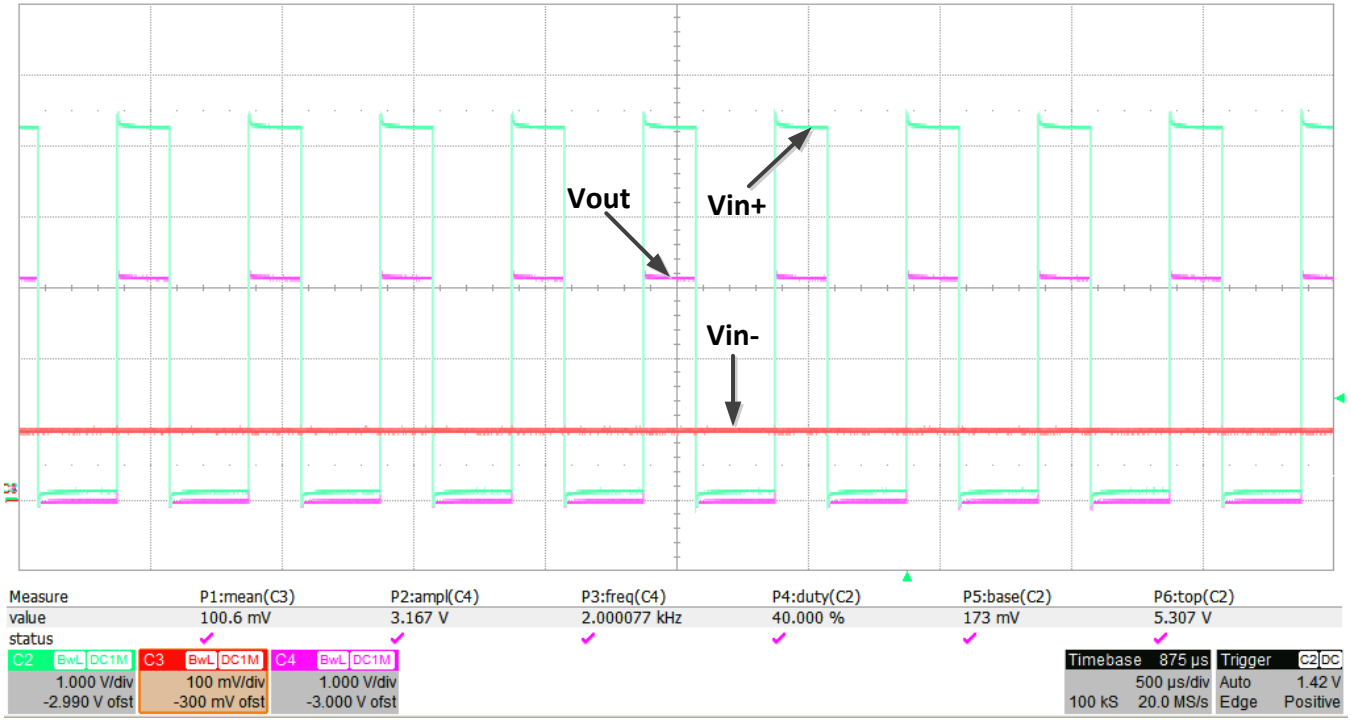


Figure 24. Transient Response of Test Case 1

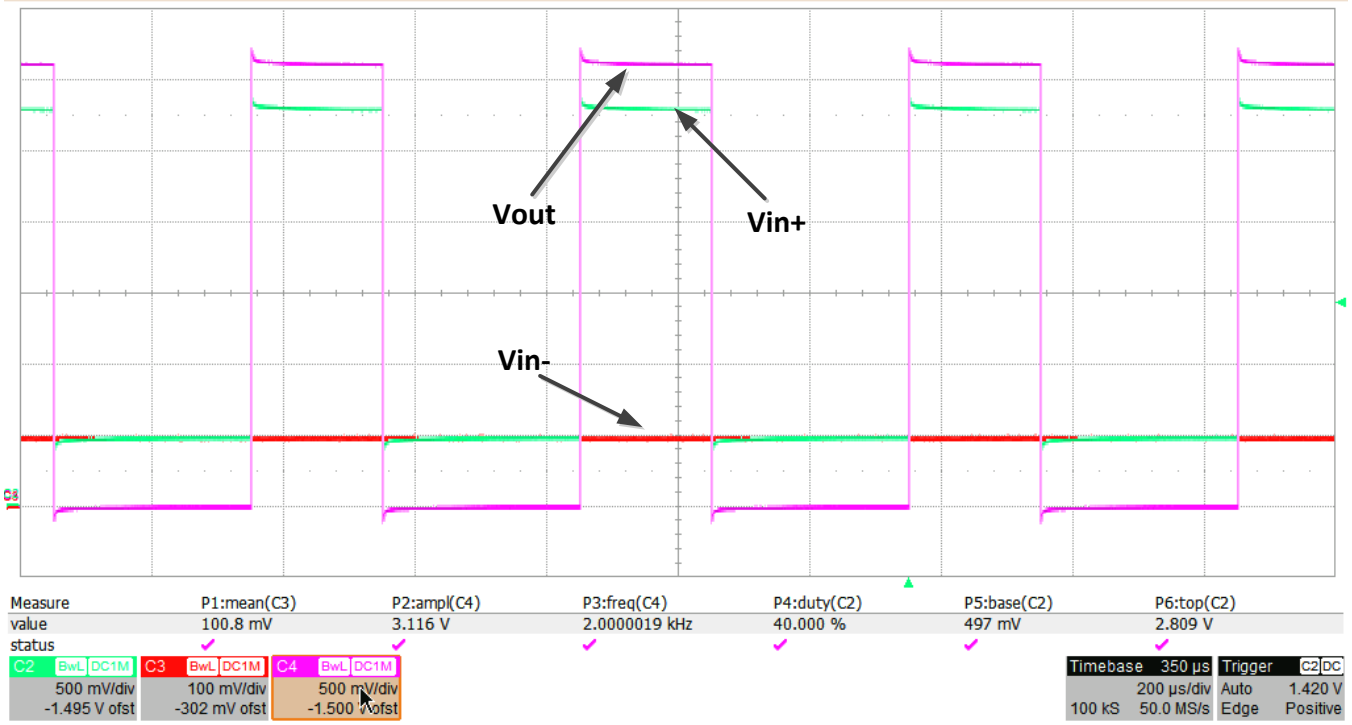


Figure 25. Transient Response of Test Case 2

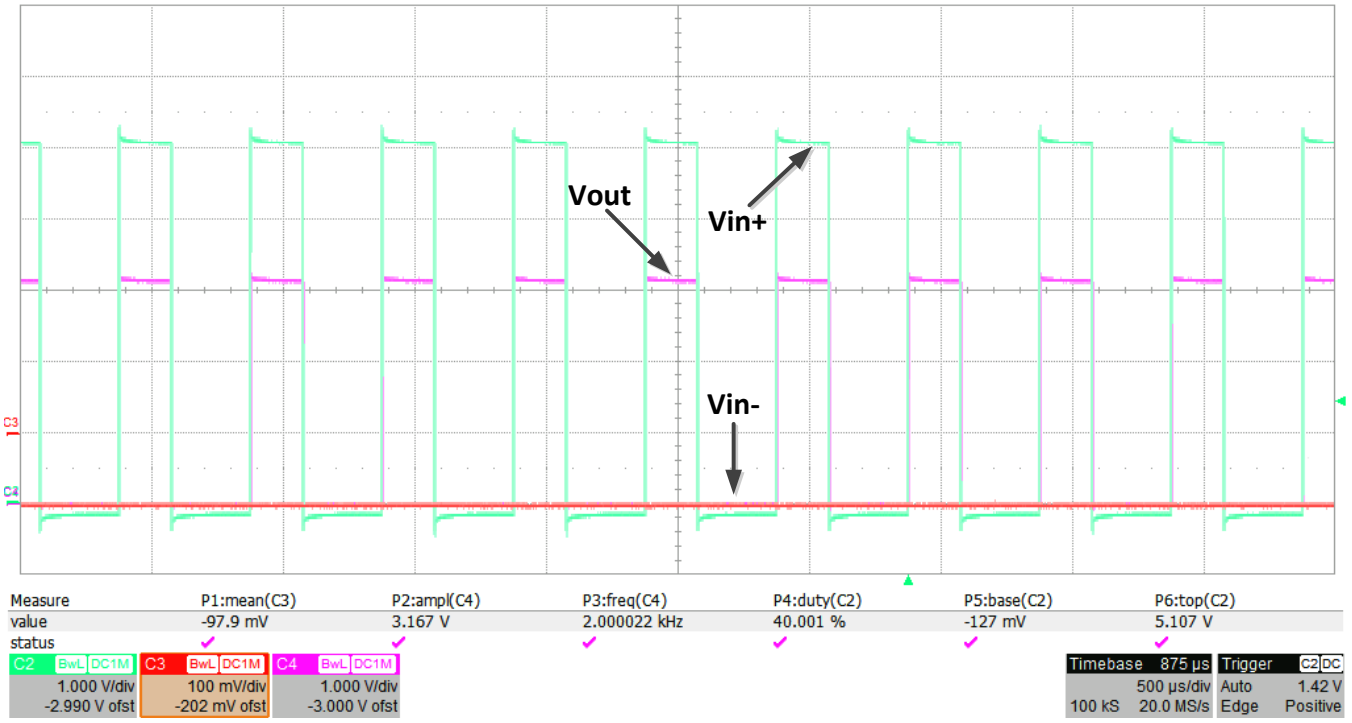


Figure 26. Transient Response of Test Case 3

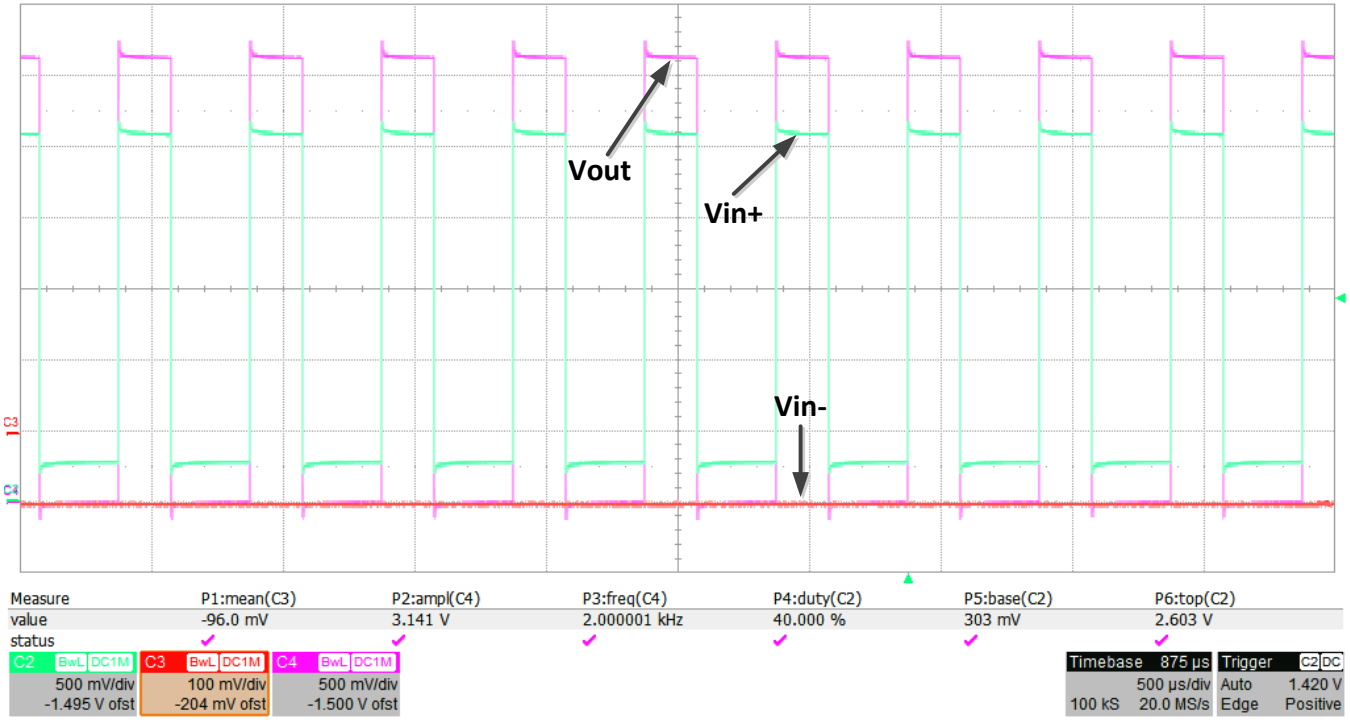


Figure 27. Transient Response of Test Case 4

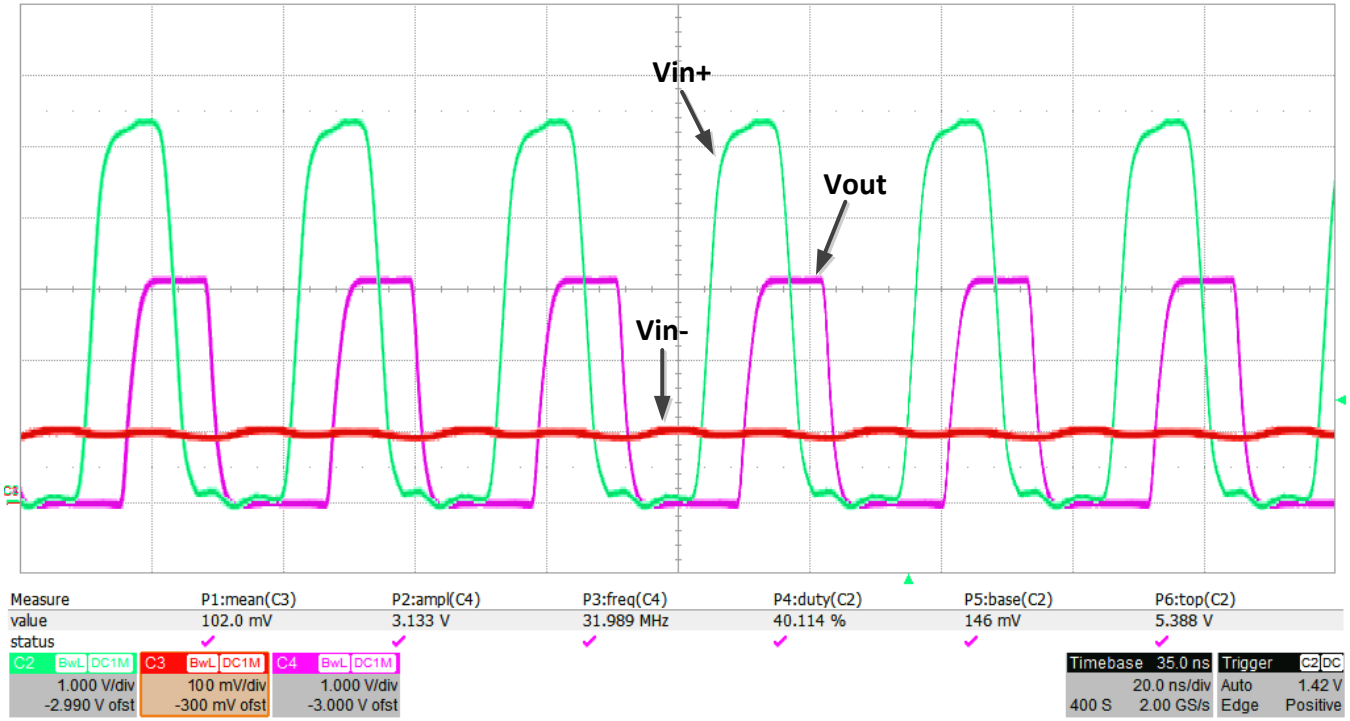


Figure 28. Transient Response of Test Case 5

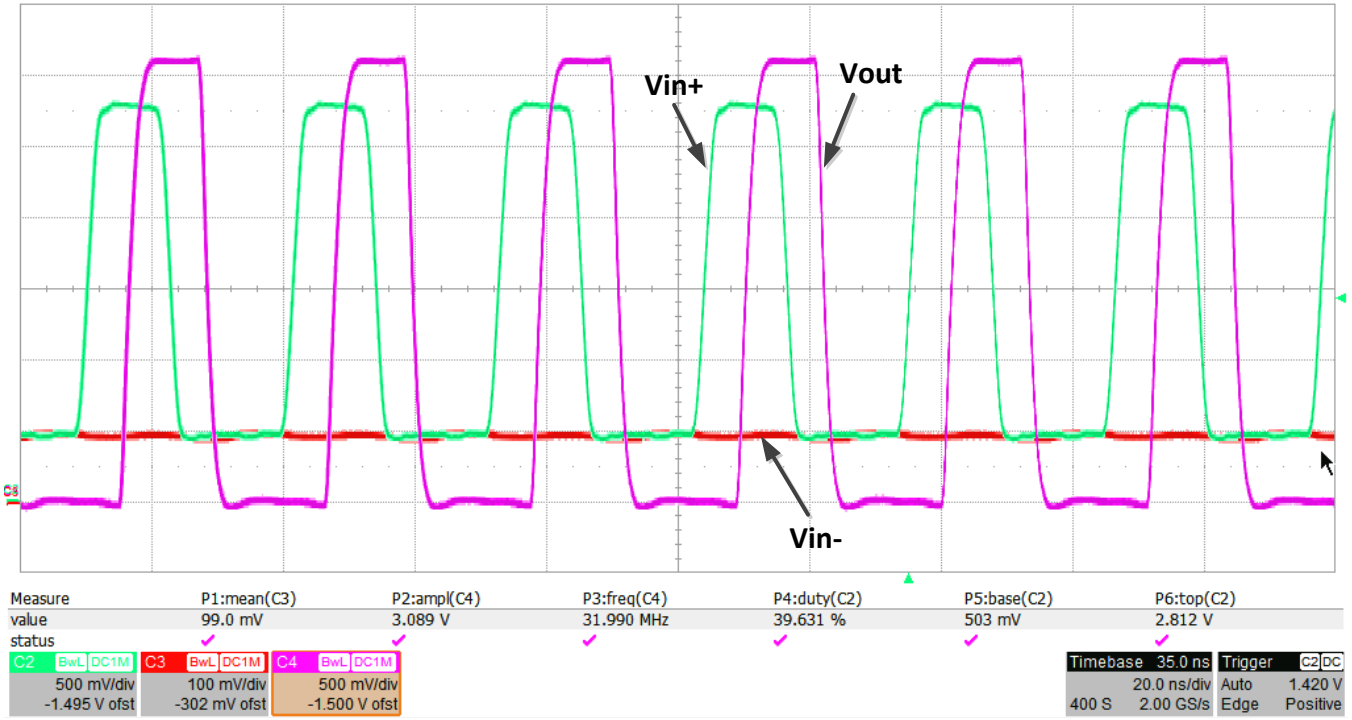


Figure 29. Transient Response of Test Case 6

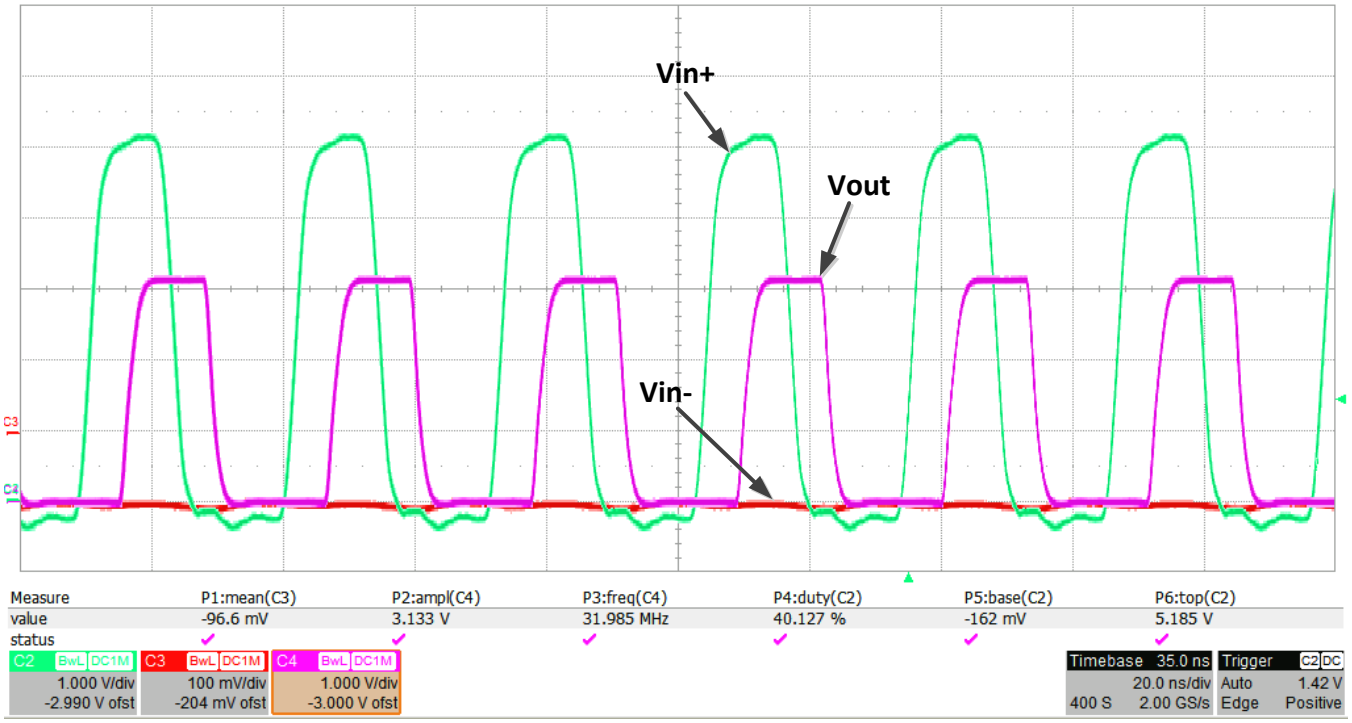


Figure 30. Transient Response of Test Case 7

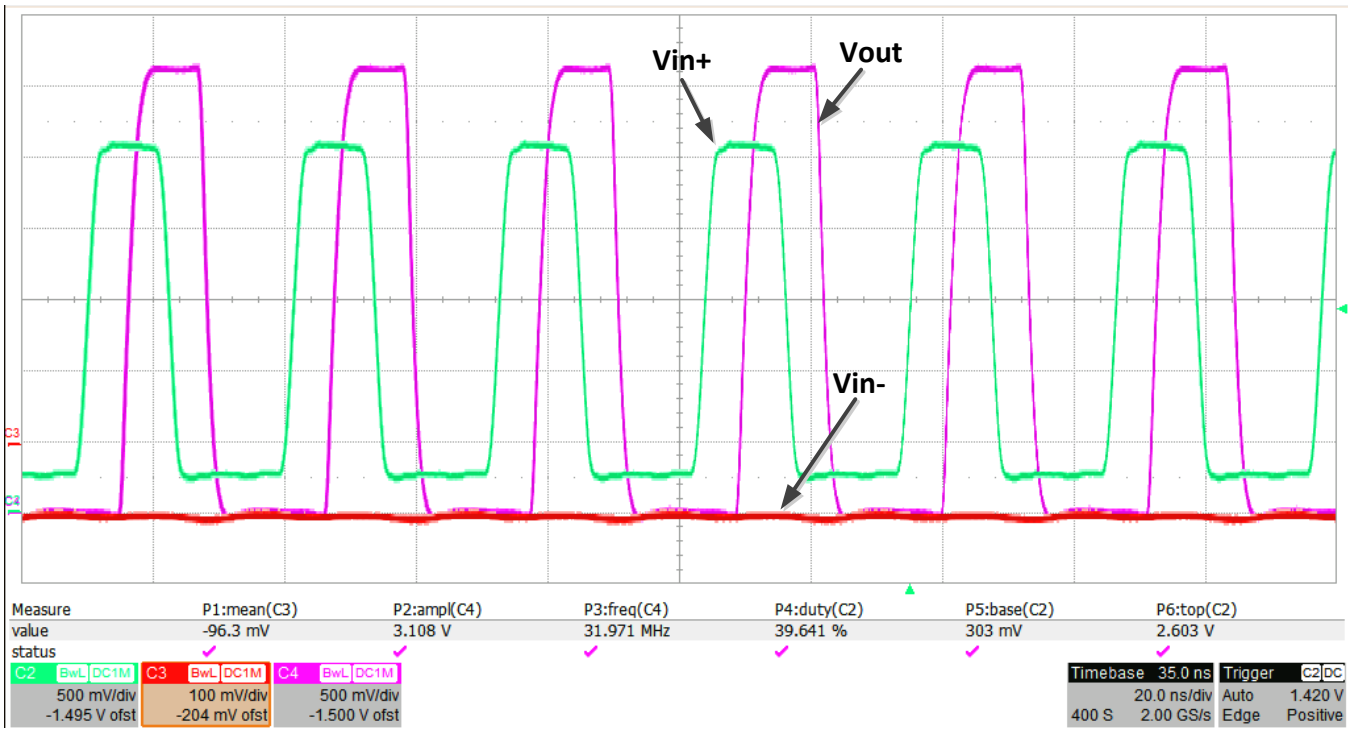


Figure 31. Transient Response of Test Case 8

Table 6 summarizes the measured performance of the design.

Table 6. Summary of Measured Performance

TEST CASE	FREQUENCY	INPUT VIL	INPUT VIH	INPUT VCM	INPUT DUTY CYCLE	COMPARATOR Vcc	DELAY	OUTPUT DUTY CYCLE
1	2 kHz	7 mV	5.2 V	100 mV	40%	3.135 V	3.3 ns	40%
2	2 kHz	397 mV	2.7 V	100 mV	40%	3.135 V	3.75 ns	40%
3	2 kHz	27 mV	5.288 V	–100 mV	40%	3.135 V	3.3 ns	40%
4	2 kHz	400 mV	2.7 V	–100 mV	40%	3.135 V	3.75 ns	40%
5	32 MHz	46 mV	5.288 V	100 mV	40%	3.135 V	3.3 ns	38%
6	32 MHz	391 mV	2.708 V	100 mV	40%	3.135 V	3.75 ns	39%
7	32 MHz	69 mV	5.234 V	–100 mV	40%	3.135 V	3.3 ns	39%
8	32 MHz	403 mV	2.703 V	–100 mV	40%	3.135 V	3.75 ns	38%

6 Modifications

The components selected for this design are based on the design goals outlined at the beginning of the design process. Selecting a short propagation delay comparator, such as the TLV3501, is critical in achieving the upper operating frequency of 32 MHz. The initial tolerances and temperature coefficient of C1 and C2 should be analyzed for their effects on voltages coupled into the comparator inputs. Ensure that all voltages remain within the common-mode voltage range of the selected comparator. By using cutoff frequencies a decade away from the desired pass-band frequencies, component sensitivities are minimized. Table 7 lists the maximum frequency possible based on propagation delay for rail-to-rail input comparators, which are optimal for this type of design based on a minimum duty cycle of 40% and single supply operation from 2.7 V < VCC < 5.5 V.

Table 7. Single Supply Comparators and Maximum Frequency for AC-Coupled Comparator

PART	PRI	CHANNELS	VCC MIN (V)	VCC MAX (V)	OUTPUT TYPE	Iq/CHANNEL (mA)	PROP DELAY (µs)	fmax (Hz)[1]
TLV3404	Yes	4	2.5	16	Open drain	0.00095	300	1333
TLV3402	Yes	2	2.5	16	Open drain	0.00095	300	1333
TLV3401	Yes	1	2.5	16	Open drain	0.00095	300	1333
TLV3704	Yes	4	2.7	16	Push-pull	0.001	240	1667
TLV3702	Yes	2	2.7	16	Push-pull	0.001	240	1667
TLV3701	Yes	1	2.7	16	Push-pull	0.001	240	1667
LMC7225	Yes	1	2	8	Open drain	1.2	29	13793
LMC7215	Yes	1	2	8	Push-pull	1.2	29	13793
TLV3494	Yes	4	1.8	5.5	Push-pull	0.0012	13.5	29630
TLV3492	Yes	2	1.8	5.5	Push-pull	0.0012	13.5	29630
TLV3491	Yes	1	1.8	5.5	Push-pull	0.0012	13.5	29630
LPV7215	Yes	1	1.8	5.5	Push-pull	0.013	12	33333
TLV7211	Yes	1	2.7	15	Push-pull	0.014	10	40000
LMC7221	Yes	1	2.7	15	Open drain	0.018	10	40000
LMC7211	Yes	1	2.7	15	Push-pull	0.014	10	40000
LMC6762	Yes	2	2.7	15	Push-pull	12.5	10	40000
LMV7291	Yes	1	1.8	5.5	Push-pull	0.016	1.3	307692
LMV762	Yes	2	2.7	5.25	Push-pull	0.7	0.27	1481481
LMV761	Yes	1	2.7	5.25	Push-pull	0.7	0.27	1481481
LMV7239	Yes	1	2.7	5.5	Push-pull	0.1	0.096	4166667
LMV7235	Yes	1	2.7	5.5	Open drain	0.1	0.096	4166667
TLV3502	Yes	2	2.7	5.5	Push-pull	5	0.012	33333333
TLV3501	Yes	1	2.7	5.5	Push-pull	5	0.012	33333333

(1) fmax based on 40% duty cycle

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIPD105.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIPD105.

7.3 PCB Layout Recommendations

Figure 32 shows the PCB layout for the design. Traces for the Vin+ and Vin– inputs are kept as balanced as possible to minimize an impedance mismatch between Vin+ and Vin–. All signal traces and most power traces are routed on the top layer to keep the bottom layer as solid as possible. The top and bottom layer are poured with a ground plane to provide a low impedance path for return currents and provide the shortest path back to ground. General PCB layout guidelines have been followed, such as traces being kept as short as possible and placing decoupling capacitors close to the supply pins of the device.

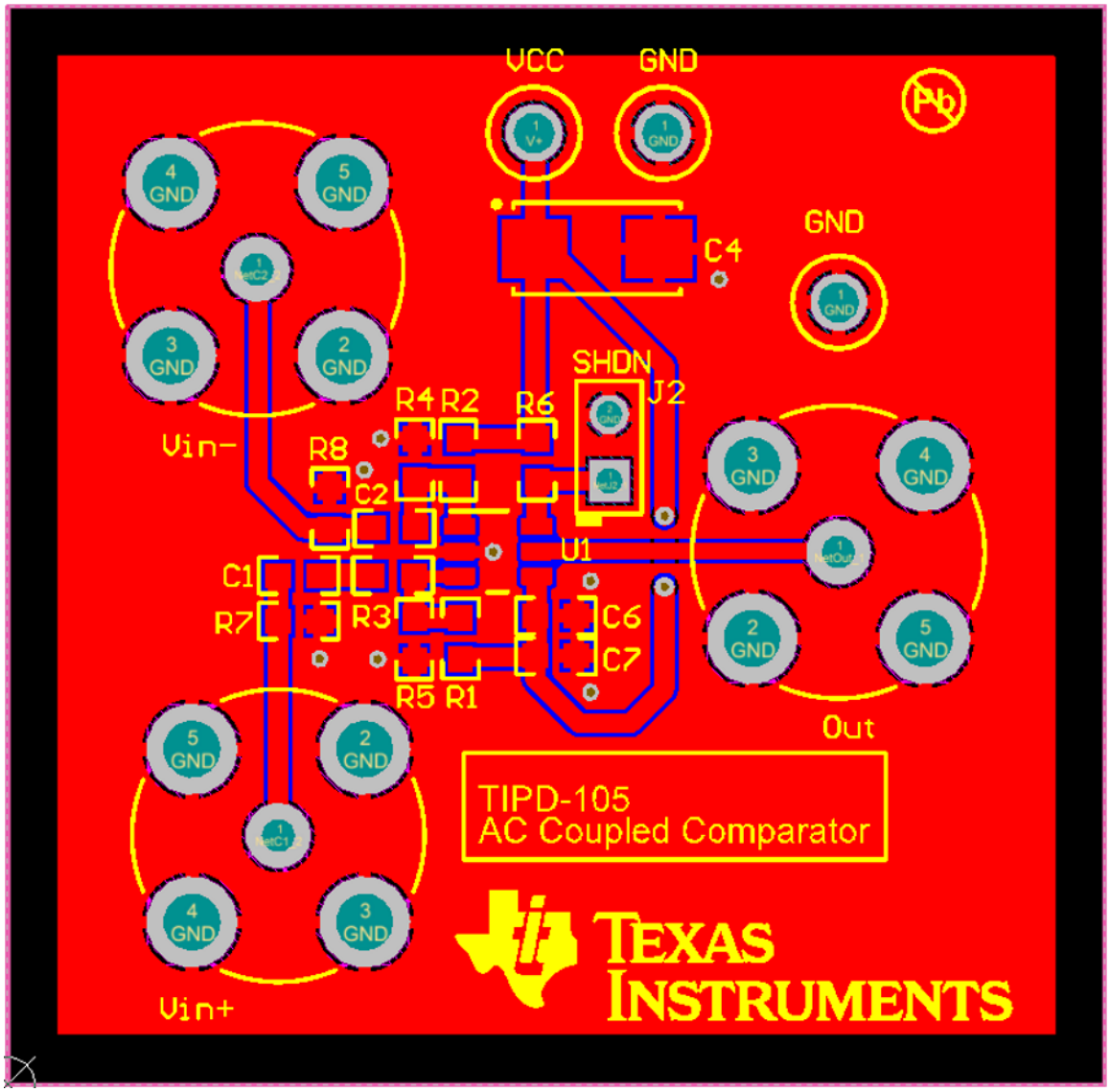


Figure 32. PCB Layout

7.4 Gerber Files

To download the Gerber files, see the design files at TIPD105.

8 Related Documentation

1. Texas Instruments, *TLV350x 4.5-ns, Rail-to-Rail, High-Speed Comparator in Microsize Packages*, TLV3501/TLV3502 Datasheet (SBOS321)

8.1 Trademarks

TINA-TI is a trademark of Texas Instruments.

9 About the Author

TIM GREEN has worked as an analog and mixed signal board/system design engineer, strategic marketing engineer, and linear applications engineer for over 31 years since earning a BSEE from the University of Arizona in 1981. He has focused on product areas such as brushless motor control, aircraft jet engine control, missile systems, power op amps, data acquisition systems, CCD cameras, and analog/mixed signal semiconductors. Tim's most recent experience focused on Power Audio for the automotive market. He is currently a senior analog applications engineer in precision analog linear applications at Texas Instruments, Tucson Design Center.

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Appendix A

A.10 TLV3501 Input Capacitance Test

Because a critical part of the design specification is high-frequency operation, the user must check that the TLV3501 SPICE macromodel matches the datasheet specifications for Ccm and Cdiff. Figure 33 shows a simple test circuit in which an AC source is swept through a known resistance, Rtest. The results show the 3-dB frequency caused by this known resistance and the input capacitance of the SPICE macromodel.

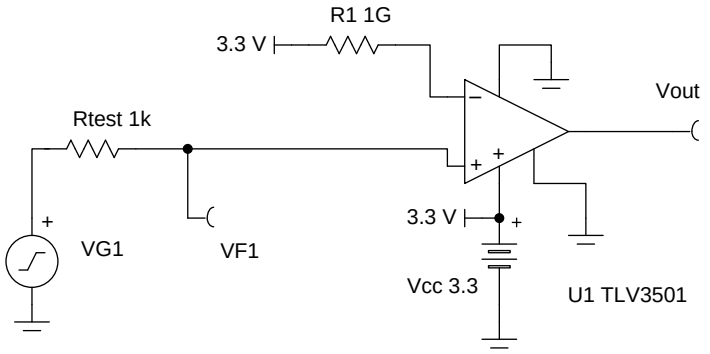

Figure 33. TLV3501 Input Capacitance Test Circuit

In Figure 34 the expected results of the test have been computed for the modeling of Ccm alone and the modeling of both Ccm and Cdiff.

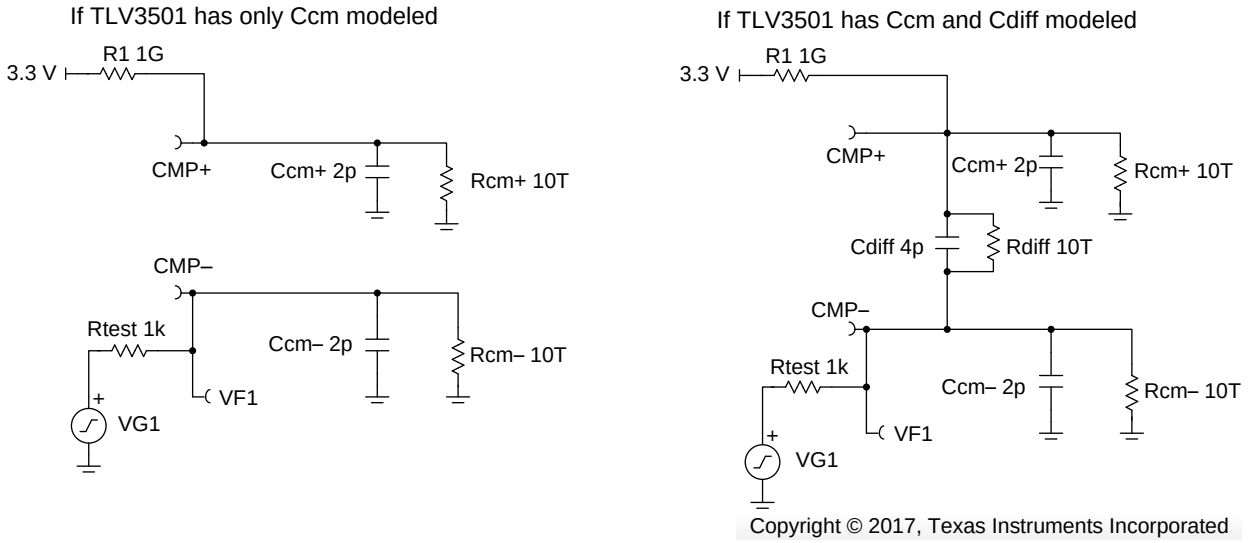

Figure 34. TLV3501 Input Capacitance Check

The results of the SPICE simulation in Figure 35 show that only Ccm has been modeled in the TLV3501 SPICE macromodel. To make sure the TIPD105 design works robustly in the real world, add a Cdiff of 4 pF external to the TLV3501 SPICE macromodel, as Figure 36 shows.

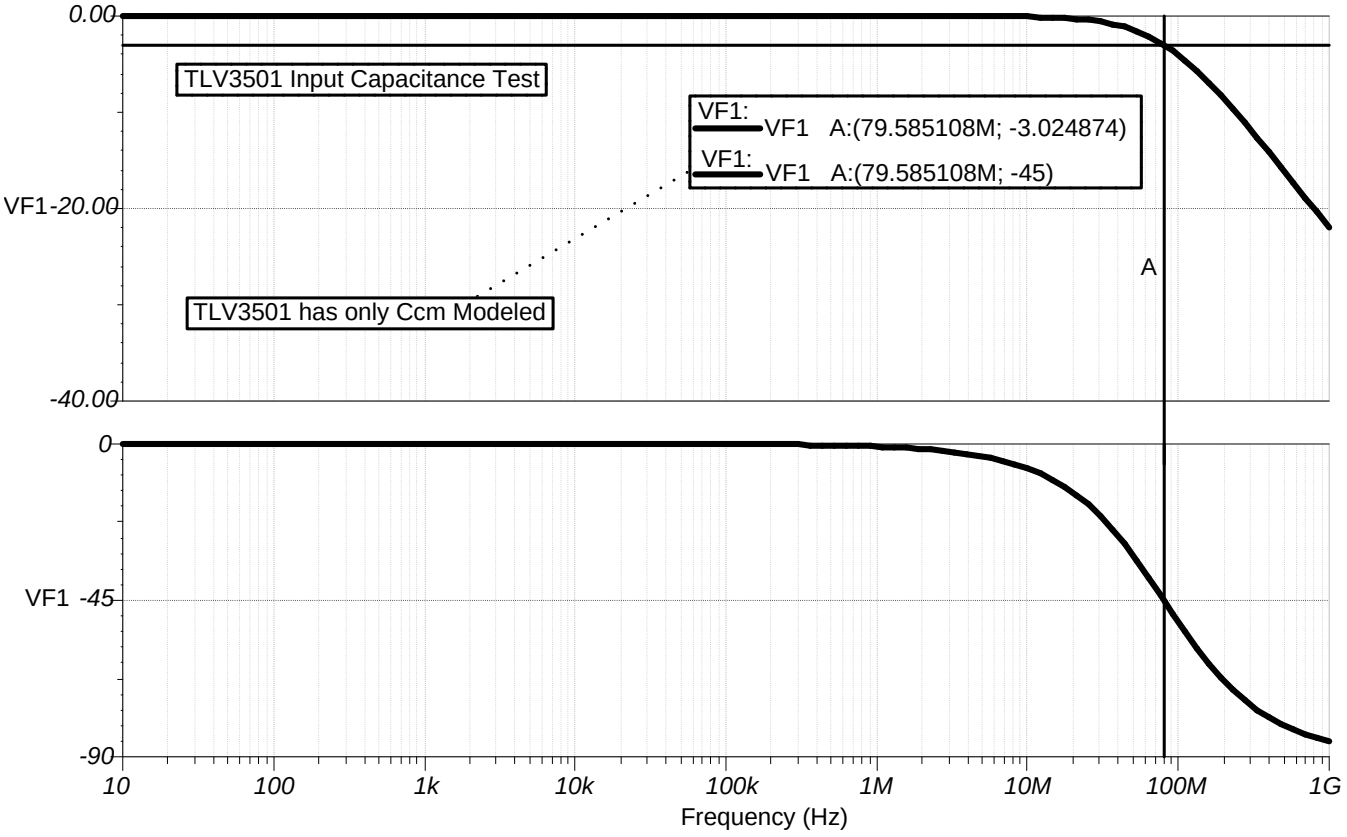

Figure 35. TLV3501 Input Capacitance Simulation Results

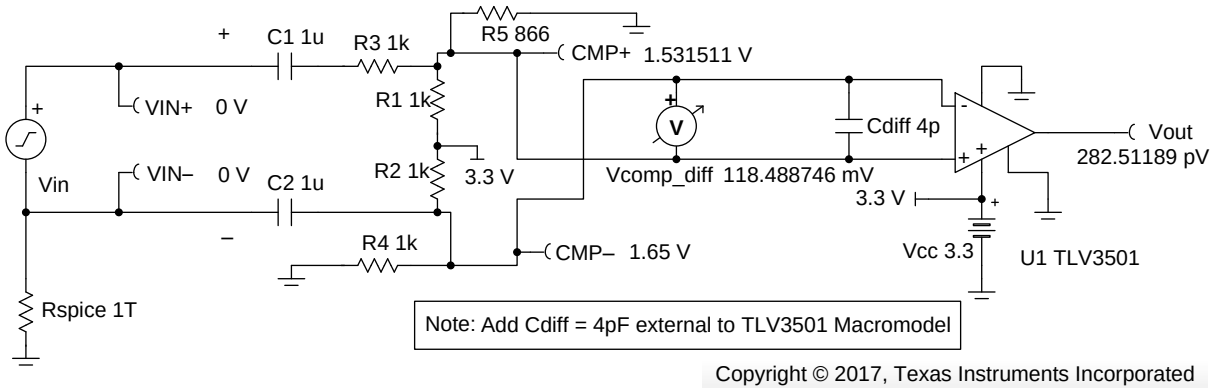

Figure 36. Modified TLV3501 Comparator for Proper Input Capacitance

A.11 Appendix (Continued)

A.11.1 Adjustable PWM Signal Source

To test the TIPD105 design, a PWM signal generator was created that is easy to adjust and use to test the final design (see Figure 37). This generator has an adjustable frequency, duty cycle, Voh (output high-voltage level), and Vol (output low-voltage level), which allows the designer to easily test all corner conditions of the specification for the implementation compliance of the final circuit.

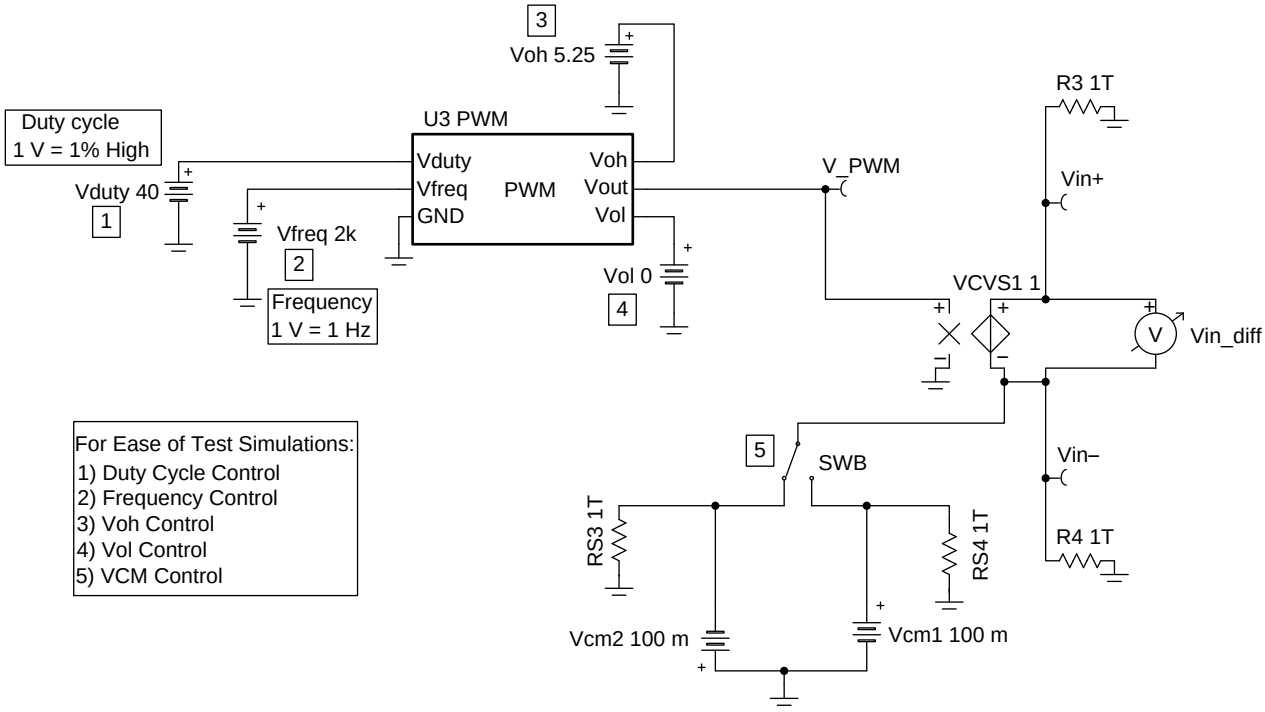

Figure 37. Transient Analysis PWM Source

Figure 38 shows the subcircuits used inside of the PWM macromodel. VCO is a SPICE-standard voltage-controlled oscillator, out of which the designer uses the triangle wave output scaled for 0 V to 1 V. The frequency is scaled for 1 V = 1 Hz. External to the macromodel, the duty cycle is scaled 0 V to 100 V for 0% to 100%, respectively. The duty cycle is scaled internally from 0 V to 1 V by VCVS2. An ideal comparator, VCVS1, compares the triangle waveform (0 V to 1 V) to the duty cycle setting (0 V to 1 V). The output high limits and output low limits, Voh and Vol, are set externally and become the limit values of U2, a voltage-controlled voltage source with clamp limits.

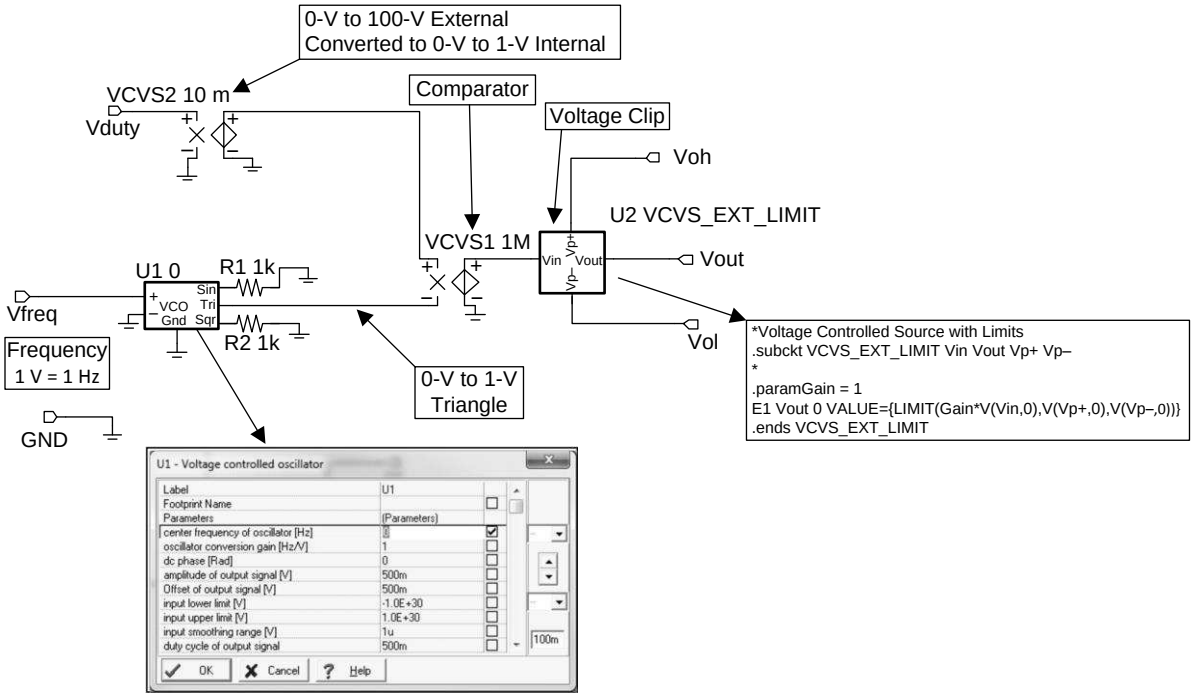

Figure 38. PWM Macromodel Details

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2013) to A Revision	Page
• Changed title from *AC Coupled Single Supply Comparator* to *AC-Coupled, Single-Supply Comparator Reference Design*	1
• Changed format from Word Document to .XML	1
• Added all figures to updated versions (changed line weights, colors to black, copyrights)	2
• Added new instruction and additional values for revised *Figure 6*	8
• Changed specified value of R3_min to 582 Ω from 681 Ω in revised *Figure 7*	9
• Added *Verification and Measured Performance* section	21
• Added *PCB Layout Recommendations section*	27

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