TFP101, TFP201, TFP401, TFP401A 2Pix/Clk Output Mode

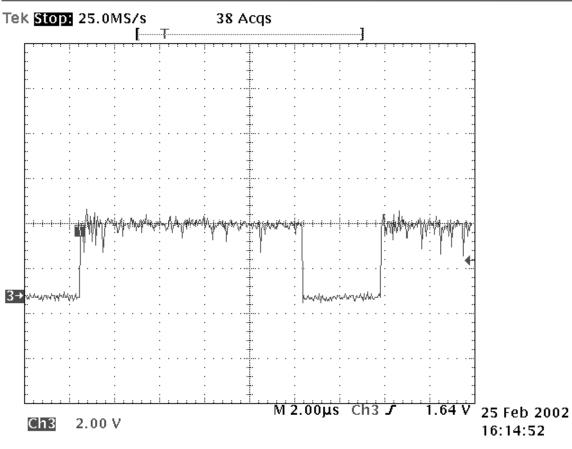*Digital Visual Interface*

ABSTRACT

This document explains the recommended configuration to operate the TFP101/201/401(A) devices in the 2Pixel/Clk mode.
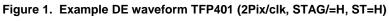
Introduction

When operating the TFP101/201/401(A) receivers in the 2Pixel/Clock mode, it is recommended to use the staggered outputs (STAG/ = 0V) mode. Due to certain timing differences, if the staggered output mode cannot be used, it is recommended that low output drive strength be used (ST = 0V).

Possible Issue

When the TFP101/201/401(A) receiver is operating in 2Pixel/Clock mode (PIXS=H), with non-staggered outputs (STAG/=H) and high output drive strength (ST=H) it is possible that when all 48 data outputs are switching simultaneously, some "dipping" can occur on other output signals such as DE, HSYNC or VSYNC. See Figure 1.
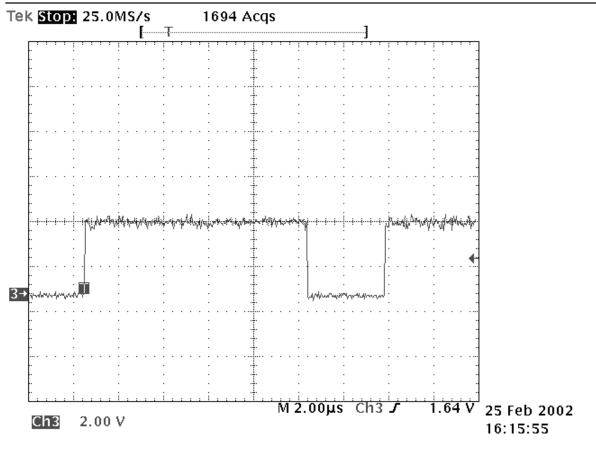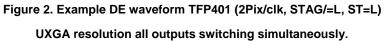
Figure 1. Example DE waveform TFP401 (2Pix/clk, STAG/=H, ST=H)

UXGA resolution all outputs switching simultaneously.

Time staggering the outputs greatly reduces the instantaneous current surge from the power supply needed to drive all outputs simultaneously in certain conditions. Under these conditions, this current surge can effect the signal levels of other outputs which could possibly cause a device downstream to interpret a wrong input signal depending on the input threshold level of that device.   See Figures 2 and 3.

Figure 2. Example DE waveform TFP401 (2Pix/clk, STAG/=L, ST=L)

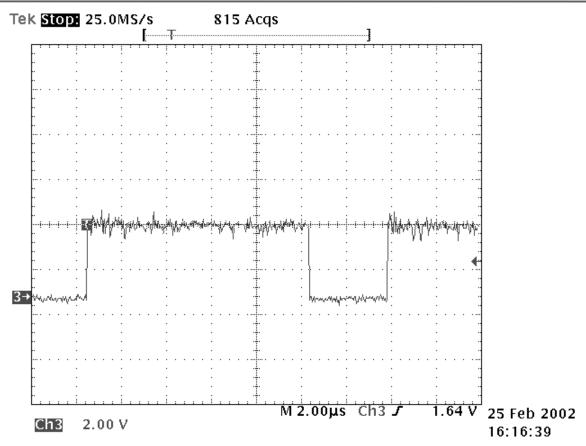**UXGA resolution all outputs switching simultaneously.**

Figure 3. Example DE waveform TFP401 (2Pix/clk, STAG/=L, ST=H)

UXGA resolution all outputs switching simultaneously.

Using the low output drive strength mode also reduces the current surge from the power supply, reducing the chances of having improper voltage levels on the other output signals. See Figure 4.
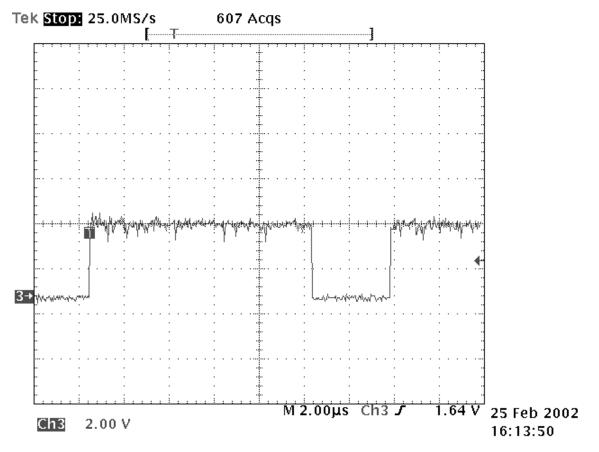

Figure 4. Example DE waveform TFP401 (2Pix/clk, STAG/=H, ST=L) UXGA resolution all outputs switching simultaneously.

Recommendations

If the system application requires that the TFP101/201/401(A) operate in the 2Pix/Clk mode with non-staggered outputs and high output drive strength, the following suggestions may be implemented into the system to improve system reliability.

Note: It is the responsibility of the individual system designer to verify correct operation.

SCHMITT-TRIGGER

A Schmitt-trigger can be used for the CTL signals to ensure that the VIH and VIL voltage levels are appropriate for a device accepting the outputs of the TFP101/201/401(A) device.
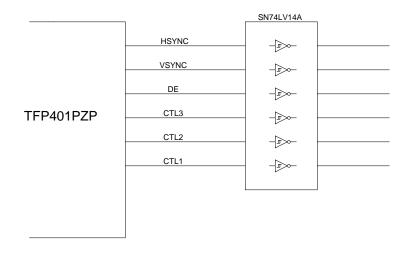
Example

Figure 5. Example Schmitt-trigger application

Note: The Texas Instruments SN74LV14A is a Hex Schmitt-Trigger Inverter.

At 3.3V, V_{IH} = 2.3V, V_{IL} = 0.99V.

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