TEXAS INSTRUMENTS

Application Report
SLLA425–August 2018

SN65DSI86 Programming Guide

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ABSTRACT

This document includes guidelines and recommendations for programming the registers of the SN65DSI86. The register settings are based on the designers system as well as the eDP panel and MIPI DSI source. Refer to the SN65DSI86 datasheet (SLLSEH2) for the register map for the exact meanings of registers.

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Trademarks

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1 Overview

The SN65DSI86 will be referred to as DSI86 in this document. The DSI86 is a MIPI DSI-to-eDP bridge device that supports video modes in forward direction. The DSI86 is primarily targeted at portable applications such as tablets and smart phones and tablets that utilize the MIPI DSI video format. The DSI86 can be used between a GPU/CPU with a DSI output and a video panel with an embedded DisplayPort.

2 Information Required

2.1 EDID Information

The EDID contains information that is needed to calculate the register values of the DSI86. The following table contains all the EDID information that will be needed from the EDID.

Table 1. EDID Information

Category	Units
Pixel Clock	MHz
Horizontal Active	Pixels
Horizontal Blanking	Pixels
Vertical Active	Lines
Vertical Blanking	Lines
Horizontal Sync Offset or FrontPorch	Pixels
Horizontal Sync Pulse Width	Pixels
Vertical Sync offset or FrontPoarch	Lines
Vertical Sync Pulse Width	Lines
Horizontal Sync Polarity	Positive/Negative
Vertical Sync Polarity	Positive/Negative
Bits per Pixel	#(e.g. 16,18,24)
eDP Version	#(1.0, 1.1, 1.2, 1.3 1.4)
Number of DP lanes for DP panel	#(e.g. 1,2,4)
Datarate Supported	Gbps(1.62 Gbps, 2.16 Gbps, 2.43 Gbps, 2.70 Gbps, 3.24 Gbps, 4.32 Gbps or 5.40 Gbps)

2.2 DSI Information

The following DSI information is required to determine the various register values of the DSI86.

Table 2. DSI Information

Category	Units
DSI A Lanes	#(e.g. 1,2,3,4)
DSI B Lanes	#(e.g. 1,2,3,4)
DSI Channel Mode	Dual/Single
Maximum DSI Clock Frequency	MHz

2.3 DSI86

To program the DSI86 for your application you must know if what the reference clock frequency is in order to program one of the registers. the reference clock frequency is in MHz. The supported reference clock frequencies are 12 MHz, 19.2 MHz, 26 MHz, 27 MHz and 38.4 MHz.

3 Calculations

This section is used to calculate the values that will be needed in later sections to program the DSI86 registers.

3.1 Stream Bit Rate

The Stream Bit rate is a function of pixel clock frequency and the amount of bits per pixel. this stream bit is used to calculate the minimum number of DSI lanes.

$$Stream\ \ Bit\ \ Rate\ =\ PixelClock\ \times\ bpp \tag{1}$$

3.2 eDP Total Bit Rate

The eDP total bit rate is the total bits that are usable coming out of the DSI86. The eDP total bit rate is a function of # of eDP lanes and bit rate. The multiplication by 0.8 is due to the 8b/10b encoding using in eDP.

$$eDPTotalBitRate = \#\_of\_eDP\_Lanes \;\; x \;\; DataRate \; x \;\; 0.8 \tag{2}$$

3.3 Minimum Number of eDP Lanes

To calculate the minimum number of eDP lanes you must satisfy the equation below. For example, if the EDP_Total_Bit_Rate = 4.7 Gbps and the eDP_Daterate_Supported = 2.43 Gbps then the minimum number of EDP_Lanes is 2.

$$eDP\_Datarate\_Supportes \geq (eDP\_Total\_Bit\_Rate \; / \; eDP\_Lanes) \tag{3}$$

3.4 Minimum DSI Lanes and DSI Clock Frequency

The Minimum DSI Clock Frequency is calculated using the maximum DSI Clock the panel and the stream bit rate. The maximum DSI Clock is the going to be 750 MHz or less because the DSI86 can only support up to 750 MHz clock frequency. The minimum number of DSI lanes is calculated the formula below. the Min_number_of_DSI_Lanes is rounded up to the nearest whole number.

$$Min\_number\_of\_DSI\_Lanes \;\; = Stream\_Bit\_Rate \; / \; (2 \;\; x \;\; max\_DSI\_Clock) \tag{4}$$

The minimum required DSI clock frequency is a function of stream bit rate and minimum number of DSI lanes. the equation is posted below to calculate the minimum required DSI clock frequency.

$$Min\_Required\_DSI\_Clock\_Frequency = \;\; Stream\_Bit\_Rate \; / \; (Min\_Number\_DSI\_Lanes \;\; x \;\; 2) \tag{5}$$

When using the REFCLK as the clock source, any DSI Clock frequency is supported, but if the clock source was instead the DSI A clock, then the required DSI Clock frequency would need to change to a frequency supported by the DSI86. When operating in this mode, any one of the following DSI A clock frequencies can be used: 384 MHz, 416 MHz, 460.8 MHz, 468 MHz, or 486 MHz. In most cases, a eDP panel would support some variation from the ideal pixel clock frequency.

3.5 Video Format Parameters

Parameter	Abbreviation	Equation/Source
Horizontal Sync Polarity	HPOL	From the EDID
Horizontal Sync Pulse Width	HPW	From the EDID
Horizontal Back Porch	HBP	=HBL - HPW - HFP
Horizontal Active Line	HACT	From the EDID
Horizontal Front Porch	HFP	From the EDID
Horizontal Blanking	HBL	From the EDID
Horizontal Total	HTOTAL	=HPW + HBP + HACT +HFP
Vertical Sync Polarity	VPOl	From the EDID
Vertical Sync Pulse Width	VPW	From the EDID
Vertical Back Porch	VBP	=VBL - VPW - VFP
Vertical Active Line	VACT	From the EDID
Vertical Front Porch	VFP	From the EDID
Vertical Blanking	VBL	From the EDID
Vertical Active Line	VTOTAL	=VPW + VBP + VACT + VFP

4 Register Programming

The following section covers the order the used to program the registers of the DSI86.

4.1 Data Rate Programming

The supported data rates for the DSI86 are 1.62 Gbps(RBR), 2.16 Gbps, 2.43 Gbps, 2.7 Gbps(HBR), 3.24 Gbps, 4.32 Gbps or 5.4 Gbps(HBR2). To program the data rate into the DSI86, the user needs to program the DP_DATARATE register (0x94 bits 7:5) per Table 3.

Table 3. DSI86 Data Rate Programming

Data Rate	Register Value
1.62 Gbps(RBR)	001
2.16 Gbps	010
2.43 Gbps	011
2.70 Gbps(HBR)	100
3.24 Gbps	101
4.32 Gbps	110
5.40 Gbps(HBR2)	11

If you are using eDP data rates that are not 1.62 Gbps, 2.7 Gbps or 5.4 Gbps such as 2.16 Gbps, 2.43 Gbps, 3.24 Gbps or 4.32 Gbps, then the user must set the LINK_RATE_SET_EN register(0x99 bits 7) to a 1, and then set the LINK_RATE_SET register(0x99 bit 2:0) per Table 4.

Table 4. eDP Data Rates

Data Rate	Register Value
2.16 Gbps	010
2.43 Gbps	011
3.24 Gbps	101
4.32 Gbps	110

4.2 ASSR

Table 5 is a sequence with register values to program the DSI86. This table includes the ASSR enabling register settings.

Table 5. ASSR Registers

Register Purpose	Register Address	Bit Number	Register Value

Reference Clock Frequency	0x0A	3	DPPLL_CLK_SRC = 0 (Ref clock used)
			DPPLL_CLK_SRC = 1 (No Ref clock)

		1:2	000=12 MHz 000 = Continuous DSIA CLK at 468 MHz
			001 = 19.2 MHz (Default) 001 = Continuous DSIA CLK at 384 MHz
			010 = 26 MHz 010 = Continuous DSIA CLK at 416 MHz
			011 = 27 MHz 011 = Continuous DSIA CLK at 486 MHz
			100 = 38.4 MHz 100 = Continuous DSIA CLK at 460.8 MHz
DSI Mode	0x10	7	LEFT_RIGHT_PIXELS
			0 = DSI channel A receives ODD pixels and channel B receives EVEN (default)
			1 = DSI channel A receives LEFT image pixels and channel B receives RIGHT image pixels
		6:5	DSI_CHANNEL_MODE
			00 = Dual-channel DSI receiver
			01 = Single channel DSI receiver A (default)
		4:3	CHA_DSI_LANES Note: Unused DSI inputs pins on the DSI86 should be left unconnected.
			This field controls the number of lanes that are enabled for DSI Channel A.
			00 = Four lanes are enabled
			01 = Three lanes are enabled
			10 = Two lanes are enabled
			11 = One lane is enabled (default)
		2:1	CHB_DSI_LANES
			This field controls the number of lanes that are enabled for DSI Channel B.
			00 = Four lanes are enabled
			01 = Three lanes are enabled
			10 = Two lanes are enabled
			11 = One lane is enabled (default)
DSI A Clock	0x12	7:0	CHA_DSI_CLK_RANGE This field specifies the DSI clock frequency range in 5-MHz increments for DSI Channel A clock. The DSI86 estimates the DSI clock frequency using the REFCLK frequency determined at the rising edge of EN and updates this field accordingly. Software can override this value. If the CHA_DSI_CLK_RANGE is not loaded before receiving the first DSI packet, the DSI86 uses the first packet to estimate the DSI_CLK frequency and loads this field with this estimate. This first packet may not be received; thus, the host should send a first dummy packet (such as DSI read or write to register 0x00). This field may be written by the host at any time. Any non-zero value written by the host is used instead of the automatically estimated value. 0x00 through 0x07: Reserved 0x08 = 40 ≤ frequency < 45 MHz 0x09 = 45 ≤ frequency < 50 MHz . . . 0x96 = 750 ≤ frequency < 755 MHz 0x97 through 0xFF: Reserved

Table 5. ASSR Registers (continued)

Register Purpose	Register Address	Bit Number	Register Value
DSI B Clock	0x13	7:0	CHB_DSI_CLK_RANGE This field specifies the DSI clock frequency range in 5-MHz increments for DSI Channel B clock. The DSI86 estimates the DSI clock frequency using the REFCLK frequency determined at the rising edge of EN and updates this field accordingly. Software can override this value. If the CHB_DSI_CLK_RANGE is not loaded before receiving the first DSI packet, the DSI86 uses the first packet to estimate the DSI_CLK frequency and loads this field with this estimate. This first packet may not be received; thus, the host should send a first dummy packet (such as DSI read or write to register 0x00). This field may be written by the host at any time. Any non-zero value written by the host is used instead of the automatically estimated value. 0x00 through 0x07: Reserved 0x08 = 40 ≤ frequency < 45 MHz 0x09 = 45 ≤ frequency < 50 MHz . . . 0x96 = 750 ≤ frequency < 755 MHz 0x97 through 0xFF: Reserved
DP Datarate	0x94	7:5	DP_DATARATE
			000 = Not Configured (Default)
			001 = 1.62 Gbps per lane (RBR)
			010 = 2.16 Gbps per lane
			011 = 2.43 Gbps per lane
			100 = 2.70 Gbps per lane (HBR)
			101 = 3.24 Gbps per lane
			110 = 4.32 Gbps per lane.
			111 = 5.4 Gbps per lane (HBR2)
Enable PLL	0x0D	0	DP_PLL_EN
			0 = PLL disabled (default)
			1 = PLL enabled
ASSR	0x64		0x1
	0x74		0x0
	0x75		0x1
	0x76		0x0A
	0x77		0x1
	0x78		0x81
Enable enhanced frame and ASSR	0x5A		0x5
Number of DP Lanes	0x93	5:4	DP_NUM_LANES.
			00 = Not Configured. (Default)
			01 = 1 DP lane.
			10 = 2 DP lanes.
			11 = 4 DP lanes.
Start Semi-Auto Link Training	0x96	3:0	0x0A

Table 5. ASSR Registers (continued)

Register Purpose	Register Address	Bit Number	Register Value
CHA Active Line Length	0x20	7:0	CHA_ACTIVE_LINE_LENGTH_LOW: When the DSI86 is configured for a single DSI input, this field controls the length in pixels of the active horizontal line for Channel A. When configured for Dual DSI Inputs in Odd/Even mode, this field controls the number of odd pixels in the active horizontal line that are received on DSI channel A. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of left pixels in the active horizontal line that are received on DSI channel A. The value in this field is the lower 8 bits of the 12-bit value for the horizontal line length. This field defaults to 0x00. Note: When the DSI86 is configured for dual DSI inputs in Left/Right mode and LEFT_CROP field is programmed to a value other than 0x00, the CHA_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Left portion of the line after LEFT_CROP has been applied.
	0x21	3:0	CHA_ACTIVE_LINE_LENGTH_HIGH: When the DSI86 is configured for a single DSI input, this field controls the length in pixels of the active horizontal line for Channel A. When configured for Dual DSI Inputs in Odd/Even mode, this field controls the number of odd pixels in the active horizontal line that are received on DSI channel A. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of left pixels in the active horizontal line that are received on DSI channel A. The value in this field is the upper 4 bits of the 12-bit value for the horizontal line length. This field defaults to 0x00. Note: When the DSI86 is configured for dual DSI inputs in Left/Right mode and LEFT_CROP field is programmed to a value other than 0x00, the CHA_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Left portion of the line after LEFT_CROP has been applied.
CHB Active Line Length	0x22	7:0	CHB_ACTIVE_LINE_LENGTH_HIGH: When configured for Dual DSI Inputs in Odd/Even mode, this field controls the number of even pixels in the active horizontal line that are received on DSI channel B. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of right pixels in the active horizontal line that are received on DSI channel B. The value in this field is the upper 4 bits of the 12-bit value for the horizontal line length. This field defaults to 0x00. Note: When the DSI86 is configured for dual DSI inputs in Left/Right mode and RIGHT_CROP field is programmed to a value other than 0x00, the CHB_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Right portion of the line after RIGHT_CROP has been applied.
	0x23	3:0	CHA_VERTICAL_DISPLAY_SIZE_LOW: This field controls the vertical display size in lines for Channel A. The value in this field is the lower 8 bits of the 12-bit value for the vertical display size. This field defaults to 0x00.
Vertical Active Size	0x24	7:0	CHA_VERTICAL_DISPLAY_SIZE_LOW: This field controls the vertical display size in lines for Channel A. The value in this field is the lower 8 bits of the 12-bit value for the vertical display size. This field defaults to 0x00.
	0x25	3:0	CHA_VERTICAL_DISPLAY_SIZE_HIGH: This field controls the vertical display size in lines for Channel A. The value in this field is the upper 4 bits of the 12-bit value for the vertical display size. This field defaults to 0x00.

Table 5. ASSR Registers (continued)

Register Purpose	Register Address	Bit Number	Register Value
Horizontal Pulse Width	0x2C	7:0	CHA_HSYNC_PULSE_WIDTH_LOW: This field controls the width in pixel clocks of the HSync Pulse Width for Channel A. The value in this field is the lower 8 bits of the 15-bit value for HSync Pulse width. This field defaults to 0x00.
	0x2D	7	CHA_HSYNC_POLARITY
			0 = Active High Pulse. Synchronization signal is high for the sync pulse width. (default)
			1 = Active Low Pulse. Synchronization signal is low for the sync pulse width.
		6:0	CHA_HSYNC_PULSE_WIDTH_HIGH
			This field controls the width in pixel clocks of the HSync Pulse Width for Channel A. The value in this field is the upper 7 bits of the 15-bit value for HSync Pulse width. This field defaults to 0x00.
Vertical Pulse Width	0x30	7:0	CHA_VSYNC_PULSE_WIDTH_LOW: This field controls the length in lines of the VSync Pulse Width for Channel A. The value in this field is the lower 8 bits of the 15-bit value for VSync Pulse width. This field defaults to 0x00. The total size of the VSYNC pulse width must be at least 1 line.
	0x31	7	CHA_VSYNC_POLARITY
			0 = Active High Pulse. Synchronization signal is high for the sync pulse width. (Default)
			1 = Active Low Pulse. Synchronization signal is low for the sync pulse width.
		6:0	CHA_VSYNC_PULSE_WIDTH_HIGH: This field controls the width in lines of the VSync Pulse Width for Channel A. The value in this field is the upper 7 bits of the 15-bit value for VSync Pulse width. This field defaults to 0x00. The total size of the VSYNC pulse width must be at least 1 line.
Horizontal Back Porch (HBP)	0x34	7:0	CHA_HORIZONTAL_BACK_PORCH: This field controls the time in pixel clocks between the end of the HSync Pulse and the start of the active video data for Channel A. This field defaults to 0x00.
Vertical Back Porch (VBP)	0x36	7:0	CHA_VERTICAL_BACK_PORCH: This field controls the number of lines between the end of the VSync Pulse and the start of the active video data for Channel A. This field defaults to 0x00. The total size of the Vertical Back Porch must be at least 1 line.
Horizontal Front Porch (HFP)	0x38	7:0	CHA_HORIZONTAL_FRONT_PORCH: This field controls the time in pixel clocks between the end of the active video data and the start of the HSync Pulse for Channel A. This field defaults to 0x00.
Vertical Front Porch (VFP)	0x3A	7:0	CHA_VERTICAL_FRONT_PORCH: This field controls the number of lines between the end of the active video data and the start of the VSync Pulse for Channel A. This field defaults to 0x00. The total size of the Vertical Front Porch must be at least 1 line.
Bit Per Pixel	0x5B	1	ENCH_FRAME_PATT
			0 = SR BF BF SR or BS BF BF BS (Default)
			1 = SR CP CP SR or BS CP CP BS
		0	DP_18BPP_EN: If this field is set, then 18BPP format will be transmitted over eDP interface regardless of the DSI pixel stream data type format.
			0 = 24BPP RGB. (default)
			1 = 18BPP RGB

Table 5. ASSR Registers (continued)

Register Purpose	Register Address	Bit Number	Register Value
Color Bar	0x3C	4	COLOR_BAR_EN: When this bit is set, the DSI86 generates a video test pattern on DisplayPort based on the values programmed into the Video Registers for Channel A.
			0 = Transmit of SMPTE color bar disabled. (default)
			1 = Transmit of SMPTE color bar enabled.
		2:0	COLOR_BAR_PATTERN:
			000 = Vertical Colors: 8 Color (Default)
			001 = Vertical Colors: 8 Gray Scale
			010 = Vertical Colors: 3 Color
			011 = Vertical Colors: Stripes
			100 = Horizontal Colors: 8 Color
			101 = Horizontal Colors: 8 Gray Scale
			110 = Horizontal Colors: 3 Color
			111 = Horizontal Colors: Stripes
Enhanced Frame, ASSR, and Vstream Enable	0x5A		0X0D

4.3 ASSR Example Code

The following is example code for the "Aardvark I2C/SPI Host Adapter" following the sequence of register programming from the previous section. This code should be modified to apply the desired system that the DSI86 is implemented in.

```
<aardvark>
<configure i2c="1" spi="1" gpio="0" tpower="1" pullups="0"/>
 <i2c_bitrate khz="100"/>
======REFCLK Frequency ======
<i2c_write addr="0x2D" count="1" radix="16"> 0A 2 </i2c_write>/>
======DSI Mode ======
<i2c_write addr="0x2D" count="1" radix="16"> 10 20 </i2c_write>/>
======DSIA Clock ======
<i2c_write addr="0x2D" count="1" radix="16"> 12 2E </i2c_write>/>
======DSIB Clock ======
<i2c_write addr="0x2D" count="1" radix="16"> 13 2E </i2c_write>/>
======DP Datarate ======
<i2c_write addr="0x2D" count="1" radix="16"> 94 E0 </i2c_write>/>
 ======Enable PLL ======
<i2c_write addr="0x2D" count="1" radix="16"> 0D 1 </i2c_write> <sleep ms="10"/>
======Enable ASSR in Panel ======
<i2c_write addr="0x2D" count="1" radix="16"> 64 1 </i2c_write>/>
<i2c_write addr="0x2D" count="5" radix="16"> 74 0 1 0A 1 81 </i2c_write> <sleep ms="10"/>
 ======Enable enhanced frame and ASSR in DSI86 ======
<i2c_write addr="0x2D" count="1" radix="16"> 5A 5 </i2c_write>/>
======Number of DP lanes ======
<i2c_write addr="0x2D" count="1" radix="16"> 93 10 </i2c_write>/>
======Start Semi-Auto Link Training ======
<i2c_write addr="0x2D" count="1" radix="16"> 96 0A </i2c_write> <sleep ms="20"/>
======CHA Active Line Length ======
<i2c_write addr="0x2D" count="2" radix="16"> 20 70 08 </i2c_write>/>
======CHB Active Line Length ======
<i2c_write addr="0x2D" count="2" radix="16"> 22 0 0 </i2c_write>/>
======Vertical Active Size ======
<i2c_write addr="0x2D" count="2" radix="16"> 24 A0 05 </i2c_write>/>
======Horizontal Pulse Width ======
<i2c_write addr="0x2D" count="2" radix="16"> 2C 20 00 </i2c_write>/>
 ======Vertical Pulse Width ======
<i2c_write addr="0x2D" count="2" radix="16"> 30 0A 00 </i2c_write>/>
======HBP ======
<i2c_write addr="0x2D" count="1" radix="16"> 34 50 </i2c_write>/>
======VBP ======
<i2c_write addr="0x2D" count="1" radix="16"> 36 1B </i2c_write>/>
===== HFP ======
<i2c_write addr="0x2D" count="1" radix="16"> 38 30 </i2c_write>/>
===== VFP ======
<i2c_write addr="0x2D" count="1" radix="16"> 3A 03 </i2c_write>/>
===== DP-18BPP Disable ======
<i2c_write addr="0x2D" count="1" radix="16"> 5B 0 </i2c_write>/>
===== Color Bar Enable ======
<i2c_write addr="0x2D" count="1" radix="16"> 3C 07 </i2c_write>/>
===== Enhanced Frame, ASSR, and Vstream Enable ======
<i2c_write addr="0x2D" count="1" radix="16"> 5A 0D </i2c_write>/>
</aardvark>
```

4.4 Non-ASSR

Table 6 is a sequence with register values to program the DSI86. This table should be followed if the panel does not support ASSR.

Table 6. Non-ASSR Registers

Register Purpose	Register Address	Bit Number	Register Value

Reference Clock Frequency	0x0A	3	DPPLL_CLK_SRC = 0 (Ref clock used)
			DPPLL_CLK_SRC = 1 (No Ref clock)

		1:2	000=12 MHz 000 = Continuous DSIA CLK at 468 MHz
			001 = 19.2 MHz (Default) 001 = Continuous DSIA CLK at 384 MHz
			010 = 26 MHz 010 = Continuous DSIA CLK at 416 MHz
			011 = 27 MHz 011 = Continuous DSIA CLK at 486 MHz
			100 = 38.4 MHz 100 = Continuous DSIA CLK at 460.8 MHz
DSI Mode	0x10	7	LEFT_RIGHT_PIXELS:
			0 = DSI channel A receives ODD pixels and channel B receives EVEN (default)
			1 = DSI channel A receives LEFT image pixels and channel B receives RIGHT image pixels
		6:5	DSI_CHANNEL_MODE:
			00 = Dual-channel DSI receiver
			01 = Single channel DSI receiver A (default)
		4:3	CHA_DSI_LANES: Note: Unused DSI inputs pins on the DSI86 should be left unconnected.
			This field controls the number of lanes that are enabled for DSI Channel A.
			00 = Four lanes are enabled
			01 = Three lanes are enabled
			10 = Two lanes are enabled
			11 = One lane is enabled (default)
		2:1	CHB_DSI_LANES:
			This field controls the number of lanes that are enabled for DSI Channel B.
			00 = Four lanes are enabled
			01 = Three lanes are enabled
			10 = Two lanes are enabled
			11 = One lane is enabled (default)
DSI A Clock	0x12	7:0	CHA_DSI_CLK_RANGE This field specifies the DSI clock frequency range in 5-MHz increments for DSI Channel A clock. The DSI86 estimates the DSI clock frequency using the REFCLK frequency determined at the rising edge of EN and updates this field accordingly. Software can override this value. If the CHA_DSI_CLK_RANGE is not loaded before receiving the first DSI packet, the DSI86 uses the first packet to estimate the DSI_CLK frequency and loads this field with this estimate. This first packet may not be received; thus, the host should send a first dummy packet (such as DSI read or write to register 0x00). This field may be written by the host at any time. Any non-zero value written by the host is used instead of the automatically estimated value. 0x00 through 0x07: Reserved 0x08 = 40 ≤ frequency < 45 MHz 0x09 = 45 ≤ frequency < 50 MHz . . . 0x96 = 750 ≤ frequency < 755 MHz 0x97 through 0xFF: Reserved

Table 6. Non-ASSR Registers (continued)

Register Purpose	Register Address	Bit Number	Register Value
DSI B Clock	0x13	7:0	CHB_DSI_CLK_RANGE This field specifies the DSI clock frequency range in 5-MHz increments for DSI Channel B clock. The DSI86 estimates the DSI clock frequency using the REFCLK frequency determined at the rising edge of EN and updates this field accordingly. Software can override this value. If the CHB_DSI_CLK_RANGE is not loaded before receiving the first DSI packet, the DSI86 uses the first packet to estimate the DSI_CLK frequency and loads this field with this estimate. This first packet may not be received; thus, the host should send a first dummy packet (such as DSI read or write to register 0x00). This field may be written by the host at any time. Any non-zero value written by the host is used instead of the automatically estimated value. 0x00 through 0x07: Reserved 0x08 = 40 ≤ frequency < 45 MHz 0x09 = 45 ≤ frequency < 50 MHz . . . 0x96 = 750 ≤ frequency < 755 MHz 0x97 through 0xFF: Reserved
DP Datarate	0x94	7:5	DP_DATARATE
			000 = Not Configured (Default)
			001 = 1.62 Gbps per lane (RBR)
			010 = 2.16 Gbps per lane
			011 = 2.43 Gbps per lane
			100 = 2.70 Gbps per lane (HBR)
			101 = 3.24 Gbps per lane
			110 = 4.32 Gbps per lane.
			111 = 5.4 Gbps per lane (HBR2)
Enable PLL	0x0D	0	DP_PLL_EN
			0 = PLL disabled (default)
			1 = PLL enabled
Enable enhanced frame and ASSR	0x5A		0x4
Number of DP Lanes	0x93	5:4	DP_NUM_LANES.
			00 = Not Configured. (Default)
			01 = 1 DP lane.
			10 = 2 DP lanes.
			11 = 4 DP lanes.
Start Semi-Auto Link Training	0x96	3:0	0x0A

Table 6. Non-ASSR Registers (continued)

Register Purpose	Register Address	Bit Number	Register Value
CHA Active Line Length	0x20	7:0	CHA_ACTIVE_LINE_LENGTH_LOW: When the DSI86 is configured for a single DSI input, this field controls the length in pixels of the active horizontal line for Channel A. When configured for Dual DSI Inputs in Odd/Even mode, this field controls the number of odd pixels in the active horizontal line that are received on DSI channel A. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of left pixels in the active horizontal line that are received on DSI channel A. The value in this field is the lower 8 bits of the 12-bit value for the horizontal line length. This field defaults to 0x00. Note: When the DSI86 is configured for dual DSI inputs in Left/Right mode and LEFT_CROP field is programmed to a value other than 0x00, the CHA_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Left portion of the line after LEFT_CROP has been applied.
	0x21	3:0	CHA_ACTIVE_LINE_LENGTH_HIGH: When the DSI86 is configured for a single DSI input, this field controls the length in pixels of the active horizontal line for Channel A. When configured for Dual DSI Inputs in Odd/Even mode, this field controls the number of odd pixels in the active horizontal line that are received on DSI channel A. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of left pixels in the active horizontal line that are received on DSI channel A. The value in this field is the upper 4 bits of the 12-bit value for the horizontal line length. This field defaults to 0x00. Note: When the DSI86 is configured for dual DSI inputs in Left/Right mode and LEFT_CROP field is programmed to a value other than 0x00, the CHA_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Left portion of the line after LEFT_CROP has been applied.
CHB Active Line Length	0x22	7:0	CHB_ACTIVE_LINE_LENGTH_HIGH: When configured for Dual DSI Inputs in Odd/Even mode, this field controls the number of even pixels in the active horizontal line that are received on DSI channel B. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of right pixels in the active horizontal line that are received on DSI channel B. The value in this field is the upper 4 bits of the 12-bit value for the horizontal line length. This field defaults to 0x00. Note: When the DSI86 is configured for dual DSI inputs in Left/Right mode and RIGHT_CROP field is programmed to a value other than 0x00, the CHB_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Right portion of the line after RIGHT_CROP has been applied.
	0x23	3:0	CHA_VERTICAL_DISPLAY_SIZE_LOW: This field controls the vertical display size in lines for Channel A. The value in this field is the lower 8 bits of the 12-bit value for the vertical display size. This field defaults to 0x00.
Vertical Active Size	0x24	7:0	CHA_VERTICAL_DISPLAY_SIZE_LOW: This field controls the vertical display size in lines for Channel A. The value in this field is the lower 8 bits of the 12-bit value for the vertical display size. This field defaults to 0x00.
	0x25	3:0	CHA_VERTICAL_DISPLAY_SIZE_HIGH: This field controls the vertical display size in lines for Channel A. The value in this field is the upper 4 bits of the 12-bit value for the vertical display size. This field defaults to 0x00.

Table 6. Non-ASSR Registers (continued)

Register Purpose	Register Address	Bit Number	Register Value
Horizontal Pulse Width	0x2C	7:0	CHA_HSYNC_PULSE_WIDTH_LOW: This field controls the width in pixel clocks of the HSync Pulse Width for Channel A. The value in this field is the lower 8 bits of the 15-bit value for HSync Pulse width. This field defaults to 0x00.
	0x2D	7	CHA_HSYNC_POLARITY
			0 = Active High Pulse. Synchronization signal is high for the sync pulse width. (default)
			1 = Active Low Pulse. Synchronization signal is low for the sync pulse width.
		6:0	CHA_HSYNC_PULSE_WIDTH_HIGH
			This field controls the width in pixel clocks of the HSync Pulse Width for Channel A. The value in this field is the upper 7 bits of the 15-bit value for HSync Pulse width. This field defaults to 0x00.
Vertical Pulse Width	0x30	7:0	CHA_VSYNC_PULSE_WIDTH_LOW: This field controls the length in lines of the VSync Pulse Width for Channel A. The value in this field is the lower 8 bits of the 15-bit value for VSync Pulse width. This field defaults to 0x00. The total size of the VSYNC pulse width must be at least 1 line.
	0x31	7	CHA_VSYNC_POLARITY:
			0 = Active High Pulse. Synchronization signal is high for the sync pulse width. (Default)
			1 = Active Low Pulse. Synchronization signal is low for the sync pulse width.
		6:0	CHA_VSYNC_PULSE_WIDTH_HIGH: This field controls the width in lines of the VSync Pulse Width for Channel A. The value in this field is the upper 7 bits of the 15-bit value for VSync Pulse width. This field defaults to 0x00. The total size of the VSYNC pulse width must be at least 1 line.
Horizontal Back Porch (HBP)	0x34	7:0	CHA_HORIZONTAL_BACK_PORCH: This field controls the time in pixel clocks between the end of the HSync Pulse and the start of the active video data for Channel A. This field defaults to 0x00.
Vertical Back Porch (VBP)	0x36	7:0	CHA_VERTICAL_BACK_PORCH: This field controls the number of lines between the end of the VSync Pulse and the start of the active video data for Channel A. This field defaults to 0x00. The total size of the Vertical Back Porch must be at least 1 line.
Horizontal Front Porch (HFP)	0x38	7:0	CHA_HORIZONTAL_FRONT_PORCH: This field controls the time in pixel clocks between the end of the active video data and the start of the HSync Pulse for Channel A. This field defaults to 0x00.
Vertical Front Porch (VFP)	0x3A	7:0	CHA_VERTICAL_FRONT_PORCH: This field controls the number of lines between the end of the active video data and the start of the VSync Pulse for Channel A. This field defaults to 0x00. The total size of the Vertical Front Porch must be at least 1 line.
Bit Per Pixel	0x5B	1	ENCH_FRAME_PATT
			0 = SR BF BF SR or BS BF BF BS (Default)
			1 = SR CP CP SR or BS CP CP BS
		0	DP_18BPP_EN: If this field is set, then 18BPP format will be transmitted over eDP interface regardless of the DSI pixel stream data type format.
			0 = 24BPP RGB. (default)
			1 = 18BPP RGB

Table 6. Non-ASSR Registers (continued)

Register Purpose	Register Address	Bit Number	Register Value
Color Bar	0x3C	4	COLOR_BAR_EN: When this bit is set, the DSI86 generates a video test pattern on DisplayPort based on the values programmed into the Video Registers for Channel A.
			0 = Transmit of SMPTE color bar disabled. (default)
			1 = Transmit of SMPTE color bar enabled.
		2:0	COLOR_BAR_PATTERN:
			000 = Vertical Colors: 8 Color (Default)
			001 = Vertical Colors: 8 Gray Scale
			010 = Vertical Colors: 3 Color
			011 = Vertical Colors: Stripes
			100 = Horizontal Colors: 8 Color
			101 = Horizontal Colors: 8 Gray Scale
			110 = Horizontal Colors: 3 Color
			111 = Horizontal Colors: Stripes
Enhanced Frame and Vstream Enable	0x5A		0x0C

4.5 Non-ASSR Example Code

The following is example code for the "Aardvark I2C/SPI Host Adapter" following the sequence of register programming from the previous section. This code should be modified to apply the desired system in which the DSI86 is implemented.

```
<aardvark>
<configure i2c="1" spi="1" gpio="0" tpower="1" pullups="0"/>
<i2c_bitrate khz="100"/>
 ======ASSR RW control ======
<i2c_write addr="0x2D" count="1" radix="16"> FF 7 </i2c_write>/>
<i2c_write addr="0x2D" count="1" radix="16"> 16 1 </i2c_write>/>
<i2c_write addr="0x2D" count="1" radix="16"> FF 0 </i2c_write>/>
======REFCLK Frequency ======
<i2c_write addr="0x2D" count="1" radix="16"> 0A 2 </i2c_write>/>
=====DSI Mode ======
<i2c_write addr="0x2D" count="1" radix="16"> 10 20 </i2c_write>/>
======DSIA Clock ======
<i2c_write addr="0x2D" count="1" radix="16"> 12 2E </i2c_write>/>
======DSIB Clock ======
<i2c_write addr="0x2D" count="1" radix="16"> 13 2E </i2c_write>/>
======DP Datarate ======
<i2c_write addr="0x2D" count="1" radix="16"> 94 E0 </i2c_write>/>
======Enable PLL ======
<i2c_write addr="0x2D" count="1" radix="16"> 0D 1 </i2c_write> <sleep ms="10"/>
======Enable enhanced frame in DSI86 ======
<i2c_write addr="0x2D" count="1" radix="16"> 5A 4 </i2c_write>/>
======Number of DP lanes ======
<i2c_write addr="0x2D" count="1" radix="16"> 93 10 </i2c_write>/>
======Start Semi-Auto Link Training ======
<i2c_write addr="0x2D" count="1" radix="16"> 96 0A </i2c_write> <sleep ms="20"/>
======CHA Active Line Length ======
<i2c_write addr="0x2D" count="2" radix="16"> 20 70 08 </i2c_write>/>
======CHB Active Line Length ======
<i2c_write addr="0x2D" count="2" radix="16"> 22 0 0 </i2c_write>/>
======Vertical Active Size ======
<i2c_write addr="0x2D" count="2" radix="16"> 24 A0 05 </i2c_write>/>
======Horizontal Pulse Width ======
<i2c_write addr="0x2D" count="2" radix="16"> 2C 20 00 </i2c_write>/>
======Vertical Pulse Width ======
<i2c_write addr="0x2D" count="2" radix="16"> 30 0A 00 </i2c_write>/>
======HBP ======
<i2c_write addr="0x2D" count="1" radix="16"> 34 50 </i2c_write>/>
======VBP ======
<i2c_write addr="0x2D" count="1" radix="16"> 36 1B </i2c_write>/>
===== HFP ======
<i2c_write addr="0x2D" count="1" radix="16"> 38 30 </i2c_write>/>
===== VFP ======
<i2c_write addr="0x2D" count="1" radix="16"> 3A 03 </i2c_write>/>
===== DP-18BPP Disable ======
<i2c_write addr="0x2D" count="1" radix="16"> 5B 0 </i2c_write>/>
===== Color Bar Enable ======
<i2c_write addr="0x2D" count="1" radix="16"> 3C 07 </i2c_write>/>
===== Enhanced Frame, and Vstream Enable ======
<i2c_write addr="0x2D" count="1" radix="16"> 5A 0C </i2c_write>/>
</aardvark>
```

5 Example

The following will be an example system using the DSI86 and walk through the calculations for the register programming of the DSI86.

5.1 System Parameters

Table 7. System Parameters

System Parameter	Example Value
Clock Source (REFCLK or DSIA_CLK)	REFCLK
REFCLK Frequency (12 MHz, 19.2 MHz, 26 MHz, 27 MHz, or 38.4 MHz)	27 MHz
Pixel Clock (MHz)	148.5
Horizontal Active (pixels)	1920
Horizontal Blanking (pixels)	280
Vertical Active (lines)	1080
Vertical Blanking (lines)	45
Horizontal Sync Offset or FrontPorch (pixels)	88
Horizontal Sync Pulse Width (pixels)	44
Vertical Sync Offset or FrontPorch(lines)	4
Vertical Sync Pulse Width (lines)	5
Horizontal Sync Pulse Polarity	Positive
Vertical Sync Pulse Polarity	Positive
Color Bit Depth (6 bpc or 8 bpc)	8 (24 bpp)
eDP Version (1.0, 1.1, 1.2, 1.3, or 1.4)	1.3
Number of eDP lanes (1, 2, or 4)	2
Datarate Supported (1.62 Gbps, 2.16 Gbps, 2.43 Gbps, 2.70 Gbps, 3.24 Gbps, 4.32 Gbps, or 5.40 Gbps)	2.70
APU or GPU Maximum number of DSI Lanes (1 through 8)	4
APU or GPU Maximum DSI Clock Frequency (MHz)	500
Single or Dual DSI	Single
Dual DSI Configuration (Odd/Even or Left/Right)	NA

5.2 Calculations

The panel, as indicated by the panel EDID information, supports a pixel clock of 148.5 MHz at 8 bpc or 24 bpp. This translates to a stream bit rate of 3.564 Gbps.

$$\begin{aligned} Stream\ \ Bit\ \ Rate &= PixelClock \times bpp \\ Stream\ \ Bit\ \ Rate &= 148.5 \times 24 \\ Stream\ \ Bit\ \ Rate &= 3.564\ \ Gbps \end{aligned} \quad (6)$$

In order to support the panel stream bit rate, the DSI86 eDP interface must be programmed so that the total eDP data rate is greater than the stream bit rate. In this example, the total eDP data rate is calculated as:

$$\begin{aligned} eDPTotalBitRate &= \#\_of\_eDP\_Lanes \times DataRate \times 0.80 \\ eDP\ \ Total\ \ Bit\ \ Rate &= 2 \times 2.7\ \ Gbps \times 0.80 \\ eDP\ \ Total\ \ Bit\ \ Rate &= 4.32\ \ Gbps \end{aligned} \quad (7)$$

In this example, the eDP panel DPCD registers indicates eDP1.3 compliant, supports a data rate of 2.7 Gbps per lane, and a lane count of 2. For this panel to operate properly, the DSI86 would need to be programmed to enable two lanes at a data rate of 2.7 Gbps each. In portable and mobile applications, total power consumption is a key care-about. In this example, the panel chosen is eDP 1.3 compliant and supports a data rate of 2.7 Gbps per lane. The DSI86 power consumption is a function of the data rate and number of active DP lanes. By reducing the number of active lanes and/or data rate, the total power consumption of the DSI86 is reduced as well. If a panel which supported data rate of 5.4 Gbps was chosen over the example panel, the number of lanes could be reduced from two lanes to one lane. Or if a panel which was eDP1.4 compliant and support 2.43 Gbps data rate was chosen over the example panel, the data rate could be reduced from 2.7 Gbps to 2.43 Gbps. Once the eDP interface parameters are known, the video resolution parameters required by the panel need to be programmed into the DSI86. For this example, the parameters programmed would be the following:

Table 8. Video Resolution Parameters

Parameter	Abbreviation	Equation/Source	Value
Horizontal Sync Polarity	HPOL	EDID	Positive
Horizontal Sync Pulse Width	HPW	EDID	44
Horizontal Back Porch	HBP	=HBL-HPW-HFP	148 = 280 - 44 - 88
Horizontal Active Line	HACT	EDID	1920
Horizontal Front Porch	HFP	EDID	88
Horizontal Blanking	HBL	EDID	280
Horizontal Total	HTOTAL	=HPW + HBP + HACT +HFP	2200 = 44 + 148 + 1920 + 88
Vertical Sync Polarity	VPOL	EDID	Positive
Vertical Sync Pulse Width	VPW	EDID	5
Vertical Back Porch	VBP	=VBL - VPW - VFP	36 = 45 - 5 - 4
Vertical Active Line	VACT	EDID	1080
Vertical Front Porch	VFP	EDID	4
Vertical Blanking	VBL	EDID	45
Vertical Active Line	VTOTAL	=VPW + VBP + VACT + VFP	1125 = 5 + 36 + 1080 + 4

The APU or GPU must provide a stream bit rate as required by the eDP panel. In this particular example, the eDP panel stream rate is 3.564 Gbps. Because the DSI86 can support a DSI clock rate of up to 750 MHz (or 1.5 Gbps), the minimum number of required DSI lanes to meet the stream bit rate is three lanes. But in this example, the APU/GPU maximum DSI Clock frequency is 500 MHz. This means the number of required DSI lanes will need to be increased to four lanes

$$\begin{aligned} Min\ \ number\ \ of\ \ DSI\ \ Lanes &= StreamBitRate\ / \ MaxDSIClock \\ Min\ \ number\ \ of\ \ DSI\ \ Lanes &= 3564\ \ MBps\ /\ (500 \times 2) \\ Min\ \ number\ \ of\ \ DSI\ \ Lanes &= 3.564\ \ lanes \\ Min\ \ number\ \ of\ \ DSI\ \ Lanes &= 4\ \ lanes \end{aligned} \quad (8)$$

After determining the number of required DSI lanes, the next step is to determine the minimum required DSI clock frequency to support the stream bit rate of the eDP panel. For 24 bpp, the calculation for determining the DSI clock frequency is as follows:

$$\begin{aligned} MinRequiredDSIClockFrequency &= StreamBitRate\ /\ (Min\_Number - DSI\_Lanes \times 2) \\ Min\ \ Required\ \ DSI\ \ Clock\ \ Frequency &= 3564\ /\ (4 \times 2) \\ Min\ \ Required\ \ DSI\ \ Clock\ \ Frequency &= 445.5\ \ MHz \end{aligned} \tag{9}$$

In this example, the clock source for the DSI86 is the REFCLK pin. When using the REFCLK as the clock source, any DSI Clock frequency is supported. But if the clock source was instead the DSI A clock, then the required DSI Clock frequency would need to change to a frequency supported by the DSI86. When operating in this mode, any one of the following DSI A clock frequencies can be used: 384 MHz, 416 MHz, 460.8 MHz, 468 MHz, or 486 MHz. In most cases, a eDP panel would support some variation from the ideal pixel clock frequency. For this example either 416 MHz or 460.8 MHz could be tried.

5.3 Script

asds

```
<aardvark>
<configure i2c="1" spi="1" gpio="0" tpower="1" pullups="0" />
<i2c_bitrate khz="100" />
======REFCLK 27MHz ======
<i2c_write addr="0x2D" count="1" radix="16">0A 06</i2c_write> />
======Single 4 DSI lanes======
<i2c_write addr="0x2D" count="1" radix="16">10 26</i2c_write> />
======DSIA CLK FREQ 445MHz======
<i2c_write addr="0x2D" count="1" radix="16">12 59</i2c_write> />
======enhanced framing and ASSR======
<i2c_write addr="0x2D" count="1" radix="16">5A 05</i2c_write> />
======2 DP lanes no SSC======
<i2c_write addr="0x2D" count="1" radix="16">93 20</i2c_write> />
======HBR (2.7Gbps)======
<i2c_write addr="0x2D" count="1" radix="16">94 80</i2c_write> />
======PLL ENABLE======
<i2c_write addr="0x2D" count="1" radix="16">0D 01</i2c_write> <sleep ms="10" />
======Verify PLL is locked======
<i2c_write addr="0x2D" count="0" radix="16">0A</i2c_write> />
<i2c_read addr="0x2D" count="2" radix="16">00</i2c_read> <sleep ms="10" />
======POST-Cursor2 0dB ======
<i2c_write addr="0x2D" count="1" radix="16">95 00</i2c_write> />
======Write DPCD Register 0x0010A in Sink to Enable ASSR======
<i2c_write addr="0x2D" count="1" radix="16">64 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">74 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">75 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">76 0A</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">77 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">78 81</i2c_write> <sleep ms="10" />
======Semi-Auto TRAIN ======
<i2c_write addr="0x2D" count="1" radix="16">96 0A</i2c_write> <sleep ms="20" />
======Verify Training was successful======
<i2c_write addr="0x2D" count="0" radix="16">96</i2c_write> />
<i2c_read addr="0x2D" count="1" radix="16">00</i2c_read> <sleep ms="10" />
=====CHA_ACTIVE_LINE_LENGTH is 1920 =======
<i2c_write addr="0x2D" count="2" radix="16">20 80 07</i2c_write> />
=====CHA_VERTICAL_DISPLAY_SIZE is 1080 =======
<i2c_write addr="0x2D" count="2" radix="16">24 38 04</i2c_write> />
=====CHA_HSYNC_PULSE_WIDTH is 44 positive =======
<i2c_write addr="0x2D" count="2" radix="16">2C 2C 00</i2c_write> />
=====CHA_VSYNC_PULSE_WIDTH is 5 positive=======
<i2c_write addr="0x2D" count="2" radix="16">30 05 80</i2c_write> />
=====CHA_HORIZONTAL_BACK_PORCH is 148=======
<i2c_write addr="0x2D" count="1" radix="16">34 94</i2c_write> />
=====CHA_VERTICAL_BACK_PORCH is 36=======
<i2c_write addr="0x2D" count="1" radix="16">36 24</i2c_write> />
=====CHA_HORIZONTAL_FRONT_PORCH is 88=======
<i2c_write addr="0x2D" count="1" radix="16">38 58</i2c_write> />
=====CHA_VERTICAL_FRONT_PORCH is 4=======
<i2c_write addr="0x2D" count="1" radix="16">3A 04</i2c_write> />
======DP- 24bpp======
<i2c_write addr="0x2D" count="1" radix="16">5B 00</i2c_write> />
=====COLOR BAR disabled=======
<i2c_write addr="0x2D" count="1" radix="16">3C 00</i2c_write> />
======enhanced framing, ASSR, and Vstream enable======
<i2c_write addr="0x2D" count="1" radix="16">5A 0D</i2c_write> />
</aardvark>0
```

6 Color Bar

The Color Bar is a series of preset patterns that The DSI86 can output without a Source. The active video size of the Color bar is determined by the values programmed into the Video Registers. The Color Bar can be a powerful tool in debugging the issues that can arise when programming the DSI86s registers.

6.1 Color Bar Register Values

The 0x3C is the Color bar register. Table 9 is the values that can be programmed into the DSI86 register 0x3C to produce the color bar.

Table 9. Color Bar Register

Pattern Generated	Binary Value	Hex Value
Color Bar Disabled	00000	0x00
Vertical Colors: 8 Color	10000	0x10
Vertical Colors: 8 Gray Scale	10001	0x11
Vertical Colors: 3 Color	10010	0x12
Vertical Colors: Stripes	10011	0x13
Horizontal Colors: 8 Color	10100	0x14
Horizontal Colors: 8 Gray Scale	10101	0x15
Horizontal Colors: 3 Color	10110	0x16
Horizontal Colors: Stripes	10111	0x17

7 Troubleshooting

To troubleshoot the DSI86 it is best to first narrow down what side of the DSI86 is the issue occurring. The best way to test if an error is originating from the eDP side of the DSI86 is to use the color bar generator because this output does not rely on the DSI side of the DSI86. See Section 6 on how to use the Color Bar

7.1 Error Registers

The DSI86 has a list of errors registers to aid in debugging errors that occur when programming and using the DSI86. These error registers are register 0xF0 to 0xF8. The different error register bits meanings are posted in Table 10.

Table 10. Error Registers

0xF0	7	CHA_CONTENTION_DET_ERR. When LP high or LP low fault is detected on the DSI channel A interface, this bit is set; this bit is cleared by writing a 1 or when the SN65DSI86 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.
	6	CHA_FALSE_CTRL_ERR. When the DSI channel A packet processor detects a LP Request not followed by the remainder of a valid escape or turnaround sequence or if it detects a HS request not followed by a bridge state (LP-00), this bit is set; this bit is cleared by writing a 1 or when the SN65DSI86 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.
	5	CHA_TIMEOUT_ERR. When the HS Rx Timer or the LP TX timer expires, this bit is set; this bit is cleared by writing a 1 or when the DSN65DSI86 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.
	4	CHA_LP_TX_SYNC_ERR. When the DSI channel A packet processor detects data not synchronized to a byte boundary at the end of Low-Power transmission, this bit is set; this bit is cleared by writing a 1 or when the SN65DSI86 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.
	3	CHA_ESC_ENTRY_ERR. When the DSI Channel A packet processor detects an unrecognized Escape Mode Entry Command, this bit is set; this bit is cleared by writing a 1 or when the SN65DSI86 responds to a Generic read request or unsolicited BTA with a Acknowledge and Error Report.
	2	CHA_EOT_SYNC_ERR. When the DSI channel A packet processor detects that the last byte of a HS transmission does not match a byte boundary, this bit is set; this bit is cleared by writing a 1 or when the SN65DSI86 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report
	1	CHA_SOT_SYNC_ERR. When the DSI channel A packet processor detects a corrupted SOT in a way that proper synchronization cannot be expected, this bit is set; this bit is cleared by writing a 1 or when the SN65DSI86 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report
	0	CHA_SOT_BIT_ERR When the DSI channel A packet processor detects an SoT leader sequence bit error, this bit is set; this bit is cleared by writing a 1 or when the SN65DSI86 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.
0xF1	7	CHA_DSI_PROTOCOL_ERR. When the DSI channel A packet processor detects a DSI protocol error, this bit is set; this bit is cleared by writing a 1 or when the SN65DSI86 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.
	6	Reserved.
	5	CHA_INVALID_LENGTH_ERR. When the DSI channel A packet processor detects an invalid transmission length, this bit is set; this bit is cleared by writing a 1 or when the SN65DSI86 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.
	4	Reserved.
	3	CHA_DATATYPE_ERR. When the DSI channel A packet processor detects a unrecognized DSI data type, this bit is set; this bit is cleared by writing a 1 or when the SN65DSI86 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.
	2	CHA_CHECKSUM_ERR When the DSI channel A packet processor detects a data stream CRC error, this bit is set; this bit is cleared by writing a 1 or when the SN65DSI86 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.
	1	CHA_UNC_ECC_ERR When the DSI channel A packet processor detects an uncorrectable ECC error, this bit is set; this bit is cleared by writing a 1 or when the SN65DSI86 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.
	0	CHA_COR_ECC_ERR When the DSI channel A packet processor detects a correctable ECC error, this bit is set; this bit is cleared by writing a 1 or when the SN65DSI86 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.

Table 10. Error Registers (continued)

0xF2	7	Reserved
	6	CHB_FALSE_CTRL_ERR. When the DSI channel B packet processor detects a LP Request not followed by the remainder of a valid escape or turnaround sequence or if it detects a HS request not followed by a bridge state (LP-00), this bit is set; this bit is cleared by writing a 1.
	5	Reserved
	4	CHB_LP_TX_SYNC_ERR. When the DSI channel B packet processor detects data not synchronized to a byte boundary at the end of Low-Power transmission, this bit is set; this bit is cleared by writing a 1.
	3	Reserved
	2	CHB_EOT_SYNC_ERR. When the DSI channel B packet processor detects that the last byte of a HS transmission does not match a byte boundary, this bit is set; this bit is cleared by writing a 1.
	1	CHB_SOT_SYNC_ERR. When the DSI channel B packet processor detects a corrupted SOT in a way that proper synchronization cannot be expected, this bit is set; this bit is cleared by writing a 1.
	0	CHB_SOT_BIT_ERR When the DSI channel B packet processor detects an SoT leader sequence bit error, this bit is set; this bit is cleared by writing a 1.
0xF3	7	CHB_DSI_PROTOCOL_ERR. When the DSI channel B packet processor detects a DSI protocol error, this bit is set; this bit is cleared by writing a 1.
	6	Reserved.
	5	CHB_INVALID_LENGTH_ERR. When the DSI channel B packet processor detects an invalid transmission length, this bit is set; this bit is cleared by writing a 1.
	4	Reserved.
	3	CHB_DATATYPE_ERR. When the DSI channel B packet processor detects a unrecognized DSI data type, this bit is set; this bit is cleared by writing a 1.
	2	CHB_CHECKSUM_ERR When the DSI channel B packet processor detects a data stream CRC error, this bit is set; this bit is cleared by writing a 1.
	1	CHB_UNC_ECC_ERR When the DSI channel B packet processor detects an uncorrectable ECC error, this bit is set; this bit is cleared by writing a 1.
	0	CHB_COR_ECC_ERR When the DSI channel B packet processor detects a correctable ECC error, this bit is set; this bit is cleared by writing a 1.
0xF4	7	I2C_DEFR. This field is set if an I2C-Over-Aux request has received a specific number X of I2C_DEFER from Sink. For direct method (clock stretching), the number X is 44. For indirect method, the number X is: 44 for AUX_LENGTH = 1 66 for AUX_LENGTH = 2 110 for 2 < AUX_LENGTH ≤ 4 154 for 4 < AUX_LENGTH ≤ 6 198 for 6< AUX_LENGTH ≤ 8 287 for 8< AUX_LENGTH ≤ 12 375 for 12 < AUX_LENGTH ≤ 16
	6	NAT_I2C_FAIL. This bit is set if the I2C-Over-Aux or Native AUX failed.
	5	AUX_SHORT. If set, then the bytes written or received did not match requested Length. SW should read AUX_LENGTH field to determine the amount of data written or read.
	4	AUX_DEFR. The SN65DSI86 will attempt to complete an AUX request by retrying the request seven times. This field is set if the response to the last retry is an AUX_DEFER.
	3	AUX_RPLY_TOUT. The SN65DSI86 will attempt to complete an AUX request by retrying the request seven times. This field is set if the response to the last retry is a 400-µs timeout.
	2	Reserved.
	1	Reserved.
	0	SEND_INT. This field is set whenever the SEND bit transitions from 1 to 0.

Table 10. Error Registers (continued)

0xF5	7	Reserved
	6	Reserved
	5	PLL_UNLOCK This bit is set whenever the PLL Lock status transitions from LOCK to UNLOCK.
	4	Reserved
	3	HPD_REPLUG. This field is set whenever the SN65DSI86 detects a replug event on the HPD pin.
	2	HPD_REMOVAL. This field is set whenever the SN65DSI86 detects a DisplayPort device removal.
	1	HPD_INSERTION. This field is set whenever the SN65DSI86 detects a DisplayPort device insertion.
	0	IRQ_HPD. This field is set whenever the SN65DSI86 detects a IRQ_HPD event.
0xF6	7	VIDEO_WIDTH_PROG_ERR. This field is set whenever the video parameters define more bytes of pixel data than can be transferred in the allotted video portion of the line time.
	6	LOSS_OF_DP_SYNC_LOCK_ERR. This field is set whenever the DP sync generator has lost lock with the DSI sync stream.
	5	DPTL_UNEXPECTED_DATA_ERR. This field is set whenever a data token at in the video stream from DSI was found at an invalid time syntactically.
	4	DPTL_UNEXPECTED_SECDATA_ERR. This field is set whenever a secondary data start token at in the video stream was found at an invalid time syntactically.
	3	DPTL_UNEXPECTED_DATA_END_ERR. This field is set whenever a data end token at in the video stream from DSI was found at an invalid time syntactically.
	2	DPTL_UNEXPECTED_PIXEL_DATA_ERR. This field is set whenever a video data start token at in the video stream from DSI was found at an invalid time syntactically.
	1	DPTL_UNEXPECTED_HSYNC_ERR. This field is set whenever a horizontal sync token at in the video stream from DSI was found at an invalid time syntactically.
	0	DPTL_UNEXPECTED_VSYNC_ERR. This field is set whenever a vertical sync token at in the video stream from DSI was found at an invalid time syntactically.
0xF7	7	Reserved
	1	DPTL_SECONDARY_DATA_PACKET_PROG_ERR. This field is set whenever a secondary data packet has an invalid length.
	0	DPTL_DATA_UNDERRUN_ERR. This field is set whenever no data was received when data should have been ready.
0xF8	7:6	Reserved.
	5	LT_EQ_CR_ERR. This field is set whenever link training fails in the channel equalization phase due to LANEx_CR_DONE not set.
	4	LT_EQ_LPCNT_ERR. This field is set whenever link training fails in the channel equalization phase due to the loop count being greater than five.
	3	LT_CR_MAXVOD_ERR. This field is set whenever link training fails in clock recovery phase due to maximum VOD reached without LANEx_CR_DONE bit(s) getting set
	2	LT_CR_LPCNT_ERR. This field is set whenever link training fails in the clock recovery phase due to same VOD being used five times.
	1	LT_FAIL. This field is set whenever the Semi-Auto link training fails to train the DisplayPort Link.
	0	LT_PASS. This field is set whenever the Semi-Auto link training successfully trains the DisplayPort Link.

8 References

- SN65DSI86 Datasheet (SLLSEH2)
- SN65DSI86 and SN65DSI96 Hardware Implementation (SLLA343)

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