Application Note

PCB Design Guidelines for MCF8316C and MCF8315C

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ABSTRACT

PCB design for BLDC motor control applications is an involved process that depends on various factors like cost, form factor, operating conditions, reliability, efficiency, and so on. This application note aims to minimize the PCB design time by providing recommendations for designing PCBs for motor control applications using devices belonging to the MCF831xC family of devices.

Note

MCF831xC refers to TI's latest *Sensorless FOC based integrated FET BLDC drivers* including MCF8316C-Q1, MCF8315C-Q1, and MCF8315C.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

MCF831xC is an all-in-one BLDC driver that integrates motor control logic, gate driver and FET inverter in a single IC for a small form factor complete BLDC driver design for up to 40V industrial and automotive applications. Therefore, the MCF831xC based motor control PCB design includes power and signal/GPIO domains. The power domain section provides recommendations like decoupling caps, buck converter design options (to optimize cost vs. efficiency) and ground connections. The signal/GPIO domain explains the recommended connections for each GPIO along with a detailed internal IO pad structure to help the end user make the correct design choice for the end their application. The power and signal domain recommendations are collated as three examples of PCB schematic and layout with different ground plane and power management options.

2 Power Pin Design Recommendations

MCF831xC needs a minimum of five capacitors for operation: VM-PGND, CPH-CPL, CP-VM, AVDD-AGND, and DVDD-DGND. The detailed design recommendations for the power pins are included in the following sections.

2.1 VM

VM is the main power supply to MCF831xC devices and powers the charge pump, buck converter and AVDD LDO in addition to powering the 3-phase inverter that drives the BLDC motor. Typically, a bulk capacitor ranging from 10s-100s of µF depending on the allowable ripple, motor phase currents, switching frequency (decided by end user system requirements) is added between VM and PGND pins. VM bulk capacitor voltage rating needs to be at least twice the VM voltage.

2.2 Charge Pump: CPH, CPL, CP

MCF831xC devices have an integrated charge pump to drive the high-side (HS) FETs. The charge pump needs two external capacitors – a fly cap between CPH and CPL pins rated at 47nF, (twice the VM voltage) and a bucket cap between CP and VM pins rated at 1uF, 16V. The charge pump output (CP) is for internal circuits only and cannot drive any external loads (like a high-side pass FET for reverse blocking, and so on).

2.3 Buck Converter: FB_BK, SW_BK, GND_BK

MCF831xC has an integrated buck regulator that can provide up to 170mA of external load current at a user configurable voltage (3.3 or 4 or 5 or 5.7V). Depending on the external load current requirements, the buck regulator can be operated in inductor or resistor mode to optimize costs against load current capability.

To further optimize costs, the buck regulator can be disabled by setting BUCK_DIS bit in EEPROM to 1b and connecting FB_BK to AVDD. Refer to Section 3.5 for more details.

2.4 AVDD

MCF831xC has an integrated LDO that can provide up to 20mA of external load current at 3.3V. The AVDD LDO input can either be VM or FB_BK – using FB_BK as AVDD LDO input reduces the internal power losses and improves the thermal performance of MCF831xC. Buck regulator can used as AVDD LDO input by setting BUCK_PS_DIS to 0b and BUCK_SEL to 01b (5V) or 11 (5.7V). AVDD needs a decoupling cap rated at 1uF, 10V connected between AVDD and AGND pins.

2.5 DVDD

MCF831xC has an integrated LDO for powering internal digital circuits at 1.5V. The DVDD LDO input is from FB_BK. DVDD needs a decoupling cap rated at 1uF, 10V connected between DVDD and DGND pins.

2.6 PGND, AGND, DGND

PGND refers to the power ground and is the return path from VM supply. AGND and DGND are low voltage signal grounds and return path for AVDD and DVDD respectively. TI recommends a two-ground plane layout one for PGND and another for GND_BK, AGND, DGND for better noise performance as shown in Figure 5-6. However, to optimize PCB costs, it is acceptable to use a single ground plane layout as shown in Figure 5-2.

2.7 Thermal Pad

MCF831xC devices have a thermal pad for better heat dissipation. This thermal pad needs to be connected to AGND and as large a copper plane as possible on end application PCB for maximizing heat dissipation.

Table 2-1. MCF831xC Power Section Components

PIN1	PIN2	Component value			Unit	% variation across op. conditions	Recommended rating
		Min.	Typ.	Max.			
VM	PGND	10			µF	NA	Twice the VM voltage
CP	VM	32.9	47	61.1	nF	30	Twice the VM voltage
CPH	CPL	0.7	1	1.3	µF	30	16V
AVDD	AGND	0.7	1	1.3	µF	30	10V
DVDD	DGND	0.7	1	1.3	µF	30	10V
FB_BK	GND_BK	15.4	22	28.6	µF	30	10V
SW_BK	FB_BK	37.6	47	56.4	µH	20	I_{sat} >= 1.0A for BUCK_CL = 0
		17.6	22	26.4	µH	20	I_{sat} >= 0.5A for BUCK_CL = 1
		20.9	22	23.1	Ω	5	1W

3 MCF831xC Buck Regulator Overview

3.1 Buck Regulator Mode of Operation

MCF831xC has an integrated buck regulator for providing power to low-voltage (≤5V) internal as well as external circuits. Depending on the external load, the buck regulator can be operated either in inductor mode or in resistor mode as shown in Figure 3-1 and Figure 3-2. If external load is > 10mA, buck regulator needs to be operated in inductor mode and if external load ≤ 10mA buck regulator can be operated in resistor mode to reduce BOM cost

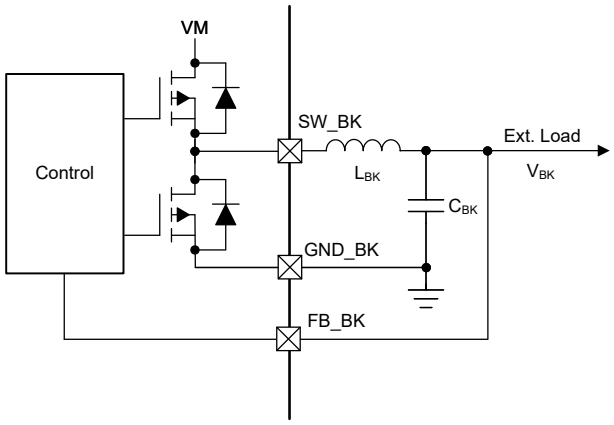


Figure 3-1. Regulator Buck in Inductor Mode

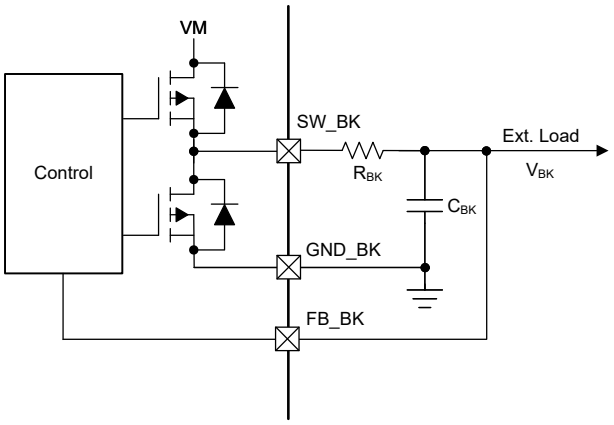


Figure 3-2. Regulator Buck in Resistor Mode

In inductor mode, buck regulator operates as a conventional switching regulator providing high efficiency. In the inductor mode, there are two inductor options to optimize between cost and performance. For external load ≤ 20mA, a 22µH inductor can be used for lower BOM cost and for external load > 20mA, a 47µH inductor needs to be used.

In resistor mode, buck regulator operates as a pseudo LDO wherein a majority of the losses are dissipated in the external resistor instead of within MCF831xC thereby allowing higher power delivery to the BLDC motor. Resistor wattage depends on VM voltage. Refer to Table 3-1 for resistor wattage calculation.

Table 3-1. Resistor Wattage Calculations

VM	12	24	35	V
Buck voltage, V_{BK}	5	5	5	V
Buck load from internal circuits, (BUCK_PS_DIS = 0b, I_{BK_EXT} = 0mA)	30	30	30	mA
Power rating	0.21	0.57	0.90	W

In both the modes, a 22µF capacitor needs to be connected across the buck regulator output (FB_BK and GND_BK) to maintain peak to peak voltage ripple within 200mV. Refer to Table 3-2 for detailed specifications of buck regulator inductor/resistor and capacitor.

Table 3-2. Buck Regulator Configuration Depending on External Load

External Load on Buck Output (mA)	Mode of Operation	Buck Current Limit, BUCK_CL (mA)
$0 \le I_{BK\_EXT} \le 10$	Resistor, 22Ω	150 (BUCK_CL =1b)
$10 < I_{BK\_EXT} \le 20$	Inductor, 22µH	150 (BUCK_CL =1b)
$20 < I_{BK\_EXT} \le 170$	Inductor, 47µH	600 (BUCK_CL =0b)

3.2 Buck Regulator Output Voltage

Buck regulator has four user configurable output voltage levels that can be configured by BUCK_SEL. Table 3-3 shows the summary of available configuration and use case.

Table 3-3. Buck SEL Configuration Summary

BUCK_SEL	Buck Voltage, V	Use Case
00b	3.3	To drive external 3.3V rated microcontrollers directly
01b	5.0	To drive external 5.0V rated microcontrollers directly
10b	4.0	Supply for external LDO to support 3.3V rated microcontroller
11b	5.7	Supply for external LDO to support 5.0V rated microcontroller

3.3 Buck Power Sequencing

MCF831xC has an option of powering the AVDD LDO using the buck regulator instead of VM to reduce the power losses inside the IC and improve thermal performance. This option can be enabled by setting BUCK_PS_DIS to 0b as shown in Figure 3-3. Buck power sequencing is available only when the buck regulator output voltage is set to 5V or 5.7V (BUCK_SEL = 01b or 11b).

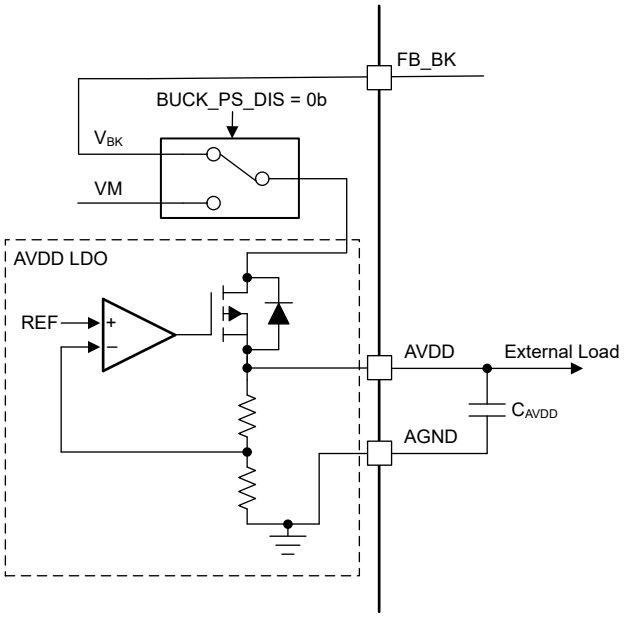


Figure 3-3. Buck Regulator Power Sequencing

3.4 Buck Inductor Selection

Table 3-4. Mapping Inductor Spec to MCF831xC Buck Regulator Specs

Description	Inductor specification	MCF831xC buck regulator specification
Value	47µH (for BUCK_CL = 0b) 22µH (for BUCK_CL = 1b)	47µH ± 20% tolerance(for BUCK_CL = 0b) 22µH ± 20% tolerance (for BUCK_CL = 1b)
Inductance at I_{sat}	Depends on vendor	MCF831xC buck regulator implements a pulse frequency modulation (PFM) scheme with peak current mode control – when inductor current reaches BUCK_CL limit, high-side FET in buck regulator is turned off. Due to internal circuit delay, inductor peak current can go up to 0.5A for BUCK_CL = 1b (Typ: 150mA) and up to 1A for BUCK_CL = 0b (Typ: 600mA). Tolerance spec at I_{sat} depends on vendor and expected range is 10% to 50%. Below is the minimum required inductance and I_{sat} for a given BUCK_CL setting. Inductance = 17.6µH at I_{sat} = 0.5A for BUCK_CL = 1b Inductance = 37.6µH at I_{sat} = 1A for BUCK_CL = 0b
DCR	DC resistance	Max. DC resistance (across operating conditions) needs to be < 1Ω
I_{RMS}	Typical operating RMS current	Needs to be greater than or equal to max DC load

Note

Recommendation is to use a package with magnetic shielding for better EMI/EMC performance.

3.5 MCF831xC Operation Without Buck Regulator

There is an option to further reduce BOM cost by removing the buck regulator components (inductor/resistor and capacitor) and disabling the buck regulator by setting BUCK_DIS to 1b and BUCK_SEL to 00b (3.3V). The DVDD LDO input is derived from the FB_BK (buck regulator output) pin and hence when the buck regulator is disabled, FB_BK needs to be tied to AVDD (externally on the PCB) for proper device operation. In this case, there is an additional power loss of ((VM-AVDD) x 0.02) W in the AVDD LDO which supplies power to the DVDD LDO instead of the buck regulator. This additional power loss results in reduced power delivery capability of MCF831xC. Alternately, an external 3.3V or 5V supply can be tied to FB_BK (instead of AVDD) to power the DVDD LDO and eliminate the additional power loss in AVDD LDO.

4 MCF831xC IO Pins Design Recommendations

MCF831xC has digital as well as analog IO pins. SPEED (PWM/Freq. mode), FG, SCL, SDA, EXT_WD, EXT_CLK, DIR, BRAKE, DRVOFF, nFAULT and ALARM pins are digital IO pins while SPEED (analog mode), DACOUT1/2, SOX are analog IO pins. The internal IO structure and connection recommendation for each pin is detailed in the following sections.

4.1 SPEED Pin

Figure 4-1 shows the IO structure of the SPEED pin. SPEED pin has dual capability and can function either as an analog input (SPEED_MODE = 00b) or as digital input (SPEED_MODE = 01b or 11b). The SPEED pin has an 1MΩ internal pull-down resistor for noise immunity – pull-down resistors can be added externally for additional noise immunity.

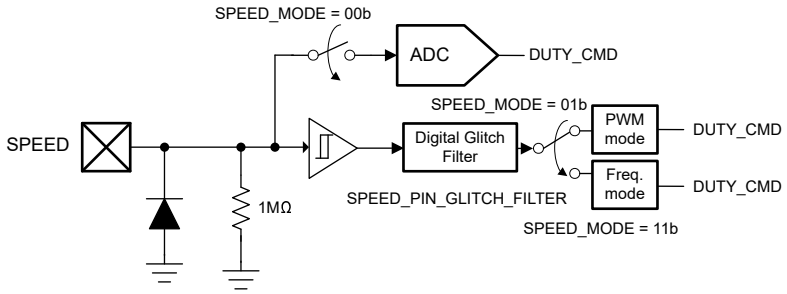


Figure 4-1. SPEED Pin IO Structure

In analog mode, the SPEED input is connected to one of the ADC channels to convert the reference input to DUTY_CMD. In digital mode, SPEED input passes through a digital buffer followed by a user configurable glitch filter (using SPEED_PIN_GLITCH_FILTER to remove glitches up to 1µs) before getting converted into DUTY_CMD.

Table 4-1. SPEED Pin Glitch Filter Setting vs Glitch Width

SPEED_PIN_GLITCH_FILTER	Glitch Width (µs)
00b	No glitch filter
01b	0.2
10b	0.5
11b	1

When used, SPEED pin (analog or digital) needs to be directly connected to the input source.

When unused, SPEED pin needs to be tied to AGND directly.

4.2 BRAKE, DIR, DRVOFF pins

BRAKE, DIR, DRVOFF are digital input pins with IO structure as shown in Figure 4-2. These pins have an 100kΩ internal pull-down resistor for noise immunity.

- BRAKE pin (active high) is used to stop the motor quickly by applying a brake (all low-side FETs are ON).
- DIR pin is used to set the direction of rotation. A logic low level provides A->C->B while a logic high level provides A->B->C.
- DRVOFF (active high) is used to immediately stop powering the motor by placing the FETs in Hi-Z state.

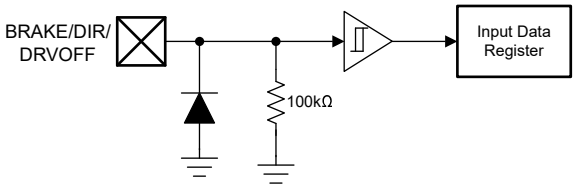


Figure 4-2. BRAKE, DIR, and DRVOFF IO Structure

When used, these pins needs to be directly connected to the input source.

When unused, these pins needs to be tied to AGND directly.

4.3 EXT_CLK, EXT_WD

EXT_CLK, EXT_WD are digital input pins with IO structure as shown in Figure 4-3. These pins have an internal buffer with hysteresis.

- EXT_CLK is an optional external clock input to improve the speed accuracy across temperature. MCF831xC, by default, uses the internal oscillator and provides a speed accuracy of 3% – EXT_CLK is used only when a better speed accuracy (< 3% error) is necessary.
- EXT_WD is an optional watchdog input to monitor the health of the external MCU.

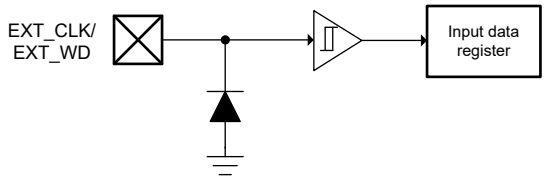


Figure 4-3. EXT_CLK and EXT_WD IO Structure

When used, these pins need to be directly connected to the input source with an external 100kΩ pull-down resistor.

When unused, these pins need to be tied to AGND directly.

4.4 ALARM

ALARM is a digital output pin with IO structure as shown in Figure 4-4. This is a push-pull output that indicates fault state as an active high signal.

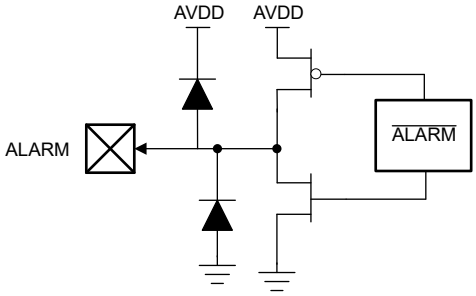


Figure 4-4. ALARM IO Structure

When used, ALARM pin needs to be directly connected to the external MCU/circuit reading the ALARM state.

When unused, ALARM pin needs to be left floating.

4.5 DACOUT1, DACOUT2

DACOUT1/2 are analog output pins with IO structure as shown in Figure 4-5. The DACOUT pins are enabled using DAC_ENABLE. These pins are used to monitor internal variables and system parameters like DC bus current, voltage, motor speed, and so on, as an analog voltage ranging between (0-3) V.

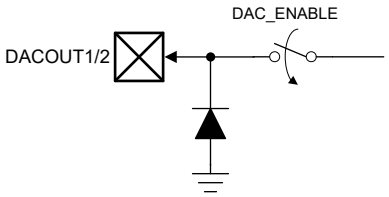


Figure 4-5. DACOUT1/2 IO Structure

When used, DACOUT1/2 pins need to be connected to a high impedance circuit since the signals are unbuffered. An optional R-C filter can be added externally for noise filtering.

When unused, DACOUT1/2 pins need to be left floating.

4.6 SDA, SCL

SDA, SCL are digital input (SDA has dual function of output also) pins with IO structure as shown in Figure 4-6. The input path has a buffer with hysteresis followed by a 50ns glitch filter to suppress noise.

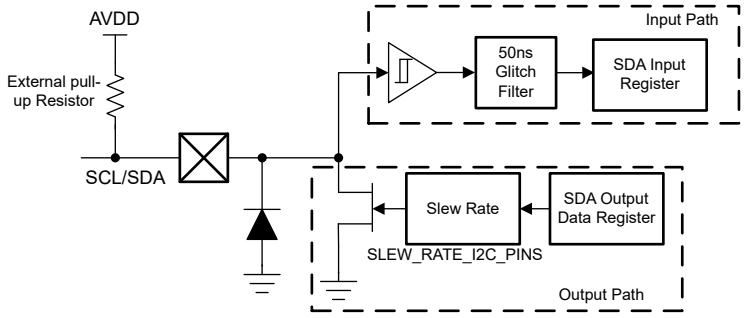


Figure 4-6. SCL, SDA IO Equivalent Circuit

The output path is an open drain that needs an external pull-up resistor to AVDD for I2C communication. The pull-down drive strength (Slew rate) can be configured using SLEW_RATE_I2C_PINS to optimize between timing requirements, EMI and cross talk. Default pull-down drive strength is 4.8mA and this can drive up to 400pF bus capacitance. If system has a lower bus capacitance, a lower pull-down drive strength can be selected. Pull-up resistor depends the I2C clock frequency and bus capacitance [2].

Table 4-2. I2C Pins Drive Strength

SLEW_RATE_I2C_PINS	Pull-Down Drive Strength (mA)
00b	4.8
01b	3.9
10b	1.86
11b	30.8

When used, these pins need to be directly connected to the external MCU with an external pull-up resistor to AVDD.

When unused, these pins need to be left floating.

4.7 nFAULT and FG pin

nFAULT, FG are digital output pins with IO structure as shown in Figure 4-7. These are open drain pins that need a pull-up resistor for proper operation. MCF831xC provides an option of internal pull-up resistor to AVDD that can be enabled by setting PULLUP_ENABLE to 1b. If a logic level (MCU IO power rail) other than 3.3V is needed for FG, nFAULT signals, then PULLUP_ENABLE need to be set to 0b and an external pull-up resistor to required voltage level need to be connected.

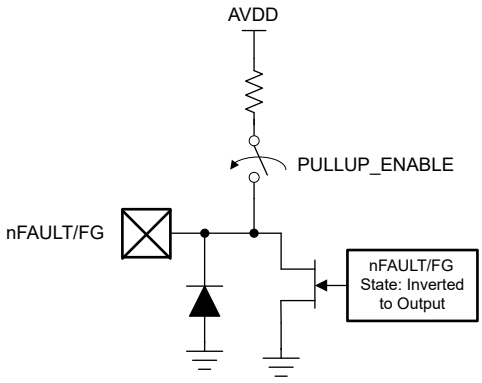


Figure 4-7. nFAULT and FG IO Equivalent Circuit

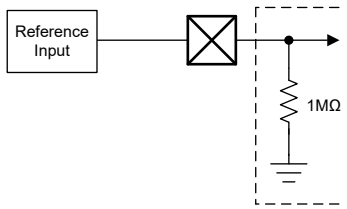
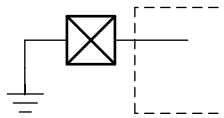
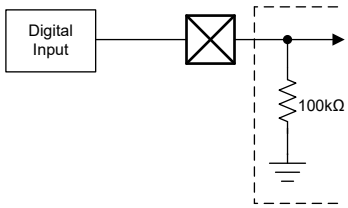
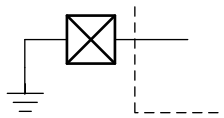
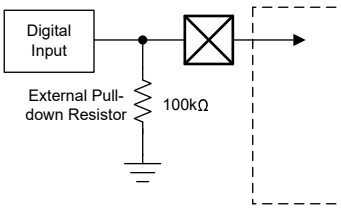
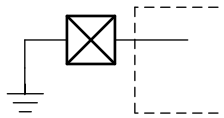
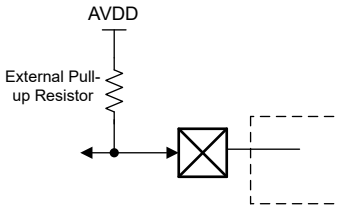
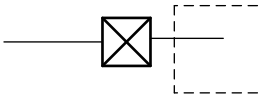
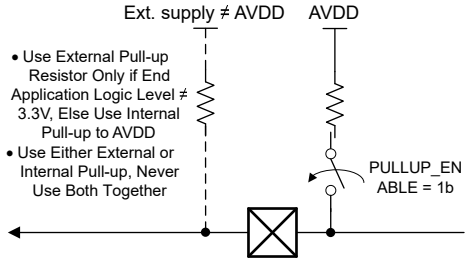
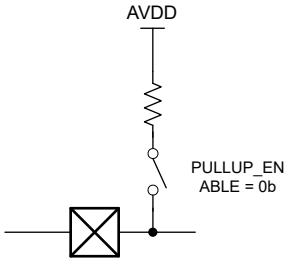
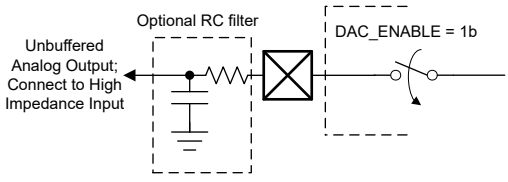
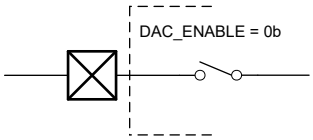
When used, these pins need to be pulled up (either internally or externally) to required logic level.

When unused, these pins need to be left floating.

Note

Internal pull-up resistors for FG, nFAULT are available only in MCF831xC and not in MCF831xA. In MCF831xA, FG needs an external pull-up to AVDD (even when unused) for normal operation.

Table 4-3. MCF831xC IO Pin Recommendations

Pin	Recommendation When Used	Recommendation When Unused
SPEED		
BRAKE, DIR, DRVOFF		
EXT_WD, EXT_CLK		
SCL, SDA		
nFAULT, FG		
DACOUT		

5 MCF831xC PCB Schematic and Layout Recommendations

5.1 Single Ground Plane

For low cost applications, wherein switching noise coupling between power ground and signal ground is not critical, short all ground pins together. Refer to Figure 5-1 and Figure 5-2 for a sample schematic and layout for a single ground plane PCB.

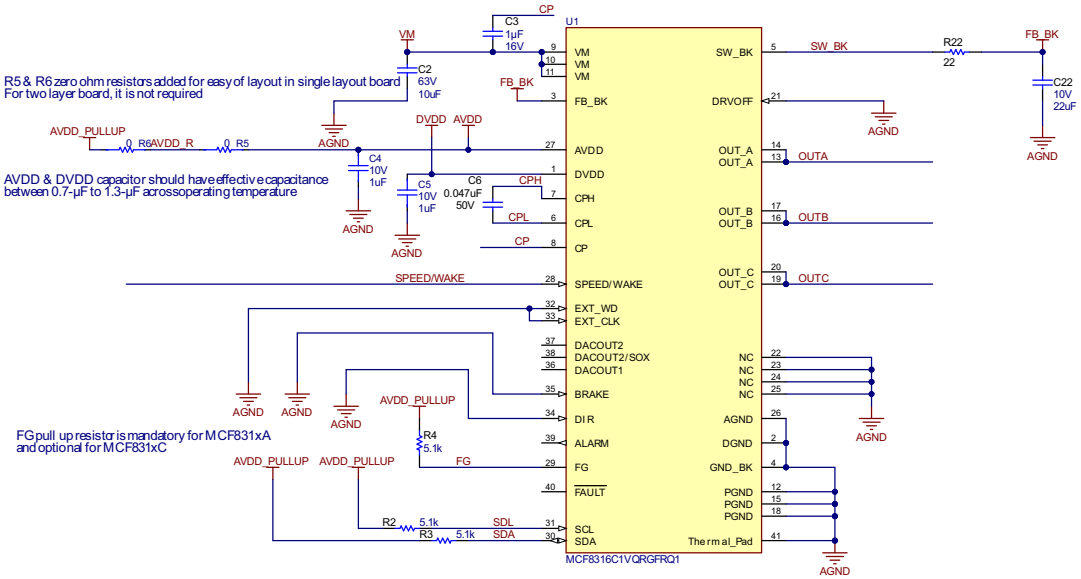


Figure 5-1. PCB Schematic for Single Ground Plane

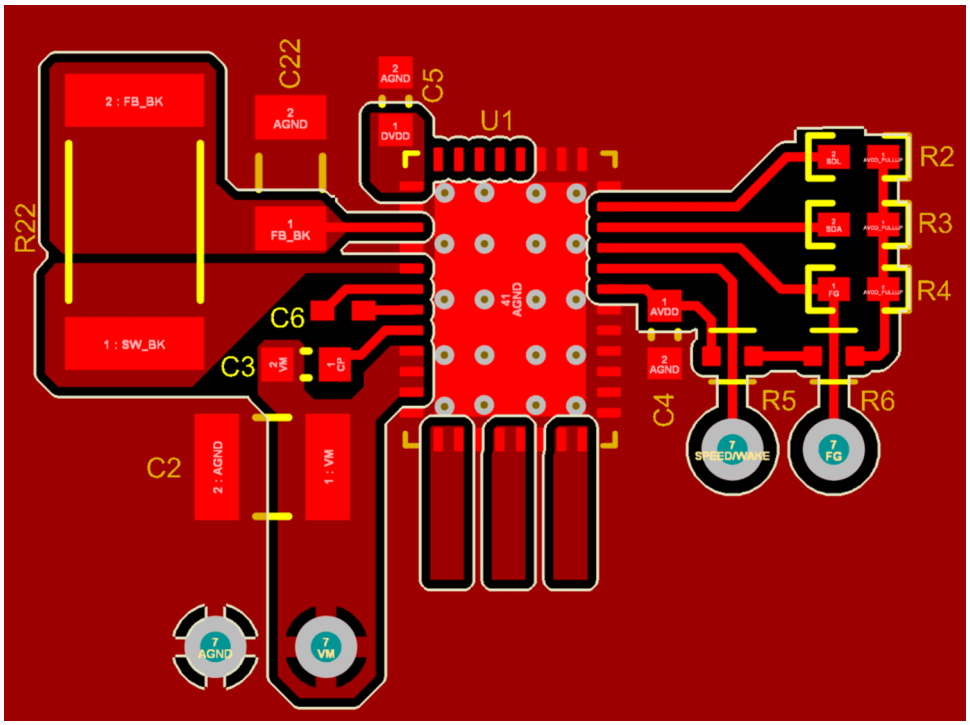


Figure 5-2. PCB Layout for Single Ground Plane

5.2 Single Ground with AVDD Shorted to FB_BK

As shown in Section 4.7, for low power/cost applications where the buck regulator is disabled, the recommendation is to connect FB_BK and AVDD externally on the board. Refer to Figure 5-3 and Figure 5-4 for a sample schematic and layout for a single ground plane PCB. One additional capacitor 1uF(C7) is added close to FB_BK due to long trace from AVDD to FB_BK.

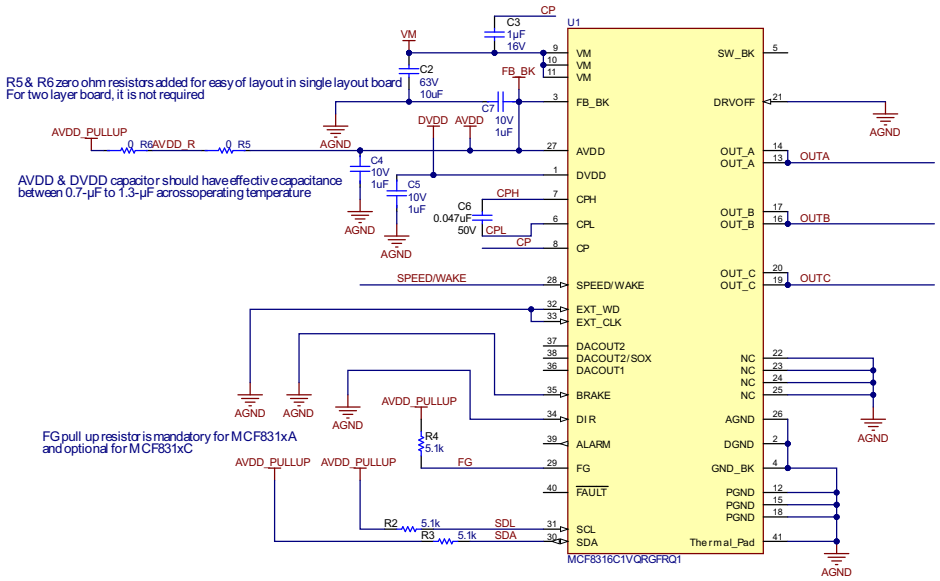


Figure 5-3. PCB Schematic for Single Ground Plane and FB_BK Powered by AVDD

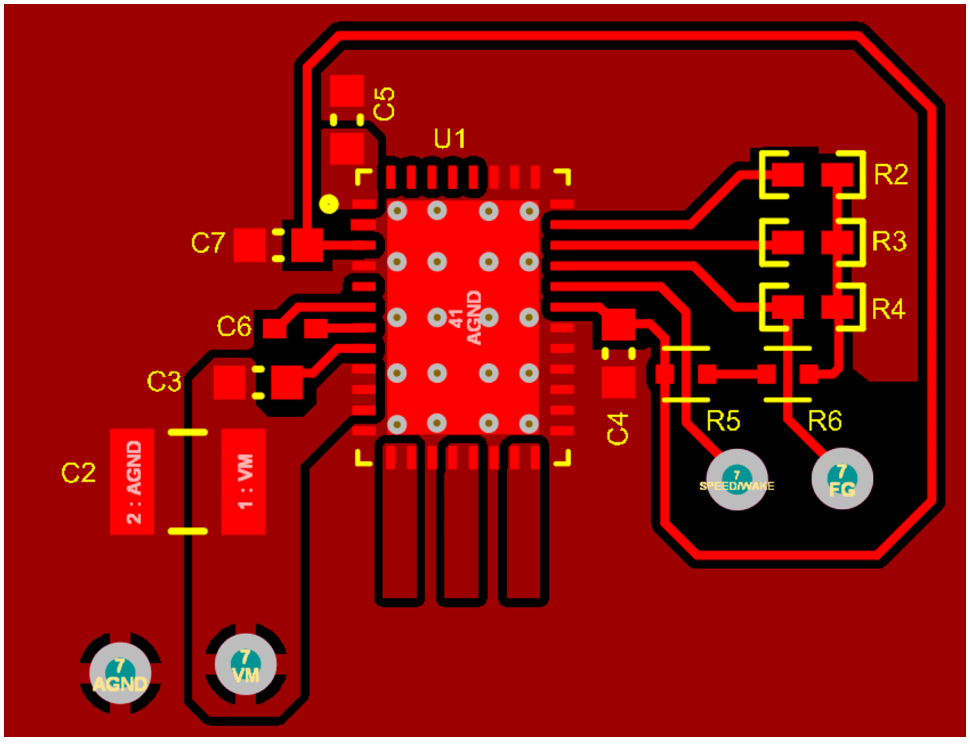


Figure 5-4. PCB Layout for Single Ground Plane and FB_BK Powered by AVDD

5.3 Two Grounds

For high performance applications, to avoid noise coupling between power and signal grounds, two ground planes can be used. Use one ground for AGND, DGND and GND_BK and another ground for PGND. Refer to Figure 5-5 and Figure 5-6 for a sample schematic and layout for a single ground plane PCB.

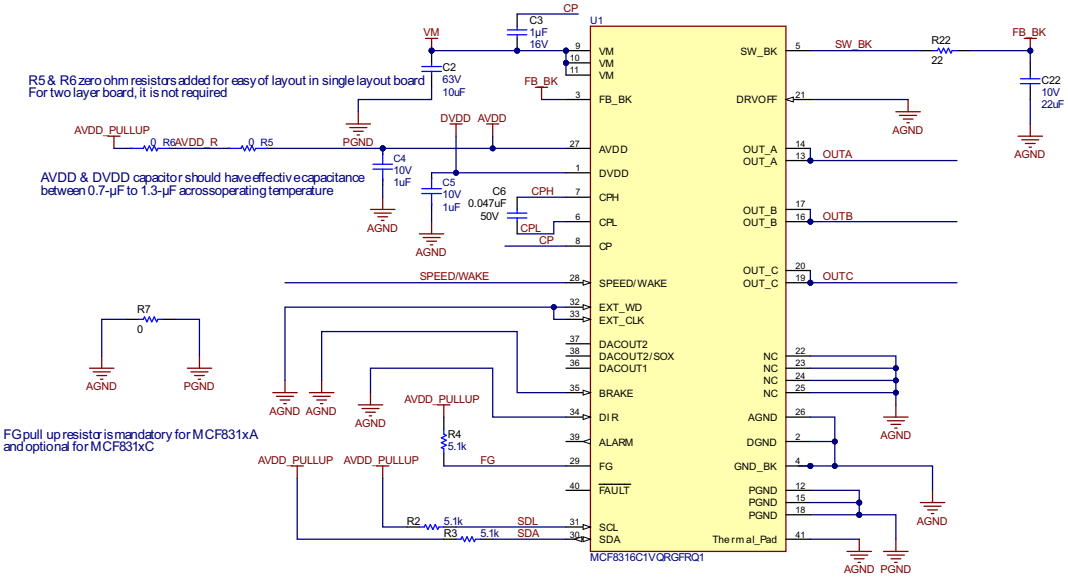


Figure 5-5. PCB Schematic for Two Ground Planes (AGND and PGND)

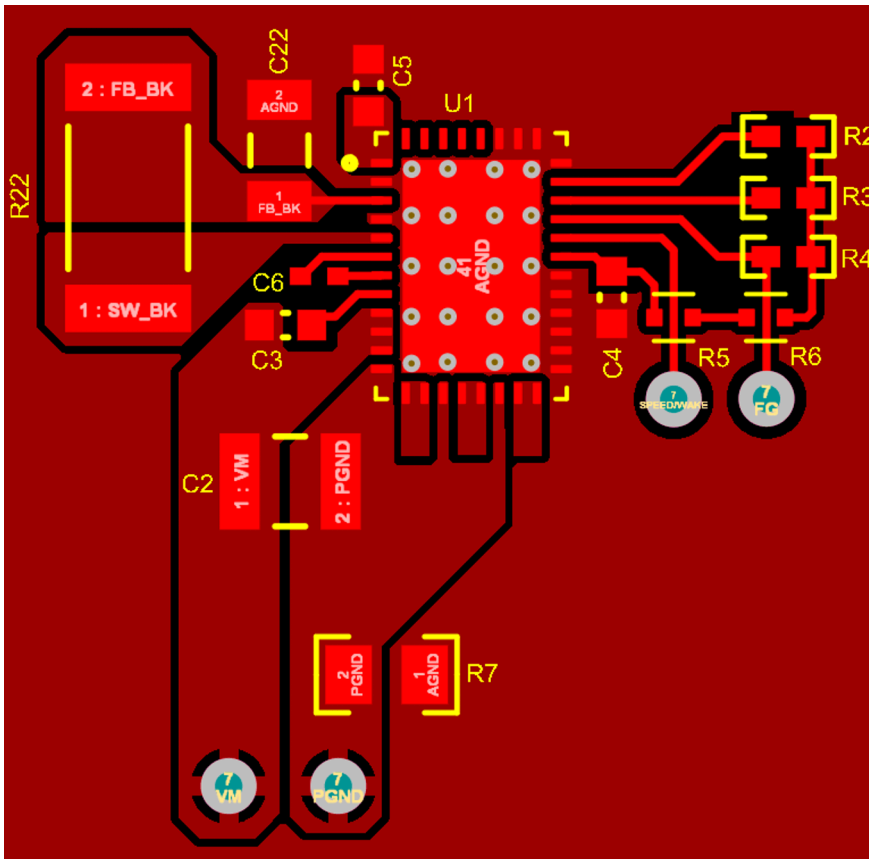


Figure 5-6. PCB Layout for Two Ground Planes (AGND and PGND)

6 Summary

This application note provides guidelines on designing PCBs with MCF831xC devices – the guidelines are intended to help end user accelerate the PCB design process. The component spec recommendations are based on the design and characterization of MCF831xC and end user must make sure that the spec recommendations are met or exceeded across operating conditions like voltage, temperature, process, and so on, for reliable operation. The layout suggestions are provided as an example to help end user get started with PCB design for different power and ground architectures – final PCB design can depend on comprehensive end user system level testing across operating conditions.

7 References

1. Texas Instruments, *Implications of Slow or Floating CMOS Inputs,* application note.
2. Texas Instruments, *I2C Bus Pullup Resistor Calculation,* application note.
3. Mouser, *Selecting the Optimal Inductor for Power Converter Applications,* white paper.
4. Coil Craft, *Selecting the Best Inductor for Your DC-DC Converter,* application note.
5. MuRata, *The voltage characteristics of electrostatic capacitance,* capacitor guide article.
6. Murata, *What is the temperature characteristics of ceramic capacitors,* capacitor guide article.

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