Application Note

How to Optimize MCF8315 Hardware Design in Fan Application

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ABSTRACT

The MCF831x is an integrated code-free sensorless FOC device, which can be widely used in appliances system, such as residential fans, ceiling fans, air purifiers, washer pumps, and so forth. The high integration and code-free of MC8315 brings great convenience to the development and use of customers, but there are also some common challenges with BLDC design. This application note introduces how to design the hardware of MCF8315 and proposes how to simplify the peripheral design, and provides temperature performance result for design reference.

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1 Introduction

The MCF8315 provides users with a single-chip, code-free, sensorless FOC design for driving 12V to 24V brushless DC motors(BLDC) that require up to 4A peak phase current and have speed loop/current loop/power loop/Voltage loop. The MCF8315 integrates three half-bridges with 40V absolute maximum voltage and low RDS(ON) (high side + low side) of 240mΩ(RGF)/250mΩ(RRY)/265mΩ(PWP) in different packages for high-power drive capability. An integrated current sensing circuit is used to sense the current, eliminating the need for an external current sensing resistor. Power management features with adjustable buck regulators and LDOs generate the necessary voltage rails for the device, which can also be used to power external circuits.

The MCF8315 implements sensorless FOC, so no external microcontroller is required to rotate a brushless DC motor. The algorithm is implemented in a fixed-function state machine (configured via the motor studio host computer), so no manual programming is required. From motor start-up to closed-loop operation, the algorithm is highly configurable through I2C register settings. Register settings can be stored in non-volatile EEPROM (20,000 erases and writes), allowing the device to operate independently after configuration. The device receives speed commands through PWM, VSP, DUTY or I2C commands to achieve closed-loop control according to the speed curve.

1.1 MCF8315 Block Diagram and Pin Functions Introduction

Figure 1-1 is MCF8315 system block diagram and pin functions introduction.

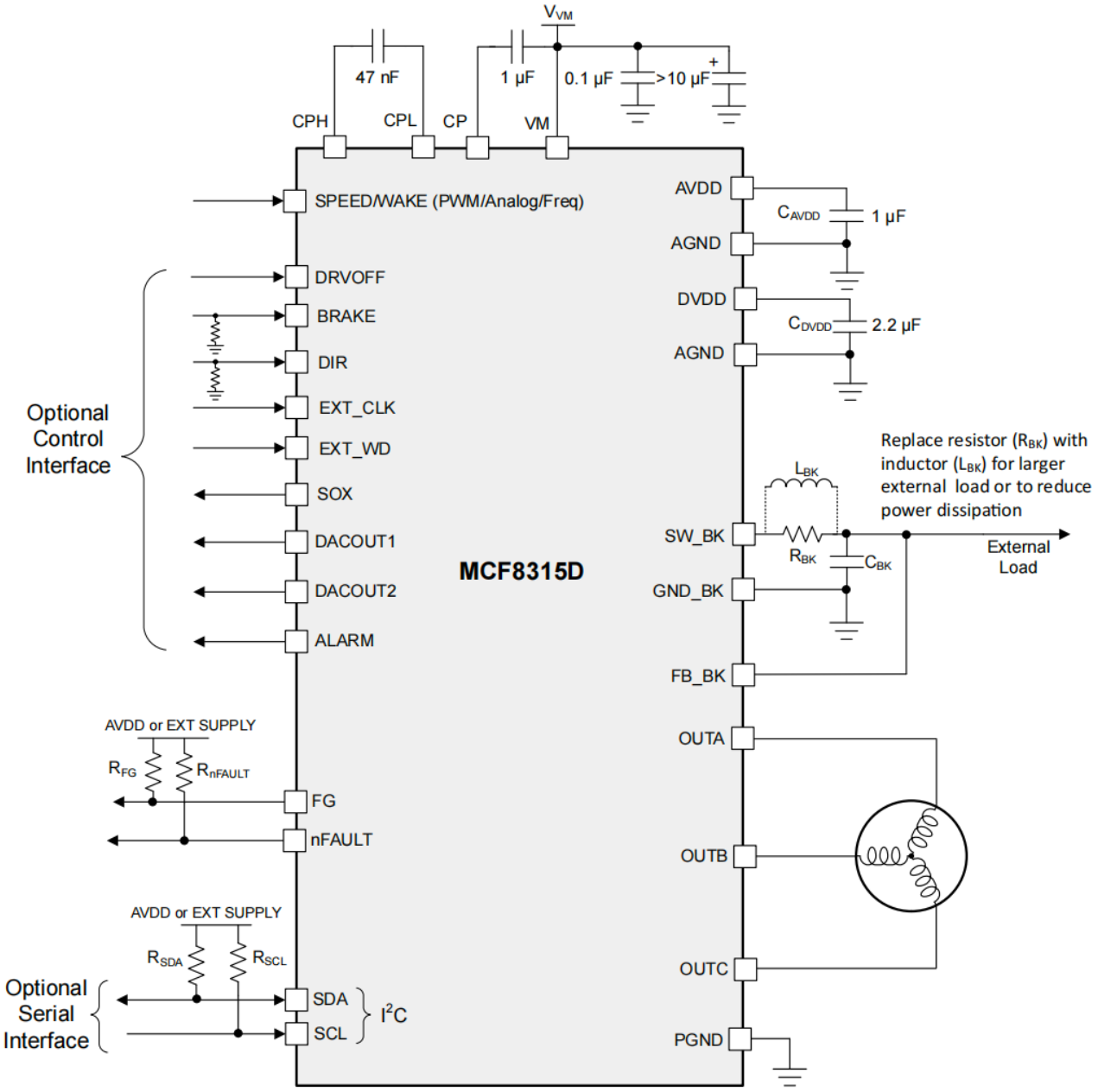

Figure 1-1. MCF8315 Block Diagram

Table 1-1. MCF8315 Pin Functions

Power Part		
Pin	**Type**	**Description**
VM	PWR	5 to 40VIN voltage input
SW_BUCK	PWR	Buck switch node, connect this pin to an inductor or resistor
AVDD	PWR O	Support 3.3V 3.3V LDO output, external 1uF capacitor to ground This regulator can provide 20mA current to the external (Need min 500nF effective capacitance across voltage and temperature. Can be 1uF or 2.2uF)
DVDD	PWR	External 1uF capacitor to ground (Need min 500nF effective capacitance across voltage and temperature. Can be 1uF or 2.2uF)
CPH,CPL	PWR	Charge pump switch node, connect a X7R, 47nF ceramic capacitor between the CPH and CPL pins, the recommendation that the rated voltage of the capacitor is at least twice the normal operating voltage of the device
CP	PWR	Charge pump output, connect a X7R, 1µF, 16V ceramic capacitor between the CP and VM pins
FB_BK	PWR I/O	The feedback pin of the buck regulator output control, the buck regulator output after connecting the inductor/resistor. Aan also be provided by external LDO voltage/connected to AVDD,then the inductor/resistor of SW_BUCK can be omitted. (Buck provides 4 different output voltage options: 3.3/4/5/5.7V)
Function Part		
SPEED/ WAKE	I	Speed command input, supports PWM/DUTY/VSP input With an internal pull-down resistor of 1MΩ
FG	O	Speed output signal, open drain output
nFAULT	O	Fault indication, pull down to low level under fault condition, PULLUP_ENABLE sets pull-up (PULLUP_ENABLE enables internal pull-up to 3.3V and no external pull-up is needed when this feature is enabled)
DRVOFF	I	DRVOFF is high level, and the six MOSFET outputs are in high impedance state. If the DRVOFF pin is not used, connect directly to AGND (single point grounding). If the DRVOFF pin is used to achieve MOSFET output high impedance state, connect an external 10k resistor to AGND for better noise suppression.
BRAKE	I	High level → brake motor Low level → normal motor operation If the BRAKE pin is not used, connect directly to AGND (single point grounding).
DIR	I	When low, the phase drive sequence is OUT A → OUT C → OUT B When high, the phase drive sequence is OUT A → OUT B → OUT C If DIR pin is not used, connect directly to AGND ,direction can be set using EEPROM setting If DIR pin is used to change the motor rotation direction, connect an external 10k resistor to AGND for better noise suppression.
EXT_CLK	I	External clock reference input in external clock reference mode Speed loop accuracy: 3% using internal clock, 1% using external clock reference(optional)
EXT_WD	I	External watchdog input(optional)
DACOUT	O	DAC output
Communication Part		
SCL/SDA	I/O	I2C clock & data
Motor Output Part		
OUTA/B/C	PWR O	Three-phase U/V/W half-bridge motor output, no external current detection resistor required

2 Fan Application Hardware Architecture

For the Fan application, most of the voltage or power level is 12 to 24V and <45W. Normal fan application such as (ventilation exhaust fans, ceiling fans, water pumps, gas wall-mounted boilers, and so on), and generally hardware architecture shown in the following:

2.1 Total Discrete Hardware Design

This design includes the architecture of processor MCU + half-bridge driver + MOSFET + current amplifier circuit + current detection circuit + protection unit. The advantage is that different materials and specifications can be flexibly selected to achieve higher power and better temperature rise. The disadvantage is that the material cost is high, and the PCB area is limited by the motor size. For example, for a 48mm/60mm motor, the internal clearance diameter of the stator is about 25mm/30mm, resulting in only a 23mm/30mm wide area for component layout in the design, which is hard for engineer to layout.

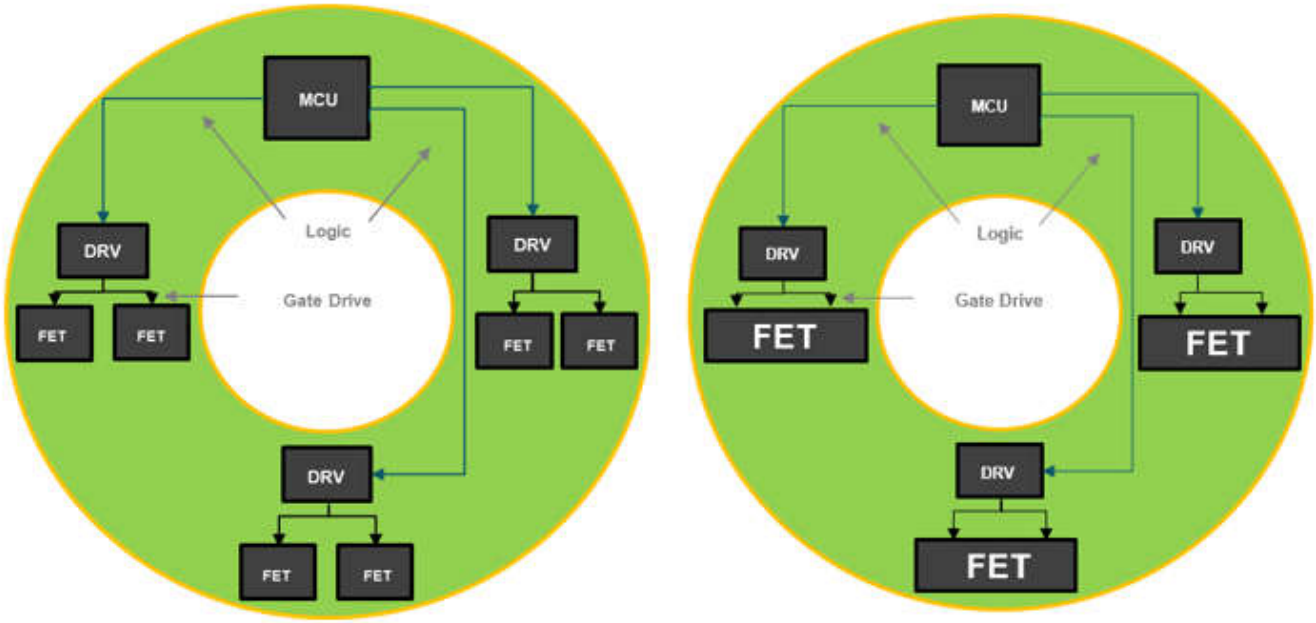

Figure 2-1. Discrete Hardware Design Architecture in Fan Application

2.2 MCU+Pre-Driver and External FET Design

In this design, some MCU device integrate gate driver and built-in current amplification/protection circuits. Users only need to connect external MOSFETs. Compared with the previous design, this can reduce material costs to a greater extent and make this easier for engineers to layout the system. This design is also widely used in the market. The disadvantage is that engineers still need to spend a lot of time on low-level driver debugging and optimizing the motor control algorithm.

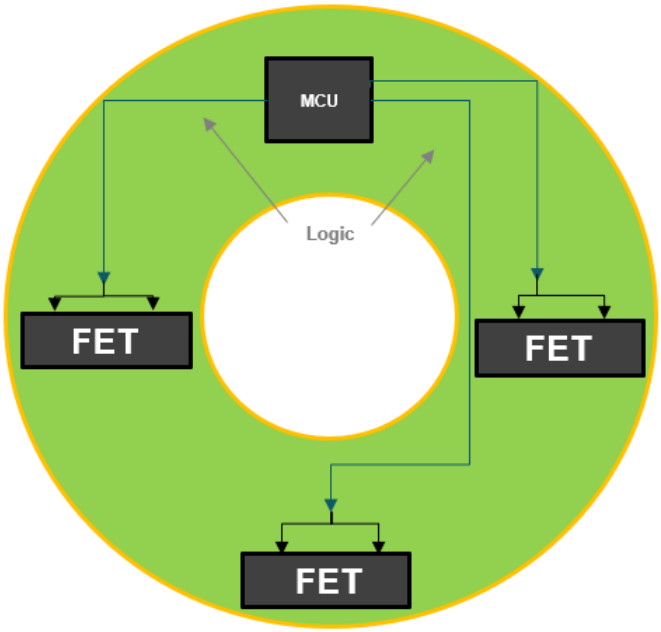

Figure 2-2. MCU+Pre-driver and External FET Architecture in Fan Application

2.3 All in One Design

This design integrates MCU, half-bridge drive circuit, current amplifier, protection circuit, MOSFET, and so on. The fully integrated design saves PCB area to a greater extent without adding additional circuits. And engineers do not need to be experienced in algorithm writing capabilities.

Through the host computer with preset parameters, product development can be completed and project evaluation can be completed faster.

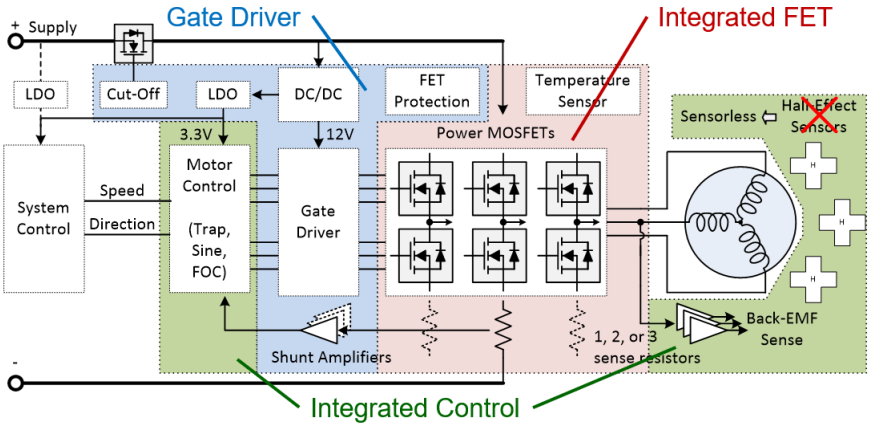

Figure 2-3. All in One Design Architecture in Fan Application

3 MCF8315 Hardware Design Guide for Fan Application

By using TI's MCF8315DVPWPR for design, the total cost of the industrial fan system can be reduced by 20-30%. The following is a system design for the commonly used motor drive design with speed control.

3.1 MCF8315 Power Part Design

According to the pin definition requirements of the data sheet, the design requirements are as follows:

Table 3-1. MCF8315 Power Part Design

Pin	Description
VM	>10uf capacitor to ground and 100nf capacitor to ground, with a withstand voltage twice that of VM input.
VM,CP	Connect a 1μF, 16V capacitor between CP and VM
CPH,CPL	Connect a 47nF capacitor between CPH and CPL, with a withstand voltage twice that of VM input.
AVDD	External 1uF capacitor to ground(Can be 1uF/2.2uF,>500nF across voltage and temperature)
DVDD	External 1uF capacitor to ground(Can be 1uF/2.2uF,>500nF across voltage and temperature)
SW_BUCK	Select the resistance/inductance value according to the load

Table 3-2. Recommended Settings for Buck Regulator

Buck Mode	Buck output voltage	Max output current from AVDD (I_{AVDD_MAX})	Max output current from Buck (I_{BK_MAX})	Buck current limit	AVDD power sequencing
Inductor - 47μH	3.3V or 4V or 5V or 5.7V	20mA	170mA	600mA (BUCK_CL = 0b)	Not supported (BUCK_PS_DIS = 1b)
Inductor - 47μH	5V or 5.7V	20mA	170mA - I_{AVDD}	600mA (BUCK_CL = 0b)	Supported (BUCK_PS_DIS = 0b)
Inductor - 22μH	3.3V or 4V or 5V or 5.7V	20mA	20mA	150mA (BUCK_CL = 1b)	Not supported (BUCK_PS_DIS = 1b)
Inductor - 22μH	5V or 5.7V	20mA	20mA - I_{AVDD}	150mA (BUCK_CL = 1b)	Supported (BUCK_PS_DIS = 0b)
Resistor - 22Ω	3.3V or 4V or 5V or 5.7V	20mA	10mA	150mA (BUCK_CL = 1b)	Not supported (BUCK_PS_DIS = 1b)
Resistor - 22Ω	5V or 5.7V	20mA	10mA - I_{AVDD}	150mA (BUCK_CL = 1b)	Supported (BUCK_PS_DIS = 0b)

3.2 MCF8315 Function Part Design

According to the pin definition requirements of the data sheet, the design requirements are as follows:

Table 3-3. MCF8315 Function Part Design

Pin	Description
SPEED	The SPEED pin can be configured to receive PWM, Frequency or VSP signals.
FG	FG provides pulses proportional to the motor speed, and PULLUP_ENABLE sets the internal pull-up (3.3V)
nFAULT	The nFAULT (active low) pin provides the fault status of the device or motor in operation. The MCF8315 provides a sound state machine protection and recovery mechanism, which can achieve device lock or self-recovery. This design does not have an additional MCU system, and can be left floating or connected to an LED light for reminder
DRVOFF	When the pin is driven to *high level*, the MCF8315 stops driving the motor by setting MOSFET to a high impedance state, when DRVOFF is driven high during motor operation, DRVOFF can be accompanied by faults such as no motor or abnormal back EMF This design has no special requirements for stopping the motor, no external lead is required, and is directly connected to AGND (single point ground)

Table 3-3. MCF8315 Function Part Design (continued)

Pin	Description
BRAKE	When BRAKE_INPUT defaults to 0h = hardware pin brake: When the BRAKE pin is driven to *high level*, the MCF8315 enters the braking state. When BRAKE_INPUT is set to 1h/2h: 1h = pin level is ignored according to BRAKE_PIN_MODE, and the braking state can be configured as low-side braking or alignment braking through BRAKE_PIN_MODE 2h = pin level is ignored, no braking/alignment This design does not use this pin, the brake is set through the register, and is directly connected to AGND (single point ground)
DIR	The DIR pin determines the direction of motor rotation; When the drive is *high level*, the sequence is OUT A → OUT B → OUT C When the drive is *low level*, the sequence is OUT A → OUT C → OUT B This design does not use the DIR pin, and is directly connected to AGND (single point ground) by configuring DIR_INPUT using the I2C interface
EXT_CLK	For low-cost applications, a speed loop accuracy of 3% is sufficient. This design does not use an external clock source, and is directly connected to AGND (single-point grounding)
EXT_WD	This design does not have an additional MCU system, and is directly connected to AGND (single-point grounding)
DACOUT	This design does not need to obtain an analog voltage equivalent to a digital variable, does not need to be led out, and can be left floating.

3.3 MCF8315 Communication and Output Part Design

MCF8315 uses the standard I2C protocol for register communication and reading and writing. The pull-up resistor can be reserved through the burner end, and the corresponding test solder joint can be reserved for the on-board circuit.

Table 3-4. MCF8315 Communication snd Output Part Design

Pin	Description
SCL/SDA	The recommendation is to use a 5.1kΩ pull-up resistor SLEW_RATE_I2C_PINS can also be adjusted according to the parasitic capacitance on the actual PCB board 0h = 4.8mA (default) 1h = 3.9mA 2h = 1.86mA 3h = 30.8mA
OUTA/B/C	No external current detection resistor is required

3.4 MCF8315 Schematic Design Reference

According to the requirements of system design, see the following reference circuit:

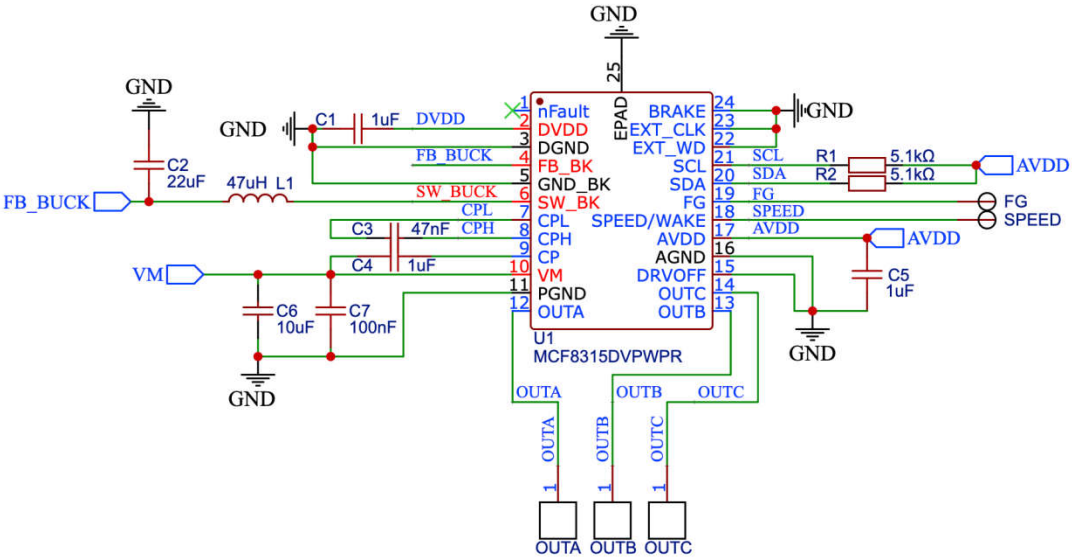

Figure 3-1. MCF8315 Schematic Design Reference

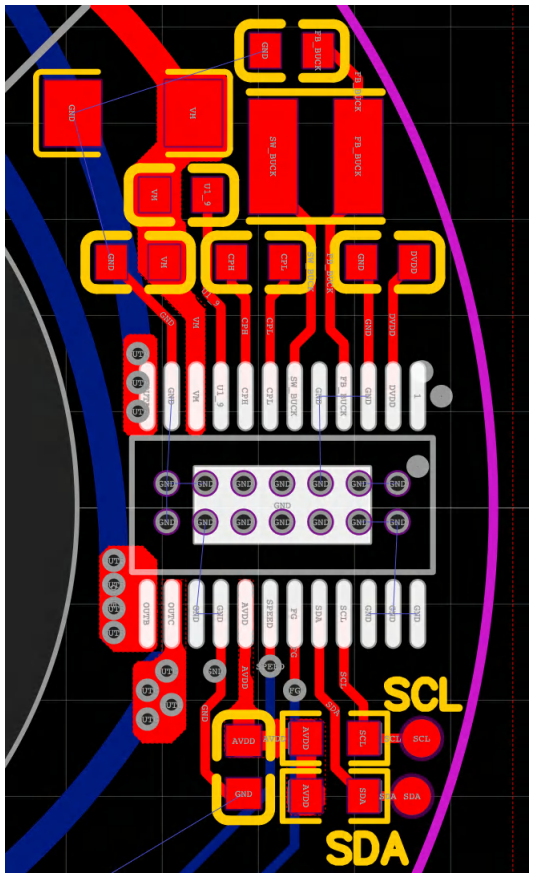

Figure 3-2. MCF8315 Layout Design Reference

MCF8315 design 3D layout reference diagram: outer diameter 48mm, inner diameter clearance 26mm. The PCB peripheral design of this design only occupies an area of 10mm x 22mmm

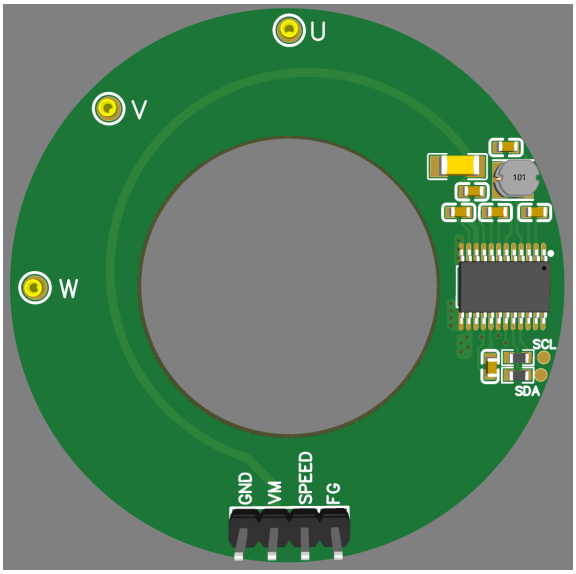

Figure 3-3. MCF8315 Layout Design 3D Picture

We can see only a small number of peripheral devices are needed to complete the hardware design of a 12 to 24V (40Wmax) sensorless FOC motor drive. Users can bring out the corresponding functional module pins according to project needs.

3.5 MCF8315 Simplifies Peripheral Design

The MCF8315 has an integrated hybrid-mode buck regulator that provides 3.3V or 5V regulated power to an external controller or system voltage rail. In addition, the buck output can be configured to 4V or 5.7V to support additional margin for external LDOs to generate 3.3V or 5V power. The buck output voltage is set by BUCK_SEL. However, in the absence of an additional MCU power rail, this inductor/resistor has no effect, but can generate additional material cost and PCB area. This article proposes a new design to optimize the design:

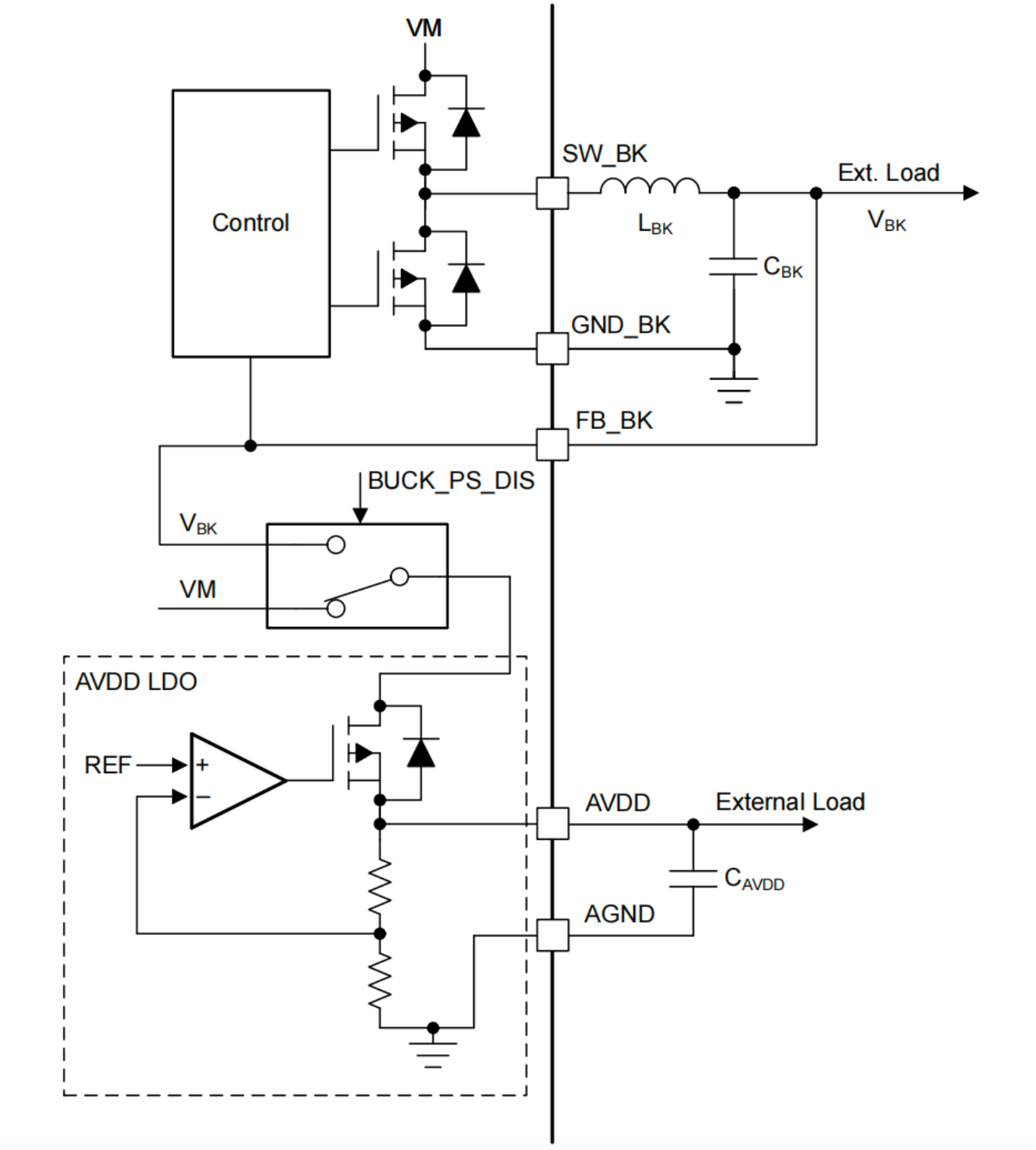

Figure 3-4. MCF8315 Power Sequence

According to the power rail architecture, this can be seen that the power rail of AVDD is provided by Vbuck or VM power supply. If the VBUCK circuit needs to be omitted, the buck regulator needs to be disabled, and BUCK_DIS = 1h (default 0h enables the buck regulator) and BUCK_CL = 1h (the buck regulator current limit is set to 150mA). At this time, the SW_BUCK pin can stop the PWM wave and limit the maximum current. Then set BUCK_PS_DIS = 1b. At this time, the AVDD power rail input path is VM->AVDD.

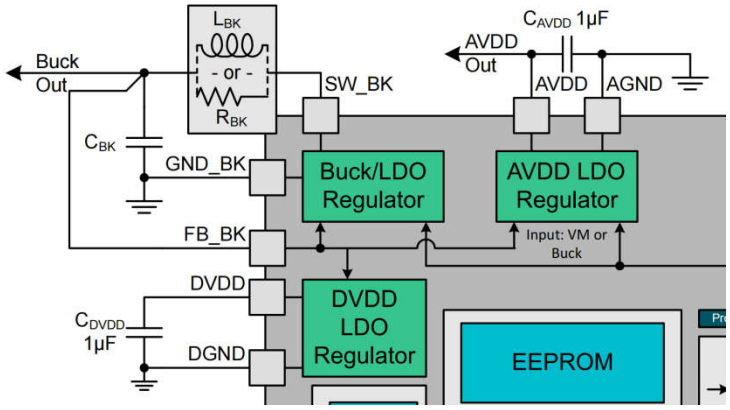

Figure 3-5. MCF8315 Power Rail

According to the power rail indicated in the specification, FB_BK has no voltage at this time, and DVDD is input through FB_BK, so DVDD has no power and the chip cannot work. The previous chapter mentioned that AVDD has a 20mA output capability, and we can connect AVDD to the FB_BK pin. If the FB_BK voltage drops to a low enough level to trigger the Under Voltage on the internal circuit.

At this stage, the power rail input path is changed to: VM->AVDD->FB_BK->DVDD.

The operation summary steps are as follows:

Table 3-5. Step to Simplify Peripheral Design

Step	Register	Setting	Comments
1	BUCK_DIS	1h	Buck regulator disabled
2	BUCK_CL	1h	Buck regulator current limit set to 150mA
3	BUCK_PS_DIS	1h	Buck power sequencing disabled
4	AVDD is routed to the FB_BK pin through the PCB. Avoid routing too long. Add a 1uf ground capacitor next to the FB_BK pin.		
5	BUCK_SEL	0h	Buck voltage set to 3.3V

Also, to reduce the loss between the input voltage and AVDD, an external LDO is also supported to be input to the FB_BK pin to reduce the power loss:

Table 3-6. Step to Simplify Peripheral Design with External LDO

Step	Register	Setting	Comments
1	BUCK_DIS	1h	Buck regulator disabled
2	BUCK_CL	1h	Buck regulator current limit set to 150mA
3	BUCK_PS_DIS	1h	Buck power sequencing disabled
4	External 3V3/5V LDO output to FB_BK pin, add 1uf capacitor to ground		
5	BUCK_SEL	0h	Buck voltage set to 3.3V

Reference Schematic:

Figure 3-6 show we can simplify peripheral design by conncet AVDD to FB_BK.

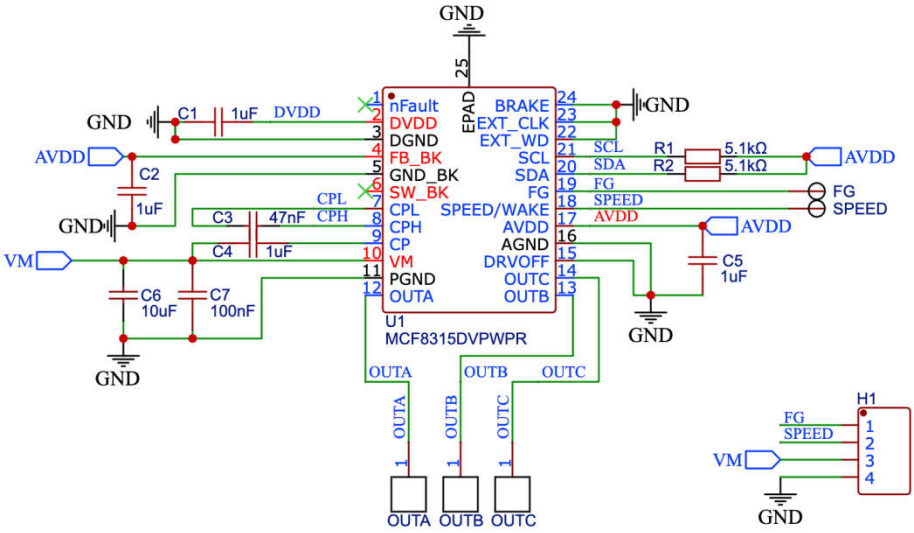

Figure 3-6. MCF8315 Simplifies Peripheral Design Schematic Reference

Reference Layout:

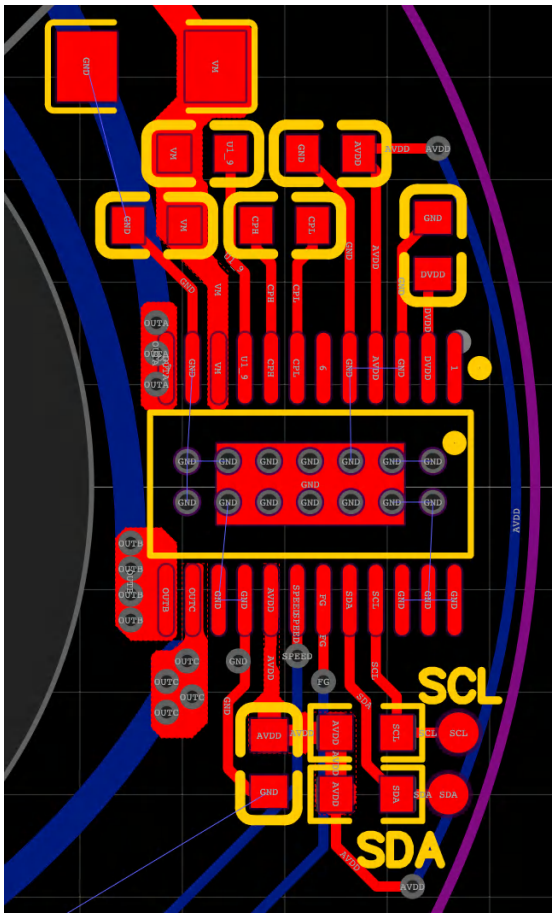

Figure 3-7. MCF8315 Simplifies Peripheral Design Schematic Reference

MCF8315 design 3D layout reference diagram: outer diameter 48mm, inner diameter clearance 26mm. The PCB peripheral design of this design occupies an area of only 10mm x 20mmm

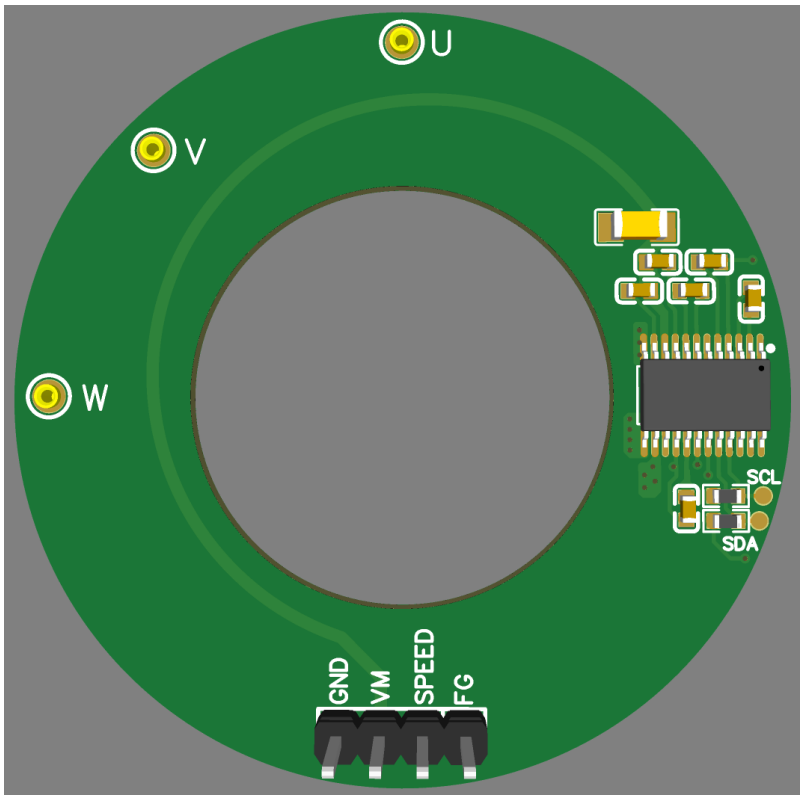

Figure 3-8. MCF8315 Simplifies Peripheral Design Layout 3D Picture

Table 3-7. MCF8315 Simplifies Peripheral Design BOM

ID	Name	Designator	Footprint	Quantity
1	1uF	C1,C2,C4,C5	C0603	4
2	47nF	C3	C0603	1
3	100nF	C7	C0603	1
4	10uF	C6	C1206	1
5	5.1kΩ	R1,R2	R0603	2
6	MCF8315DVPWPR	U1	HTSSOP-24	1

After updating the BOM table (excluding connectors) for comparison, only **7** necessary capacitors are needed to complete this design. This design can reduce the cost of peripheral components and reduce the layout of components while making sure the motor performance remains unchanged to the greatest extent. Of course, this can also introduce the problem of increased power consumption of the device.

3.6 MCF8315 Thermal Performance Test

3.6.1 MCF8315 TSSOP Thermal Test With Inductance Version

The following test run the MCF8315 TSSOP at 24V and 1.25A (**30W**), output peak current approximately 2.3A(73Hz), **two layer PCB** test result. **(PWM switching frequency :15KHz)**

Ambient temperature is 26°C, temperature rise is about 68°C.

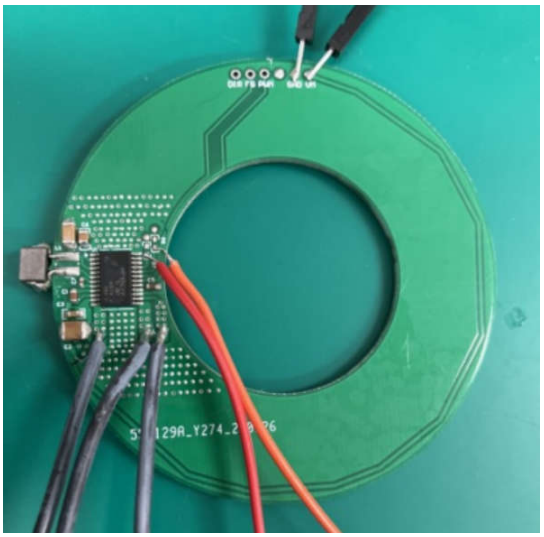

Figure 3-9. MCF8315 Two Layer With Inductance Version PCB

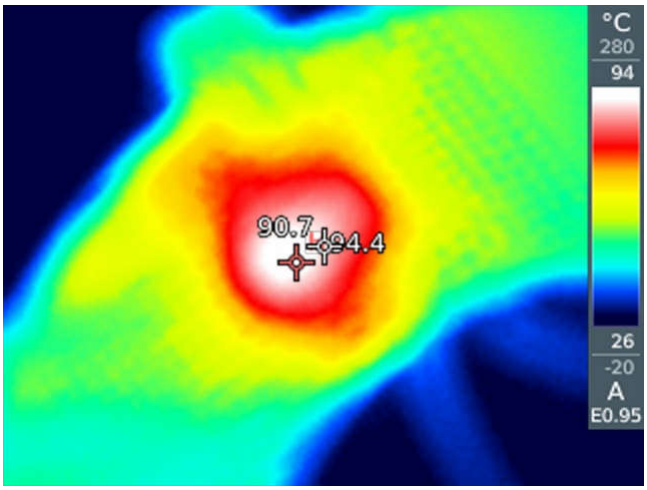

Figure 3-10. MCF8315 Two Layer With Inductance 30W Thermal Test Result

The following test run the MCF8315 TSSOP at 24V and 0.89A (approximately **20W**), out output peak current approximately 2.1A(68Hz). **Single layer PCB** test result. **(PWM switching frequency :15KHz)**

Ambient temperature is 27°C, temperature rise is about 57.5°C.

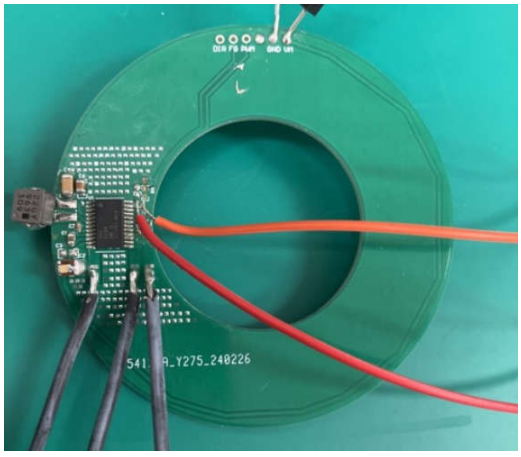

Figure 3-11. MCF8315 Single Layer With Inductance Version PCB

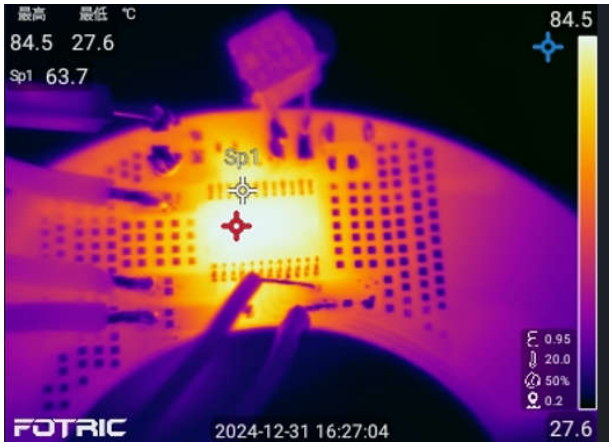

Figure 3-12. MCF8315 Single Layer With Inductance 20W Thermal Test Result

4 Summary

This application note discusses the application cases of fans, summarizes the hardware design using the MCF8315 device, achieves system-level optimization in the integrated design, and proposes a more cost-effective design based on this. The document also uses different PCBs to optimize the device temperature rise to achieve the best design for cost and performance.

5 References

- Texas Instruments, *MCF8315A Sensorless Field Oriented Control (FOC) Integrated FET BLDC Driver*, data sheet.
- Texas Instruments, *MCF8316A Tuning Guide*, user's guide.
- Texas Instruments, *How to Design a Thermally-Efficient Integrated BLDC Motor Drive PCB*, application note.
- Texas Instruments, *MCF8316A -Design Challenges and Solution*, application note.
- Texas Instruments, *How to Use the MCF831x to Solve Thermal and Quick Startup Challenges*, application note.
- Texas Instruments, *24V, 35W Sensorless FOC BLDC Reference Design With 85VAC to 265VAC, PF of 0.92, Single-Stage PFC*, design guide.

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